

# **DLP470TE 0.47-Inch 4K UHD Digital Micromirror Device**

### 1 Features

- 0.47-Inch diagonal micromirror array
  - 4K UHD (3840 × 2160) display resolution
  - 5.4-micron micromirror pitch
  - ±17° micromirror tilt (relative to flat surface)
  - Bottom illumination
- 2xLVDS input data bus
- The DLP470TE chipset includes:
  - DLP470TE DMD
  - DLPC4420 controller
  - DLPA100 controller power management and motor driver IC

## 2 Applications

- 4K UHD display
- Laser TV
- **Business and education**
- Digital signage
- Gaming
- Home cinema

## 3 Description

The TI DLP470TE digital micromirror device (DMD) is a digitally controlled micro-electromechanical system (MEMs) spatial light modulator (SLM) that enables bright, full 4K UHD display solutions. When coupled with the appropriate optical system, the DLP470TE DMD displays true 4K UHD resolution (over 8 million pixels on screen) and is capable of delivering accurate, detailed images to a variety of surfaces. The DLP470TE DMD, together with the DLPC4420 display controller, the DLPA100 controller power and motor driver provides the capability to achieve high performance systems and is a great fit for 4K UHD high brightness display applications in a smaller package.

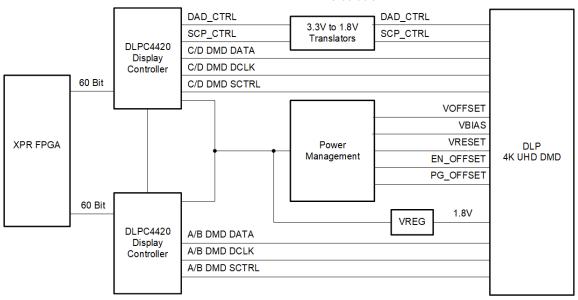
The DMD ecosystem includes established resources to help the user accelerate the design cycle, visit the DLP® Products third-party search tools to find approved optical module manufacturers and third party providers.

Visit Getting Started With TI DLP Display Technology to learn more about how to start designing with the DMD.

### **Device Information**

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE	
DLP470TE	FXJ (257)	32.2mm × 22.3mm	

For more information, see the Mechanical, Packaging, and Orderable addendum.



**DLP470TE Simplified Application** 



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# 4 Pin Configuration and Functions

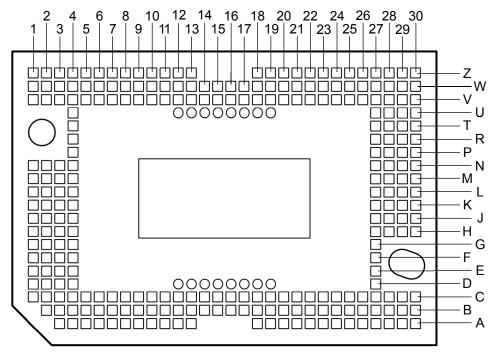


Figure 4-1. Series 410 Package. 257-pin FXJ. Bottom View.

#### **CAUTION**

To ensure reliable, long-term operation of the .47-inch 4K UHD S410 DMD, it is critical to properly manage the layout and operation of the signals identified in the table below. For specific details and guidelines, refer to the *PCB Design Requirements for TI DLP Standard TRP Digital Micromirror Devices* application report before designing the board.

Table 4-1. Pin Functions

PIN		(1)	(1)	(4)		DATA	INTERNAL		TRACE
NAME	NO.	I/O <sup>(1)</sup>	SIGNAL	RATE TERMINATION		DESCRIPTION	LENGTH (mil)		
D_AN(0)	C6								
D_AN(1)	C3								
D_AN(2)	E1								
D_AN(3)	C4								
D_AN(4)	D1								
D_AN(5)	B8								
D_AN(6)	F4								
D_AN(7)	E3	1.	LVDC	DDB	Differential	Data pagativa	905.0		
D_AN(8)	C11	] '	LVDS	DDR	Differential	Data negative	805.0		
D_AN(9)	F3								
D_AN(10)	K4								
D_AN(11)	НЗ								
D_AN(12)	J3								
D_AN(13)	C13								
D_AN(14)	A5								
D_AN(15)	A3								

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PIN				ВАТА	INTERNAL		TRACE
NAME	NO.	I/O <sup>(1)</sup>	SIGNAL	RATE	TERMINATION	DESCRIPTION	LENGTH (mil)
D_AP(0)	C7						
D_AP(1)	C2						
D_AP(2)	E2						
D_AP(3)	B4						
D_AP(4)	C1						
D_AP(5)	B7						
D_AP(6)	E4						
D_AP(7)	D3		LVDS	DDR	Differential	Data positive	805.0
D_AP(8)	C12	] '	LVDS	DDK	Differential	Data positive	005.0
D_AP(9)	F2						
D_AP(10)	J4						
D_AP(11)	G3						
D_AP(12)	J2						
D_AP(13)	C14						
D_AP(14)	A6						
D_AP(15)	A4						
D_BN(0)	N4						
D_BN(1)	Z11						
D_BN(2)	W4						
D_BN(3)	W10						
D_BN(4)	L1						
D_BN(5)	V8						
D_BN(6)	W6						
D_BN(7)	M1		LVDS	DDR	Differential	Data negative	805.0
D_BN(8)	R4	] '	LVDS	DDK	Differential	Data negative	005.0
D_BN(9)	W1						
D_BN(10)	U4						
D_BN(11)	V2						
D_BN(12)	Z5						
D_BN(13)	N3						
D_BN(14)	Z2						
D_BN(15)	L4						



PIN				DATA	INTERNAL		TRACE						
NAME	NO.	I/O <sup>(1)</sup>	SIGNAL	RATE	TERMINATION	DESCRIPTION	LENGTH (mil)						
D_BP(0)	M4												
D_BP(1)	Z12												
D_BP(2)	Z4												
D_BP(3)	Z10												
D_BP(4)	L2												
D_BP(5)	V9												
D_BP(6)	W7												
D_BP(7)	N1	1	LVDS	DDR	Differential	Data positive	805.0						
D_BP(8)	P4	<b>1</b> '	LVDS	DUK	Differential	Data positive	005.0						
D_BP(9)	V1												
D_BP(10)	T4												
D_BP(11)	V3												
D_BP(12)	Z6												
D_BP(13)	N2												
D_BP(14)	Z3												
D_BP(15)	L3												
D_CN(0)	H27												
D_CN(1)	A20												
D_CN(2)	H28												
D_CN(3)	K28												
D_CN(4)	K30												
D_CN(5)	C23												
D_CN(6)	G27												
D_CN(7)	J30	1	LVDS	DDR	Differential	Data negative	805.0						
D_CN(8)	B24	] '	LVDS	DDK	Differential	Data negative	605.0						
D_CN(9)	A21												
D_CN(10)	A27												
D_CN(11)	C29												
D_CN(12)	A26												
D_CN(13)	C25												
D_CN(14)	A29												
D_CN(15)	C30												



PIN		I/O <sup>(1)</sup>										DATA	INTERNAL		TRACE
NAME	NO.		SIGNAL	RATE	TERMINATION	DESCRIPTION	LENGTH (mil)								
D_CP(0)	J27														
D_CP(1)	A19														
D_CP(2)	H29														
D_CP(3)	K27														
D_CP(4)	K29														
D_CP(5)	C22														
D_CP(6)	F27														
D_CP(7)	H30	1.	1)/D0	DDD	Differential	D.4	005.0								
D_CP(8)	B25	I	LVDS	DDR	Differential	Data positive	805.0								
D_CP(9)	B21														
D_CP(10)	B27														
D_CP(11)	C28														
D_CP(12)	A25														
D_CP(13)	C24														
D_CP(14)	A28	1													
D_CP(15)	B30														
D_DN(0)	V25						805.0								
D_DN(1)	V28														
D_DN(2)	T30														
D_DN(3)	V27														
D_DN(4)	U30														
D_DN(5)	W23														
D_DN(6)	R27														
D_DN(7)	T28		LVDS	DDR	Differential	Data negative									
D_DN(8)	V20	·	LVDS	DDR	Differential	Data negative									
D_DN(9)	R28														
D_DN(10)	L27														
D_DN(11)	N28														
D_DN(12)	M28														
D_DN(13)	V18														
D_DN(14)	Z26														
D_DN(15)	Z28														

PIN			Tubic			continued)	TRACE
NAME	NO.	I/O <sup>(1)</sup>	SIGNAL	DATA RATE	INTERNAL TERMINATION	DESCRIPTION	LENGTH (mil)
D_DP(0)	V24						805.0
D_DP(1)	V29	1					
D_DP(2)							
D_DP(3)	W27	-					
D_DP(4)	V30	1					
D DP(5)	W24	1					
D_DP(6)	T27	1					
D_DP(7)	U28	1.			D. 6		
D_DP(8)	V19	- I	LVDS	DDR	Differential	Data positive	
D_DP(9)	R29	1					
D_DP(10)	M27	1					
D_DP(11)	P28						
D_DP(12)	M29	1					
D_DP(13)	V17						
D_DP(14)	Z25	1					
D_DP(15)	Z27	1					
SCTRL_AN	G1	ı	LVDS	DDR	Differential	Serial control negative <sup>(2)</sup>	805.0
SCTRL_AP	F1	ı	LVDS	DDR	Differential	Serial control negative <sup>(2)</sup>	805.0
SCTRL_BN	V5	I	LVDS	DDR	Differential	Serial control negative <sup>(2)</sup>	805.0
SCTRL_BP	V4	I	LVDS	DDR	Differential	Serial control negative <sup>(2)</sup>	805.0
SCTRL_CN	C26	I	LVDS	DDR	Differential	Serial control negative <sup>(2)</sup>	805.0
SCTRL_CP	C27	I	LVDS	DDR	Differential	Serial control positive <sup>(2)</sup>	805.0
SCTRL_DN	P30	I	LVDS	DDR	Differential	Serial control negative <sup>(2)</sup>	805.0
SCTRL_DP	R30	I	LVDS	DDR	Differential	Serial control positive <sup>(2)</sup>	805.0
DCLK_AN	H2	I	LVDS		Differential	Clock negative <sup>(2)</sup>	805.0
DCLK_AP	H1	I	LVDS		Differential	Clock positive <sup>(2)</sup>	805.0
DCLK_BN	V6	I	LVDS		Differential	Clock negative <sup>(2)</sup>	805.0
DCLK_BP	V7	I	LVDS		Differential	Clock positive <sup>(2)</sup>	805.0
DCLK_CN	D27	I	LVDS		Differential	Clock negative <sup>(2)</sup>	805.0
DCLK_CP	E27	I	LVDS		Differential	Clock positive <sup>(2)</sup>	805.0
DCLK_DN	N29	I	LVDS		Differential	Clock negative <sup>(2)</sup>	805.0
DCLK_DP	N30	I	LVDS		Differential	Clock positive <sup>(2)</sup>	805.0
SCPCLK	A10	I	LVCMOS		Pulldown	Serial communications port clock. Active only when SCPENZ is logic low <sup>(2)</sup>	
SCPDI	A12	I	LVCMOS	SDR	Pulldown	Serial communications port data input. Synchronous to SCPCLK rising edge <sup>(2)</sup>	
SCPENZ	C10	I	LVCMOS		Pulldown	Serial communications port enable active low <sup>(2)</sup>	
SCPDO	A11	0	LVCMOS	SDR		Serial communications port output	
RESET_ADDR(0)	Z13						
RESET_ADDR(1)	W13	1 .	11/01/02		Dullder	Doort driver address14(2)	
RESET_ADDR(2)	V10	- I	LVCMOS		Pulldown	Reset driver address select <sup>(2)</sup>	
RESET_ADDR(3)	W14	1					



PIN				DATA	INTERNAL	,	TRACE
NAME	NO.	I/O <sup>(1)</sup>	SIGNAL	RATE	TERMINATION	DESCRIPTION	LENGTH (mil)
RESET_MODE(0)	W9					Reset driver mode select <sup>(2)</sup>	
RESET_SEL(0)	V14	I	LVCMOS		Pulldown	Reset driver level select <sup>(2)</sup>	
RESET_SEL(1)	Z8				Reset driver level select <sup>(2)</sup>		
RESET_STROBE	<b>Z</b> 9	I	LVCMOS		Pulldown	Rising edge latches in RESET_ADDR, RESET_MODE, and RESET_SEL. <sup>(2)</sup>	
PWRDNZ	A8	ı	LVCMOS		Pulldown	Active low device reset. <sup>(2)</sup>	
RESET_OEZ	W15	I	LVCMOS		Pullup	Active low output enable for internal reset driver circuits. (2)	
RESET_IRQZ	V16	0	LVCMOS			Active low output interrupt to the DLP® display controller	
EN_OFFSET	C9	0	LVCMOS			Active high enable for external V <sub>OFFSET</sub> regulator	
PG_OFFSET	A9	_	LVCMOS		Pullup	Active low fault from external V <sub>OFFSET</sub> regulator <sup>(2)</sup>	
TEMP_N	B18		Analog			Temperature sensor diode cathode	
TEMP_P	B17		Analog			Temperature sensor diode anode	
RESERVED **MUST VERIFY WITH SRC DATA SHEET	D12, D13, D14, D15, D16, D17, D18, D19, U12, U13, U14, U15	NC	Analog		Pulldown	Do not connect on the DLP® system board. No connect. No electrical connections from CMOS bond pad to package pin	
No Connect	U16, U17, U18, U19	NC				No connect. No electrical connection from the CMOS bond pad to package pin	
RESERVED_BA	W11						
RESERVED_BB	B11	0	LVCMOS			Do not connect on the DLP system board.	
RESERVED_BC	Z20	O	LVCIVIOS			Do not connect on the DEI system board.	
RESERVED_BD	C18						
RESERVED_PFE	A18	ı	LVCMOS		Pulldown	Connect to ground on the DLP system board.	
RESERVED_TM	C8		2.000		T dilidowii	Sommost to ground on the BE. System Board.	
RESERVED_TP0	Z19						
RESERVED_TP1	W20	I	Analog			Do not connect on the DLP system board.	
RESERVED_TP2	W19						
V <sub>BIAS</sub> (3)	C15, C16, V11, V12	Р	Analog			Supply voltage for positive bias level of micromirror reset signal	
V <sub>RESET</sub> (3)	G4, H4, J1, K1	Р	Analog			Supply voltage for negative reset level of micromirror reset signal	
V <sub>OFFSET</sub> (3)	A30, B2, M30, Z1, Z30	Р	Analog			Supply voltage for HVCMOS logic. Supply voltage for positive offset level of micromirror reset signal. Supply voltage for stepped high voltage at micromirror address electrodes	

Table 4-1. Pin Functions (continued)									
PIN		I/O <sup>(1)</sup>	SIGNAL	DATA	INTERNAL	DESCRIPTION	TRACE LENGTH		
NAME	NO.	1/0(1)	SIGNAL	RATE	TERMINATION	DESCRIPTION	(mil)		
V <sub>CC</sub> <sup>(3)</sup>	A24, A7, B10, B13, B16, B19, B22, B28, B5, C17, C20, D4, J29, K2, L29, M2, N27, U27, V13, V15, V22, W17, W21, W26, W29, W3, Z18, Z23, Z29, Z7	Р	Analog			Supply voltage for LVCMOS core. Supply voltage for positive offset level of micromirror reset signal during power down. Supply voltage for normal high level at micromirror address electrodes			
Vss <sup>(4)</sup>	A13, A22, A23, B12, B14, B15, B20, B23, B26, B29, B3, B6, B9, C19, C21, C5, D2, G2, J28, K3, L28, L30, M3, P27, P29, U29, V21, V23, V26, W12, W16, W18, W2, W22, W25, W28, W30, W5, W8, Z21, Z22, Z24	G				Device ground. Common return for all power			

<sup>(1)</sup> I = Input, O = Output, P = Power, G = Ground, NC = No connect

<sup>(2)</sup> These signals are very sensible to noise or intermittent power connections, which can cause irreversible DMD micromirror array damage or, to a lesser extent, image disruption. Consider this precaution during DMD board design and manufacturer handling of the DMD subassemblies.

<sup>(3)</sup> V<sub>BIAS</sub>, V<sub>CC</sub>, V<sub>OFFSET</sub>, and V<sub>RESET</sub> power supplies must be connected for proper DMD operation.

<sup>(4)</sup> V<sub>SS</sub> must be connected for proper DMD operation.



## **5 Specifications**

## 5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted). Stresses beyond those listed under Section 5.1 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device is not implied at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure above or below the *Recommended Operating Conditions*. Exposure above or below the *Recommended Operating Conditions* for extended periods may affect device reliability.

		MIN	MAX	UNIT
SUPPLY VOLTAGE	S			
V <sub>CC</sub>	Supply voltage for LVCMOS core logic <sup>(1)</sup>	-0.5	2.3	V
V <sub>OFFSET</sub>	Supply voltage for HVCMOS and micromirror electrode <sup>(1)</sup> (2)	-0.5	11	V
V <sub>BIAS</sub>	Supply voltage for micromirror electrode <sup>(1)</sup>	-0.5	19	V
V <sub>RESET</sub>	Supply voltage for micromirror electrode <sup>(1)</sup>	-15	-0.3	V
V <sub>BIAS</sub> – V <sub>OFFSET</sub>	Supply voltage difference (absolute value) <sup>(3)</sup>		11	V
V <sub>BIAS</sub> – V <sub>RESET</sub>	Supply voltage difference (absolute value) <sup>(4)</sup>		34	V
INPUT VOLTAGES		-	-	
	Input voltage for all other LVCMOS input pins <sup>(1)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
	Input voltage for all other LVDS input pins (1) (5)	-0.5	V <sub>CC</sub> + 0.5	V
V <sub>ID</sub>	Input differential voltage (absolute value) <sup>(6)</sup>		500	mV
I <sub>ID</sub>	Input differential current <sup>(5)</sup>		6.3	mA
Clocks		'		
fclock	Clock frequency for LVDS interface, DCLK_A		400	MHz
$f_{CLOCK}$	Clock frequency for LVDS interface, DCLK_B		400	MHz
fclock	Clock frequency for LVDS interface, DCLK_C		400	MHz
fclock	Clock frequency for LVDS interface, DCLK_D		400	MHz
ENVIRONMENTAL				
T <sub>ARRAY</sub> and	Temperature, operating <sup>(7)</sup>	0	90	°C
T <sub>WINDOW</sub>	Temperature, non-operating <sup>(7)</sup>	-40	90	°C
T <sub>DELTA</sub>	Absolute temperature delta between any point on the window edge and the ceramic test point TP1 <sup>(8)</sup>		30	°C
T <sub>DP</sub>	Dew point temperature, operating and non-operating (non-condensing)		81	°C

- All voltages are referenced to common ground V<sub>SS</sub>. V<sub>BIAS</sub>, V<sub>CC</sub>, V<sub>OFFSET</sub>, and V<sub>RESET</sub> power supplies are all required for proper DMD operation. V<sub>SS</sub> must also be connected.
- (2) V<sub>OFFSET</sub> supply transients must fall within specified voltages.
- (3) Exceeding the recommended allowable voltage difference between V<sub>BIAS</sub> and V<sub>OFFSET</sub> may result in excessive current draw.
- (4) Exceeding the recommended allowable voltage difference between V<sub>BIAS</sub> and V<sub>RESET</sub> may result in excessive current draw.
- (5) LVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
- (6) This maximum LVDS input voltage rating applies when each input of a differential pair is at the same voltage potential.
- (7) The highest temperature of the active array (as calculated using *Micromirror Array Temperature Calculation*) or of any point along the window edge as defined in Figure 6-1. The locations of thermal test points TP2, TP3, TP4, and TP5 in Figure 6-1 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, use that location.
- (8) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in Figure 6-1. The window test points TP2, TP3, TP4, and TP5 shown in Figure 6-1 are intended to result in the worst case delta. If a particular application causes another point on the window edge to result in a larger delta temperature, use that location.

Applicable for the DMD as a component or non-operating in a system.

## 5.2 Storage Conditions

	<u> </u>			
		MIN	MAX	UNIT
$T_{DMD}$	DMD storage temperature	-40	80	°C



**5.2 Storage Conditions (continued)** 

		MIN	MAX	UNIT
T <sub>DP-AVG</sub>	Average dew point temperature (non-condensing) (1)		28	°C
T <sub>DP-ELR</sub>	Elevated dew point temperature range (non-condensing) (2)	28	36	°C
CT <sub>ELR</sub>	Cumulative time in elevated dew point temperature range		24	months

- (1) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
- (2) Limit the exposure to dew point temperatures in the elevated range during storage and operation to less than a total cumulative time of CT<sub>ELR</sub>.

## 5.3 ESD Ratings

				VALUE	UNIT
	V <sub>(ESD)</sub>	Electrostatic	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		discharge Charged device	Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	V

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## **5.4 Recommended Operating Conditions**

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by this table. No level of performance is implied when operating the device above or below these limits.

		MIN	NOM	MAX	UNIT
VOLTAGE SUPP	PLY				
V <sub>CC</sub>	LVCMOS logic supply voltage <sup>(1)</sup>	1.65	1.8	1.95	V
V <sub>OFFSET</sub>	Mirror electrode and HVCMOS voltage <sup>(1) (2)</sup>	9.5	10	10.5	V
V <sub>BIAS</sub>	Mirror electrode voltage <sup>(1)</sup>	17.5	18	18.5	V
V <sub>RESET</sub>	Mirror electrode voltage <sup>(1)</sup>	-14.5	-14	-13.5	V
V <sub>BIAS</sub> – V <sub>OFFSET</sub>	Supply voltage difference (absolute value) <sup>(3)</sup>			10.5	V
V <sub>BIAS</sub> – V <sub>RESET</sub>	Supply voltage difference (absolute value) <sup>(4)</sup>			33	V
LVCMOS INTER	FACE				
V <sub>IH(DC)</sub>	DC input high voltage <sup>(5)</sup>	0.7 × V <sub>CC</sub>		V <sub>CC</sub> + 0.3	V
V <sub>IL(DC)</sub>	DC input low voltage <sup>(5)</sup>	-0.3		0.3 × V <sub>CC</sub>	V
V <sub>IH(AC)</sub>	AC input high voltage <sup>(5)</sup>	0.8 × V <sub>CC</sub>		V <sub>CC</sub> + 0.3	V
V <sub>IL(AC)</sub>	AC input low voltage <sup>(5)</sup>	-0.3		0.2 × V <sub>CC</sub>	V
t <sub>PWRDNZ</sub>	PWRDNZ pulse duration <sup>(6)</sup>	10			ns
SCP INTERFAC	E				
$f_{\sf SCPCLK}$	SCP clock frequency <sup>(7)</sup>			500	kHz
t <sub>SCP_PD</sub>	Propagation delay, Clock to Q, from rising-edge of SCPCLK to valid SCPDO <sup>(8)</sup>	0		900	ns
t <sub>SCP_NEG_ENZ</sub>	Time between falling-edge of SCPENZ and the first rising- edge of SCPCLK	1			μs
t <sub>SCP_POS_ENZ</sub>	Time between falling-edge of SCPCLK and the rising-edge of SCPENZ	1			μs
t <sub>SCP_DS</sub>	SCPDI Clock setup time (before SCPCLK falling edge) <sup>(8)</sup>	800			ns
t <sub>SCP_DH</sub>	SCPDI Hold time (after SCPCLK falling edge) <sup>(8)</sup>	900			ns
t <sub>SCP_PW_ENZ</sub>	SCPENZ inactive pulse duration (high level)	2			μs

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## 5.4 Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by this table. No level of performance is implied when operating the device above or below these limits.

•		MIN	NOM	MAX	UNIT
LVDS INTERI	FACE				
$f_{CLOCK}$	Clock frequency for LVDS interface (all channels), DCLK <sup>(9)</sup>			400	MHz
V <sub>ID</sub>	Input differential voltage (absolute value) <sup>(10)</sup>	150	300	440	mV
V <sub>CM</sub>	Common mode voltage <sup>(10)</sup>	1100	1200	1300	mV
V <sub>LVDS</sub>	LVDS voltage <sup>(10)</sup>	880		1520	mV
t <sub>LVDS_RSTZ</sub>	Time required for LVDS receivers to recover from PWRDNZ			2000	ns
Z <sub>IN</sub>	Internal differential termination resistance	80	100	120	Ω
Z <sub>LINE</sub>	Line differential impedance (PWB/trace)	90	100	110	Ω
ENVIRONME	NTAL	-			
т	Array temperature, long–term operational <sup>(11)</sup> (12) (13)	10		40 to 70 <sup>(14)</sup>	°C
T <sub>ARRAY</sub>	Array temperature, short–term operational, 500 hr max <sup>(12)</sup> (15)	0		10	°C
T <sub>WINDOW</sub>	Window temperature – operational <sup>(16)</sup> (22)			85	°C
T <sub>DELTA</sub>	Absolute temperature delta between any point on the window edge and the ceramic test point TP1 <sup>(17)</sup>			14	°C
T <sub>DP -AVG</sub>	Average dew point temperature (non–condensing) <sup>(18)</sup>			28	°C
T <sub>DP-ELR</sub>	Elevated dew point temperature range (non-condensing) <sup>(19)</sup>	28		36	°C
CT <sub>ELR</sub>	Cumulative time in elevated dew point temperature range			24	Months
ILL <sub>θ</sub>	Illumination marginal ray angle <sup>(22)</sup>			55	degrees
SOLID STATE	E ILLUMINATION				
ILL <sub>UV</sub>	Illumination power at wavelengths < 410nm <sup>(11)</sup> (21)			10	mW/cm2
ILL <sub>VIS</sub>	Illumination power at wavelengths ≥ 410nm and ≤ 800nm (20) (21)			44.9	W/cm2
ILL <sub>IR</sub>	Illumination power at wavelengths > 800nm <sup>(21)</sup>			10	mW/cm2
ILL <sub>BLU</sub>	Illumination power at wavelengths ≥ 410nm and ≤ 475nm <sup>(20)</sup> (21)			14.3	W/cm2
ILL <sub>BLU1</sub>	Illumination power at wavelengths ≥ 410nm and ≤ 440nm <sup>(20)</sup> <sup>(21)</sup>			2.3	W/cm2
LAMP ILLUM	IINATION				
ILL <sub>UV</sub>	Illumination power at wavelengths < 395nm <sup>(11)</sup> (21)			2.0	mW/cm2
ILL <sub>VIS</sub>	Illumination power at wavelengths ≥ 395nm and ≤ 800nm <sup>(20)</sup> (21)			36.8	W/cm2
ILL <sub>IR</sub>	Illumination power at wavelengths > 800nm <sup>(21)</sup>			10	mW/cm2

- (1) All voltages are referenced to common ground V<sub>SS</sub>. V<sub>BIAS</sub>, V<sub>CC</sub>, V<sub>OFFSET</sub>, and V<sub>RESET</sub> power supplies are all required for proper DMD operation. V<sub>SS</sub> must also be connected.
- (2) V<sub>OFFSET</sub> supply transients must fall within specified max voltages.
- (3) To prevent excess current, the supply voltage delta |V<sub>BIAS</sub> V<sub>OFFSET</sub>| must be less than the specified limit. See Section 8, Figure 8-1, Table 8-1
- (4) To prevent excess current, the supply voltage delta |V<sub>BIAS</sub> V<sub>RESET</sub>| must be less than the specified limit. See Section 8, Figure 8-1,
- (5) The low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, "Low-Power Double Data Rate (LPDDR)" JESD209B. Tester Conditions for VIH and VIL.
  - Frequency = 60MHz. Maximum Rise Time = 2.5ns @ (20% 80%)
  - Frequency = 60MHz. Maximum Fall Time = 2.5ns @ (80% 20%)
- (6) PWRDNZ input pin resets the SCP and disables the LVDS receivers. PWRDNZ input pin overrides SCPENZ input pin and tristates the SCPDO output pin.
- (7) The SCP clock is a gated clock. Duty cycle shall be 50% ± 10%. SCP parameter is related to the frequency of DCLK.
- (8) See Figure 5-2
- (9) See LVDS Timing Requirements in Section 5.8 and Figure 5-6.
- (10) Refer to Figure 5-5.
- (11) Simultaneous exposure of the DMD to the maximum Section 5.4 for temperature and UV illumination reduces device lifetime.
- (12) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in Figure 6-1 and the package Section 5.5 using the calculation in Section 6.6.

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- (13) Long-term is defined as the usable life of the device.
- (14) Per Figure 5-1, the maximum operational array temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. See Section 6.8 for a definition of micromirror landed duty cycle.
- (15) Short-term is defined as cumulative time over the usable life of the device.
- (16) The locations of thermal test points TP2, TP3, TP4, and TP5 in Figure 6-1 are intended to measure the highest window edge temperature. For most applications, the locations shown are representative of the highest window edge temperature. If a particular application causes additional points on the window edge to be at a higher temperature, test points should be added to those locations.
- (17) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in Figure 6-1. The window test points TP2, TP3, TP4, and TP5 shown in Figure 6-1 are intended to result in the worst-case delta temperature. If a particular application causes another point on the window edge to result in a larger delta in temperature, that point should be used.
- (18) The average over time (including storage and operating) that the device is not in the "elevated dew point temperature range."
- (19) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT<sub>ELR</sub>.
- (20) The maximum allowable optical power incident on the DMD is limited by the maximum optical power density for each wavelength range specified and the micromirror array temperature (T<sub>ARRAY</sub>).
- (21) To calculate see Section 6.7.
- (22) The maximum marginal ray angle of the incoming illumination light at any point in the micromirror array, including the 8V micromirrors (POM), should not exceed 55 degrees from the normal to the device array plane. The device window aperture has not necessarily been designed to allow incoming light at higher maximum angles to pass to the micromirrors, and the device performance has not been tested nor qualified at angles exceeding this. Illumination light exceeding this angle outside the micromirror array (including POM) will contribute to thermal limitations described in this document, and may negatively affect lifetime.

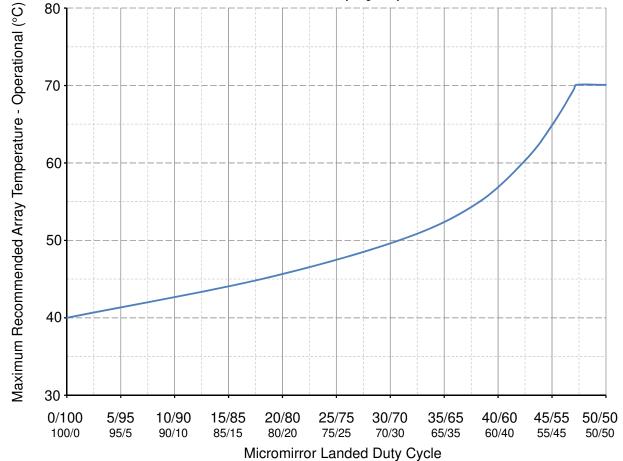


Figure 5-1. Maximum Recommended Array Temperature—Derating Curve



#### 5.5 Thermal Information

	DLP470TE	
THERMAL METRIC	FXJ Package	UNIT
	257 PINS	
Thermal resistance, active area to test point 1 (TP1) <sup>(1)</sup>	0.90	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package where it can be removed by an appropriate heat sink. The heat sink and cooling system must be capable of maintaining the package within the temperature range specified in the Section 5.4.

The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array.

Optical systems need to be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

Over operating free-air temperature range (unless otherwise noted).

#### 5.6 Electrical Characteristics

	PARAMETER	TEST CONDITIONS	MIN	TYP MAX	UNIT
V <sub>OH</sub>	High level output voltage	V <sub>CC</sub> = 1.8V, I <sub>OH</sub> = -2mA	0.8 × V <sub>CC</sub>		V
V <sub>OL</sub>	Low level output voltage	V <sub>CC</sub> = 1.95V, I <sub>OL</sub> = 2mA		0.2 × V <sub>CC</sub>	V
l <sub>oz</sub>	High impedance output current	V <sub>CC</sub> = 1.95V	-40	25	μΑ
I <sub>IL</sub>	Low level input current	V <sub>CC</sub> = 1.95V, V <sub>I</sub> = 0	-1		μA
I <sub>IH</sub>	High level input current <sup>(1)</sup>	$V_{CC} = 1.95V, V_I = V_{CC}$		110	μA
I <sub>CC</sub>	Supply current V <sub>CC</sub> <sup>(2)</sup>	V <sub>CC</sub> = 1.95V		1500	mA
I <sub>OFFSET</sub>	Supply current V <sub>OFFSET</sub> (3)	V <sub>OFFSET</sub> = 10.5V		13.2	mA
I <sub>BIAS</sub>	Supply current V <sub>BIAS</sub> (3) (4)	V <sub>BIAS</sub> = 18.5V		3.6	mA
I <sub>RESET</sub>	Supply current V <sub>RESET</sub> (4)	V <sub>RESET</sub> = -14.5V		<b>–</b> 9	mA
Pcc	Supply power dissipation V <sub>CC</sub>	V <sub>CC</sub> = 1.95V		2925.0	mW
P <sub>OFFSET</sub>	Supply power dissipation V <sub>OFFSET</sub> (3)	V <sub>OFFSET</sub> = 10.5V		138.6	mW
P <sub>BIAS</sub>	Supply power dissipation V <sub>BIAS</sub> <sup>(3)</sup> <sup>(4)</sup>	V <sub>BIAS</sub> = 18.5V		66.6	mW
P <sub>RESET</sub>	Supply power dissipation V <sub>RESET</sub> <sup>(4)</sup>	V <sub>RESET</sub> = -14.5V		130.5	mW
P <sub>TOTAL</sub>	Supply power dissipation V <sub>TOTAL</sub>			3260.7	mW

- (1) Applies to LVCMOS pins only. Excludes LVDS pins and MBRST (15:0) pins.
- (2) See the Pin Functions table for pull-up and pull-down configuration per device pin.
- (3) To prevent excess current, the supply voltage difference |V<sub>BIAS</sub> V<sub>OFFSET</sub>| must be less than the specified limits listed in the Recommended Operating Conditions table.
- (4) To prevent excess current, the supply voltage difference |V<sub>BIAS</sub> V<sub>RESET</sub>| must be less than specified limit in Recommended Operating Conditions

### 5.7 Capacitance at Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C <sub>I_lvds</sub>	LVDS input capacitance 2xLVDS	f = 1 MHz			20	pF
C <sub>I_nonlvds</sub>	Non-LVDS input capacitance 2xLVDS	f = 1 MHz			20	pF
C <sub>I_tdiode</sub>	Temperature diode input capacitance 2xLVDS	f = 1 MHz			30	pF
Co	Output capacitance	f = 1 MHz			20	pF



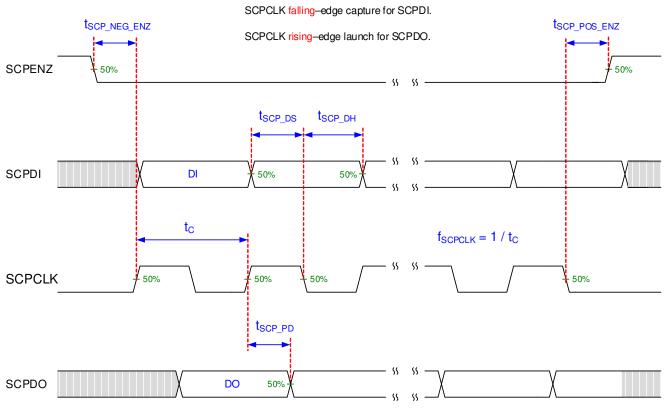
## 5.8 Timing Requirements

	ning Kequireni		MIN	NOM	MAX	UNIT
SCP <sup>(1)</sup>						
t <sub>r</sub>	Rise time	20% to 80% reference points			30	ns
t <sub>f</sub>	Fall time	80% to 20% reference points			30	ns
LVDS <sup>(2)</sup>						
t <sub>r</sub>	Rise slew rate	20% to 80% reference points	0.7	1		V/ns
t <sub>f</sub>	Fall slew rate	80% to 20% reference points	0.7	1		V/ns
		DCLK_A, LVDS pair	2.5			ns
	Ola ak ayala	DCLK_B, LVDS pair	2.5			ns
t <sub>C</sub>	Clock cycle	DCLK_C, LVDS pair	2.5			ns
		DCLK_D, LVDS pair	2.5			ns
		DCLK_A, LVDS pair	1.19	1.25		ns
	Dada a damatian	DCLK_B, LVDS pair	1.19	1.25		ns
t <sub>W</sub>	Pulse duration	DCLK_C, LVDS pair	1.19	1.25		ns
		DCLK_D, LVDS pair	1.19	1.25		ns
		D_A(15:0) before DCLK_A, LVDS pair	0.275			ns
		D_B(15:0) before DCLK_B, LVDS pair	0.275			ns
	Setup time	D_C(15:0) before DCLK_C, LVDS pair	0.275			ns
		D_D(15:0) before DCLK_D, LVDS pair	0.275			ns
t <sub>Su</sub>		SCTRL_A before DCLK_A, LVDS pair	0.275	,		ns
		SCTRL_B before DCLK_B, LVDS pair	0.275			ns
		SCTRL_C before DCLK_C, LVDS pair	0.275			ns
		SCTRL_D before DCLK_D, LVDS pair	0.275			ns
		D_A(15:0) after DCLK_A, LVDS pair	0.195			ns
		D_B(15:0) after DCLK_B, LVDS pair	0.195	,		ns
		D_C(15:0) after DCLK_C, LVDS pair	0.195			ns
	l lald time a	D_D(15:0) after DCLK_D, LVDS pair	0.195			ns
t <sub>h</sub>	Hold time	SCTRL_A after DCLK_A, LVDS pair	0.195			ns
		SCTRL_B after DCLK_B, LVDS pair	0.195			ns
		SCTRL_C after DCLK_C, LVDS pair	0.195			ns
		SCTRL_D after DCLK_D, LVDS pair	0.195			ns
t <sub>SKEW</sub>	Skew time	Channel B relative to channel A (3) (4)	-1.25		1.25	ns
t <sub>SKEW</sub>	Skew time	Channel D relative to channel C <sup>(5)</sup> (6), LVDS pair	-1.25		1.25	ns

- (1) See the specifications for rise time and fall time for SCP.
- (2) See the specifications the for timing requirements for LVDS.
- (3) Channel A (Bus A) includes the following LVDS pairs: DCLK\_AN and DCLK\_AP, SCTRL\_AN and SCTRL\_AP, D\_AN(15:0) and D\_AP(15:0).
- (4) Channel B (Bus B) includes the following LVDS pairs: DCLK\_BN and DCLK\_BP, SCTRL\_BN and SCTRL\_BP, D\_BN(15:0) and D\_BP(15:0).
- (5) Channel C (Bus C) includes the following LVDS pairs: DCLK\_CN and DCLK\_CP, SCTRL\_CN and SCTRL\_CP, D\_CN(15:0) and D CP(15:0).
- (6) Channel D (Bus D) includes the following LVDS pairs: DCLK\_DN and DCLK\_DP, SCTRL\_DN and SCTRL\_DP, D\_DN(15:0) and D\_DP(15:0).

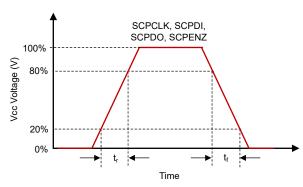


## 5.8.1 Timing Diagrams



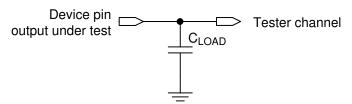
See Recommended Operating Conditions for  $f_{\text{SCP-LK}}$ ,  $t_{\text{SCP-DS}}$ ,  $t_{\text{SCP-DH}}$  and  $t_{\text{SCP-PD}}$  specifications.

Figure 5-2. SCP Timing Requirements



See *Timing Diagrams* for t<sub>r</sub> and t<sub>f</sub> specifications and conditions.

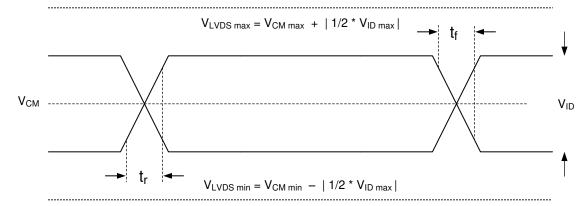
Figure 5-3. SCP Requirements for Rise and Fall



For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. System designers use IBIS or other simulation tools to correlate the timing reference load to a system environment.

Figure 5-4. Test Load Circuit for Output Propagation Measurement

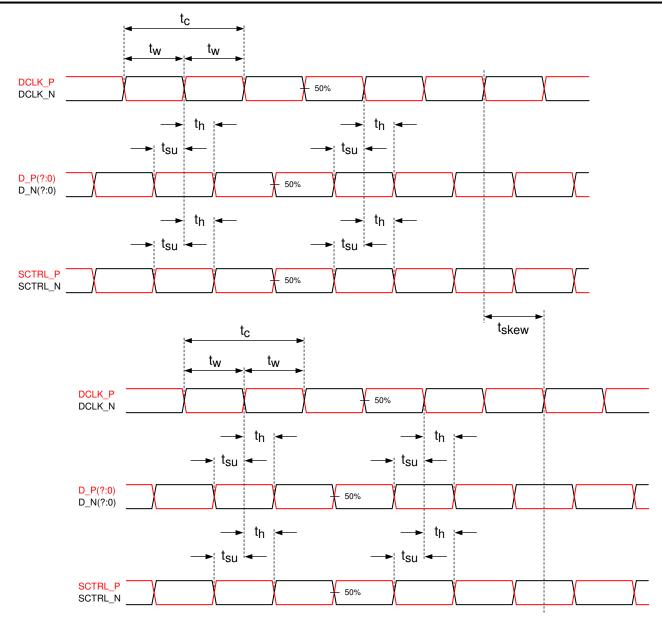




See Recommended Operating Conditions for  $V_{CM}$ ,  $V_{ID}$ , and  $V_{LVDS}$  specifications and conditions.

Figure 5-5. LVDS Waveform Requirements





See Timing Diagrams for timing requirements and LVDS pairs per channel (bus) defining D\_P(?:0) and D\_N(?:0).

Figure 5-6. Timing Requirements

# 5.9 System Mounting Interface Loads

Table 5-1. System Mounting Interface Loads

PARAMETER	MIN	NOM	MAX	UNIT
Thermal interface area <sup>(1)</sup>			12	kg
Electrical interface area <sup>(1)</sup>			25	kg

(1) Uniformly distributed within area shown in Figure 5-7.



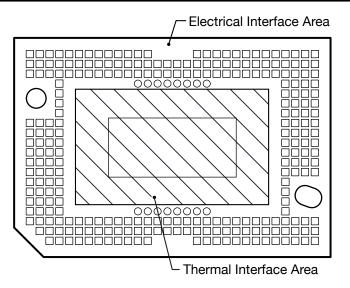


Figure 5-7. System Mounting Interface Loads

## **5.10 Micromirror Array Physical Characteristics**

**Table 5-2. Micromirror Array Physical Characteristics** 

PARAMETER DESCRIPTION			UNIT
Number of active columns (1)	M	1920	micromirrors
Number of active rows (1)	N	1080	micromirrors
Micromirror (pixel) pitch (1)	Р	5.4	μm
Micromirror active array width (1)	Micromirror pitch × number of active columns	10.368	mm
Micromirror active array height (1)	Micromirror pitch × number of active rows	5.832	mm
Micromirror active border (top / bottom) (2)	Pond of micromirrors (POM)	80	micromirrors/side
Micromirror active border (right / left) (2)	Pond of micromirrors (POM)	84	micromirrors/side

<sup>(1)</sup> See Figure 5-8

<sup>(2)</sup> The structure and qualities of the border around the active array includes a band of partially functional micromirrors referred to as the pond of micromirrors (POM). These micromirrors are prevented from tilting toward the bright or "on" state but still require an electrical bias to tilt toward "off."



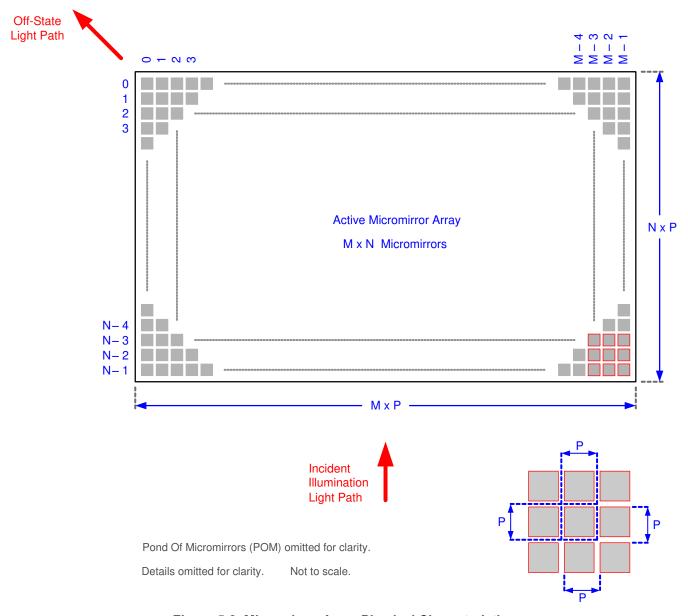


Figure 5-8. Micromirror Array Physical Characteristics

Refer to section Micromirror Array Physical Characteristics table for M, N, and P specifications.

## **5.11 Micromirror Array Optical Characteristics**

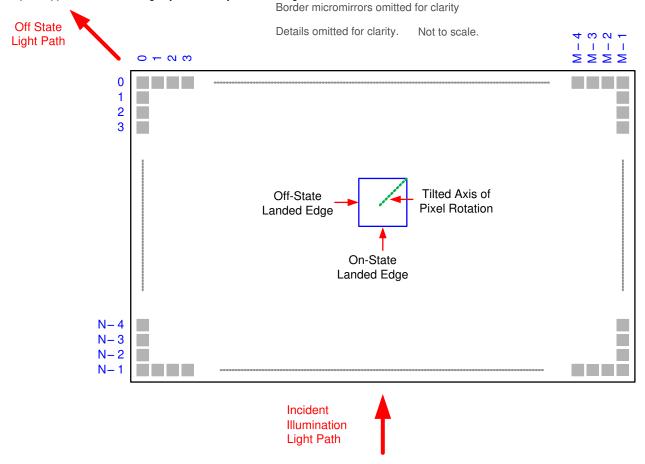
PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
Micromirror tilt angle, variation device to device (2) (3) (4) (5)		Landed State <sup>(1)</sup>	15.6	17	18.4	degrees
	Bright pixel(s) in active area <sup>(7)</sup>	Gray 10 screen <sup>(10)</sup>			0	
	Bright pixel(s) in the POM <sup>(7)</sup> (9)	Gray 10 screen <sup>(10)</sup>			1	
Image performance <sup>(6)</sup>	Dark pixel(s) in the active area <sup>(8)</sup>	White screen <sup>(11)</sup>			4	micromirrors
	Adjacent pixel(s)(12)	Any screen			0	
	Unstable pixel(s) in active area <sup>(13)</sup>	Any screen			0	

(1) Measured relative to the plane formed by the overall micromirror array.

(2) Additional variation exists between the micromirror array and the package datums.

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- (3) This represents the variation that can occur between any two individual micromirrors, locaed on the same device or located on different devices.
- (4) For some applications it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs the micromirror tilt angle variations within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations, or system contrast variations.
- (5) See figure Figure 5-9.
- (6) Conditions of acceptance. All DMD image performance returns are evaluated using the following projected image test conditions:
  - · Test set degamma shall be linear.
  - · Test set brightness and contrast shall be set to nominal.
  - The diagonal size of the projected image shall be a minimum of 60 inches.
  - The projections screen shall be a 1× gain.
  - The projected image shall be inspected from an 8 foot minimum viewing distance.
  - · The image shall be in focus during all image performance tests.
- (7) Bright pixel definition: a single pixel or mirror that is stuck in the ON position and is visibly brighter than the surrounding pixels.
- (8) Dark pixel definition: a single pixel or mirror that is stuck in the OFF position and is visibly darker than the surrounding pixels.
- (9) POM definition: The rectangular border of off-state mirrors surrounding the active area.
- (10) Gray 10 screen definition: A full screen with RGB values set to R=10/255, G=10/255, B=10/255.
- (11) White screen definition: A full screen with RGB values set to R=255/255, G=255/255, B=255/255.
- (12) Adjacent pixel definition: Two or more stuck pixels sharing a common border or common point. Also referred to as a cluster.
- (13) Unstable pixel definition: A single pixel or mirror that does not operate in sequence with parameters loaded into memory. The unstable pixel appears to be flickering asynchronously with the image.



- A. Pond of micromirrors (POM) omitted for clarity.
- B. Refer to section *Micromirror Array Physical Characteristics* table for M, N, and P specifications.

Figure 5-9. Micromirror Landed Orientation and Tilt



### **5.12 Window Characteristics**

### **Table 5-3. DMD Window Characteristics**

Table V VI DIND TIME OF CHARACTER CO.						
DESCRIPTION	MIN	NOM				
Window material		Corning Eagle XG				
Window refractive index at 546.1 nm		1.5119				
Window transmittance, minimum within the wavelength range 420-680 nm. Applies to all angles 0°-30° AOI. (1) (2)	97%					
Window transmittance, average over the wavelength range 420-680 nm. Applies to all angles 30°-45° AOI.	97%					

<sup>(1)</sup> Single-pass through both surfaces and glass.

## **5.13 Chipset Component Usage Specification**

Reliable function and operation of the DLP470TE DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices used for operating or controlling a DLP DMD.

<sup>(2)</sup> Angle of incidence (AOI) is the angle between an incident ray and the normal to a reflecting or refracting surface.



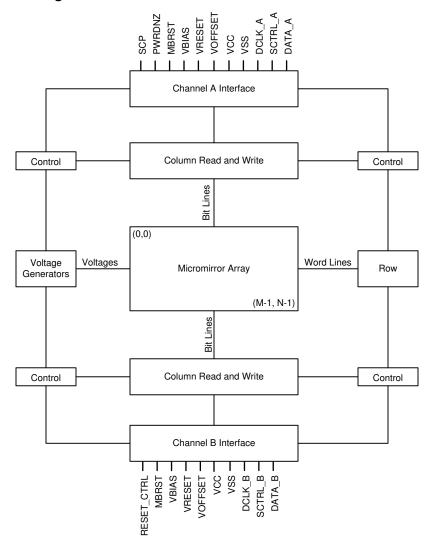
## **6 Detailed Description**

### 6.1 Overview

The DMD is a 0.47-inch diagonal spatial light modulator which consists of an array of highly reflective aluminum micromirrors. The DMD is an electrical input, optical output micro-electrical-mechanical system (MEMS). The electrical interface is low voltage differential signaling (LVDS). The DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of M memory cell columns by N memory cell rows. Refer to the *Functional Block Diagram*. The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

The DLP470TE DMD is part of the chipset that comprises the DLP470TE DMD, the DLPC4420 display controller, and the DLPA100 power and motor driver. To ensure reliable operation, the DLP470TE DMD must always be used with the DLPC4420 display controller and the DLPA100 power and motor driver.

## 6.2 Functional Block Diagram





#### Note

Channels C and D are not shown. For pin details on channels A, B, C, and D, refer to the Pin Configurations and Functions table and the LVDS interface section of Timing Diagrams. RESET CTRL is used in applications when an external reset signal is required.

## **6.3 Feature Description**

#### 6.3.1 Power Interface

The DMD requires five DC voltages: DMD\_P3P3V, DMD\_P1P8V, V<sub>OFFSET</sub>, V<sub>RESET</sub>, and V<sub>BIAS</sub>. DMD\_P3P3V is created by the DLPA100 power and motor driver and is used on the DMD board to create the other four DMD voltages, as well as powering various peripherals (TMP411, I<sup>2</sup>C, and TI level translators). DMD P1P8V is created by the TI PMIC LP38513S and provides the V<sub>CC</sub> voltage required by the DMD. V<sub>OFFSET</sub> (10V), V<sub>RESET</sub> (-14V), and V<sub>BIAS</sub> (18V) are made by the TI PMIC TPS65145 and are supplied to the DMD to control the micromirrors.

#### **6.3.2 Timing**

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. The specifications show an equivalent test load circuit for the output under test. Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. System designers use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

#### 6.4 Device Functional Modes

DMD functional modes are controlled by the DLPC4420 display controller. For more information, see the DLPC4420 Display Controller Data Sheet or contact a TI applications engineer.

## 6.5 Optical Interface and System Image Quality Considerations

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. System optical performance and image quality strongly relate to optical system design parameter trade offs. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

#### 6.5.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area needs to be the same. This angle cannot exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination and projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, contrast degradation, and objectionable artifacts in the display border or active area could occur.

#### 6.5.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display border or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

#### 6.5.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. Design the illumination optical system to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

## **6.6 Micromirror Array Temperature Calculation**

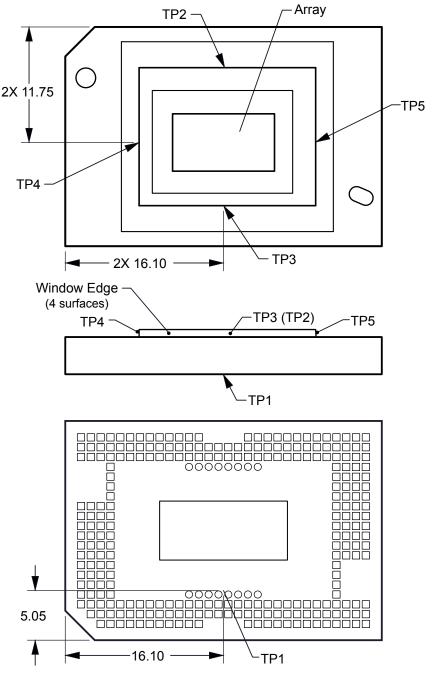


Figure 6-1. DMD Thermal Test Points



Micromirror array temperature cannot be measured directly, therefore it must be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The following equations show the relationship between array temperature and the reference ceramic temperature, thermal test TP1 Figure 6-1 shown above:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY-TO-CERAMIC})$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + (Q_{ILLUMINATION})$$

#### where

- T<sub>ARRAY</sub> = Computed array temperature (°C)
- T<sub>CERAMIC</sub> = Measured ceramic temperature (°C), TP1 Figure 6-1
- R<sub>ARRAY-TO-CERAMIC</sub> = Thermal resistance of package specified in Section 5.5 from array to ceramic TP1 Figure 6-1 (°C/W).
- Q<sub>ARRAY</sub> = Total DMD Power (electrical + absorbed) on array (W).
- Q<sub>ELECTRICAL</sub> = Nominal electrical power (W)
- Q<sub>INCIDENT</sub> = Incident illumination optical power (W)
- Q<sub>ILLIMINATION</sub> = (DMD average thermal absorptivity × Q<sub>INCIDENT</sub> (W)
- DMD average thermal absorptivity = 0.41

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 0.9W. The absorbed optical power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for a single chip or multichip DMD system. It assumes an illumination distribution of 83.7% on the active array and 16.3% on the array border.

The sample calculation for a typical projection application is as follows:

```
Q<sub>INCIDENT</sub> = 31W (measured)
T<sub>CFRAMIC</sub>= 55.0° (measured)
Q<sub>ELECTRICAL</sub> = 0.9W
Q_{ARRAY} = 0.9W + (0.41 \times 31W) = 13.61W
T_{ARRAY} = 55.0°C + (13.61W × 0.90°C/W) = 67.2°C
```

## 6.7 Micromirror Power Density Calculation

The calculation of the optical power density of the illumination on the DMD in the different wavelength bands uses the total measured optical power on the DMD, percent illumination overfill, area of the active array, and the ratio of the spectrum in the wavelength band of interest to the total spectral optical power.

Product Folder Links: DLP470TE

- ILL<sub>UV</sub> = [OP<sub>UV-RATIO</sub> × Q<sub>INCIDENT</sub>] × 1000mW/W ÷ A<sub>ILL</sub> (mW/cm<sup>2</sup>)
- ILL<sub>VIS</sub> = [OP<sub>VIS-RATIO</sub> × Q<sub>INCIDENT</sub>] ÷ A<sub>ILL</sub> (W/cm<sup>2</sup>)
- ILL<sub>IR</sub> =  $[OP_{IR-RATIO} \times Q_{INCIDENT}] \times 1000 \text{mW/W} \div A_{ILL} \text{ (mW/cm}^2)$
- ILL<sub>BLU</sub> =  $[OP_{BLU-RATIO} \times Q_{INCIDENT}] \div A_{ILL} (W/cm^2)$
- ILL<sub>BLU1</sub> = [OP<sub>BLU1-RATIO</sub> × Q<sub>INCIDENT</sub>] ÷ A<sub>ILL</sub> (W/cm<sup>2</sup>)
- $A_{ILL} = A_{ARRAY} \div (1 OV_{ILL}) (cm^2)$

#### where:

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- ILL<sub>UV</sub> = UV illumination power density on the DMD (mW/cm<sup>2</sup>)
- ILL<sub>VIS</sub> = VIS illumination power density on the DMD (W/cm<sup>2</sup>)
- ILL<sub>IR</sub> = IR illumination power density on the DMD (mW/cm<sup>2</sup>)
- ILL<sub>BLU</sub> = BLU illumination power density on the DMD (W/cm<sup>2</sup>)
- ILL<sub>BLU1</sub> = BLU1 illumination power density on the DMD (W/cm<sup>2</sup>)
- A<sub>ILL</sub> = illumination area on the DMD (cm<sup>2</sup>)
- Q<sub>INCIDENT</sub> = total incident optical power on DMD (W) (measured)
- A<sub>ARRAY</sub> = area of the array (cm<sup>2</sup>) (data sheet)
- OV<sub>III</sub> = percent of total illumination on the DMD outside the array (%) (optical model)
- OP<sub>UV-RATIO</sub> = ratio of the optical power for wavelengths <410nm to the total optical power in the illumination spectrum (spectral measurement)
- OP<sub>VIS-RATIO</sub> = ratio of the optical power for wavelengths ≥410 and ≤800nm to the total optical power in the illumination spectrum (spectral measurement)
- OP<sub>IR-RATIO</sub> = ratio of the optical power for wavelengths >800nm to the total optical power in the illumination spectrum (spectral measurement)
- OP<sub>BLU-RATIO</sub> = ratio of the optical power for wavelengths ≥410 and ≤475nm to the total optical power in the illumination spectrum (spectral measurement)
- OP<sub>BLU1-RATIO</sub> = ratio of the optical power for wavelengths ≥410 and ≤440nm to the total optical power in the illumination spectrum (spectral measurement)

The illumination area varies and depends on the illumination overfill. The total illumination area on the DMD is the array area and the overfill area around the array. The optical model is used to determine the percent of the total illumination on the DMD that is outside the array  $(OV_{ILL})$  and the percent of the total illumination that is on the active array. From these values, the illumination area  $(A_{ILL})$  is calculated. The illumination is assumed to be uniform across the entire array.

From the measured illumination spectrum, the ratio of the optical power in the wavelength bands of interest to the total optical power is calculated.

### Sample calculation:

 $\begin{aligned} &Q_{\text{INCIDENT}} = 31\text{W (measured)} \\ &A_{\text{ARRAY}} = (10.3680\text{mm} \times 5.8320\text{mm}) \div 100\text{mm}^2/\text{cm}^2 = 0.6047\text{cm}^2 \text{ (data sheet)} \\ &OV_{\text{ILL}} = 16.3\% \text{ (optical model)} \\ &OP_{\text{UV-RATIO}} = 0.00017 \text{ (spectral measurement)} \\ &OP_{\text{VIS-RATIO}} = 0.99977 \text{ (spectral measurement)} \\ &OP_{\text{IR-RATIO}} = 0.00006 \text{ (spectral measurement)} \\ &OP_{\text{BLU-RATIO}} = 0.28100 \text{ (spectral measurement)} \\ &OP_{\text{BLU1-RATIO}} = 0.03200 \text{ (spectral measurement)} \\ &A_{\text{ILL}} = 0.6047\text{cm}^2 \div (1 - 0.163) = 0.7224\text{cm}^2 \\ &ILL_{\text{LIV}} = [0.00017 \times 31\text{W}] \times 1000\text{mW/W} \div 0.7224\text{cm}^2 = 7.295\text{mW/cm}^2 \end{aligned}$ 

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```
\begin{split} & \text{ILL}_{\text{VIS}} = [0.99977 \times 31\text{W}] \div 0.7224\text{cm}^2 = 42.90\text{W/cm}^2 \\ & \text{ILL}_{\text{IR}} = [0.00006 \times 31\text{W}] \times 1000\text{mW/W} \div 0.7224\text{cm}^2 = 2.575\text{mW/cm}^2 \\ & \text{ILL}_{\text{BLU}} = [0.28100 \times 31\text{W}] \div 0.7224\text{cm}^2 = 12.06\text{W/cm}^2 \\ & \text{ILL}_{\text{BIJJ}} = [0.03200 \times 31\text{W}] \div 0.7224\text{cm}^2 = 1.37\text{W/cm}^2 \end{split}
```

## 6.8 Micromirror Landed-On/Landed-Off Duty Cycle

### 6.8.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

As an example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the ON state 100% of the time (and in the OFF state 0% of the time), whereas 0/100 indicates that the pixel is in the OFF state 100% of the time. Likewise, 50/50 indicates that the pixel is ON for 50% of the time (and OFF for 50% of the time).

Note that when assessing the landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.

### 6.8.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD usable life.

Note that it is the symmetry or asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

#### 6.8.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD temperature and landed duty cycle interact to affect DMD usable life, and this interaction can be exploited to reduce the impact that an asymmetrical landed duty cycle has on the DMD usable life. This is quantified in the de-rating curve shown in Figure 5-1. The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the
  usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the maximum operating DMD temperature at a given long-term average landed duty cycle.

## 6.8.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the landed duty cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel operates under a 100/0 landed duty cycle during that time period. Likewise, when displaying pure-black, the pixel operates under a 0/100 landed duty cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the landed duty cycle tracks one-to-one with the; gray scale value, as shown in Table 6-1.

Table 6-1. Graysc	ale Value and Landed Duty	Cycle
-------------------	---------------------------	-------

GRAYSCALE VALUE	LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, or blue) for the given pixel as well as the color cycle time for each primary color, where "color cycle time" is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

Use this equation to calculate the landed duty cycle of a given pixel during a given time period:

```
Landed Duty Cycle =

(Red_Cycle_% × Red_Scale_Value) +

(Green_Cycle_% × Green_Scale_Value) +

(Blue_Cycle_% × Blue_Scale_Value)
```

#### where

- Red\_Cycle\_% represents the percentage of the frame time that red is displayed to achieve the desired white
  point.
- Green\_Cycle\_% represents the percentage of the frame time that green is displayed to achieve the desired white point.
- Blue\_Cycle\_% represents the percentage of the frame time that blue is displayed to achieve the desired white point.

For example, assume that the red, green, and blue color cycle times are 50%, 20%, and 30% respectively (in order to achieve the desired white point), then the landed duty cycle for various combinations of red, green, and blue color intensities are as shown in Table 6-2 and Table 6-3.

Table 6-2. Example Landed Duty Cycle for Full-Color, Color Percentage

CYCLE PERCENTAGE			
RED	GREEN	BLUE	
50%	20%	30%	

Table 6-3. Example Landed Duty Cycle for Full-Color

rabio o o. Example Lanaca Baty Cycle for fair Color			
SCALE VALUE			LANDED DUTY
RED	GREEN	BLUE	CYCLE
0%	0%	0%	0/100

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Table 6-3. Example Landed Duty Cycle for Full-Color (continued)

(continued)			
SCALE VALUE			LANDED DUTY
RED	GREEN	BLUE	CYCLE
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

## 7 Application and Implementation

#### Note

Information in the following application section is not part of the TI component specifications, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 7.1 Application Information

Texas Instruments DLP® technology is a micro-electro-mechanical systems (MEMS) technology that modulates light using a digital micromirror device (DMD). The DMD is a spatial light modulator, which reflects incoming light from an illumination source in one of two directions, towards the projection optics or collection optics. The new TRP pixel with a higher tilt angle increases brightness performance and enables smaller system electronics for size-constrained applications. Typical applications using the DLP470NE include home theater, digital signage, interactive displays, low-latency gaming displays, and portable smart displays.

The most recent class of chipsets from Texas Instruments is based on a breakthrough micromirror technology called TRP. With a smaller pixel pitch of  $5.4~\mu m$  and increased tilt angle of 17 degrees, TRP chipsets enable higher resolution in a smaller form factor and enhanced image processing features while maintaining high optical efficiency. DLP® chipsets are a great fit for any system that requires high resolution and high brightness displays. The following orderables have been replaced by the DLP470TE.

#### **Device Information**

PART NUMBER	PACKAGE	PACKAGE SIZE	Mechanical ICD
1910-5532B	FXJ (257)	32.2mm × 22.3mm	2516207
1910-5537B	FXJ (257)	32.2mm × 22.3mm	2516207
1910-553AB	FXJ (257)	32.2mm × 22.3mm	2516207

## 7.2 Typical Application

The DLP470TE DMD combined with two DLPC4420 display controllers, an FPGA, a power management device DLPA100, and other electrical, optical, and mechanical components, enables bright, affordable, full 4K UHD display solutions. Figure 7-1 shows a typical 4K UHD system application using the DLP470TE DMD.

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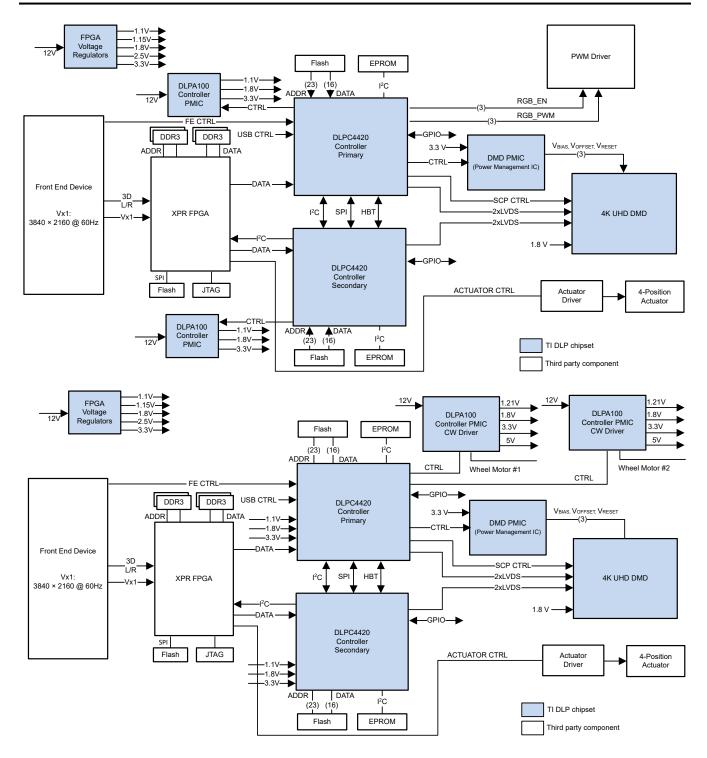


Figure 7-1. Typical DLPC4420 4K UHD Application (LED, Top; LPCW, Bottom)

### 7.2.1 Design Requirements

A DLP470TE projection system is created by using the DMD chipset, including the DLP470TE digital micromirror device (DMD), the DLPC4420 controller, and the DLPA100 power management and motor driver. The DLP470TE is used as the core imaging device in the display system and contains a 0.47-inch array of micromirrors. The DLPC4420 controller is the digital interface between the DMD and the rest of the system,

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taking digital input from a front-end receiver and driving the DMD over a high-speed interface. The DLPA100 power management device provides voltage regulators for the DMD, controller, and illumination functionality.

Other core components of the display system include an FPGA, illumination source, an optical engine for the illumination and projection optics, other electrical and mechanical components, and software. The illumination source options include lamp, LED, laser, or laser phosphor. The type of illumination used and desired brightness will have a major effect on the overall system design and size.

### 7.2.2 Detailed Design Procedure

For a complete DLP® system, an optical module or light engine is required that contains the DLP470TE DMD, associated illumination sources, optical elements, and necessary mechanical components.

To ensure reliable operation, the DLP470TE DMD must always be used with the DLPC4420 display controller and the DLPA100 PMIC driver. Refer to the PCB design requirements to see DLP standard TRP digital micromirror devices for the DMD board design and manufacturer handling of the DMD subassemblies.

### 7.2.3 Application Curves

When LED illumination is utilized, the typical LED-current-to-luminance relationship is shown in Figure 7-2.

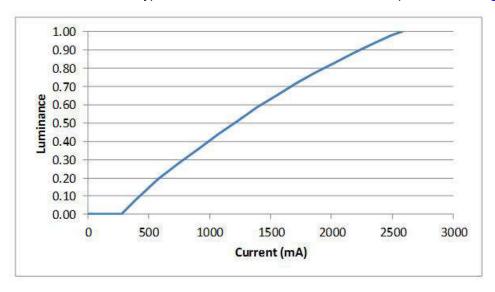


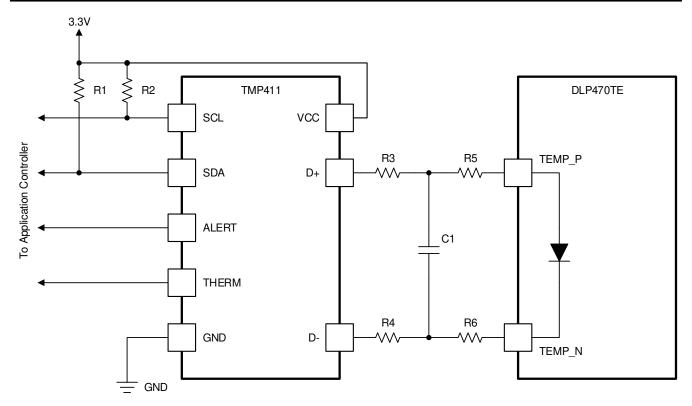
Figure 7-2. Luminance vs. Current

### 7.3 DMD Die Temperature Sensing

The DMD features a built-in thermal diode that measures the temperature at one corner of the die outside the micromirror array. The thermal diode can be interfaced with the TMP411 temperature sensor as shown in Figure 7-3. The serial bus from the TMP411 can be connected to the DLPC4420 display controller to enable its temperature sensing features. Contact TI for the *DLPC4420 Programmers' Guide* for instructions on installing the DLPC4420 controller support firmware bundle and obtaining the temperature readings.

The software application contains functions to configure the TMP411 to read the DMD temperature sensor diode. This data can be leveraged to incorporate additional functionality in the overall system design such as adjusting illumination, fan speeds, and so forth. All communication between the TMP411 and the DLPC4420 controller will be completed using the I<sup>2</sup>C interface. The TMP411 connects to the DMD via pins B17 and B18 as outlined in *Pin Configuration and Functions*.





- A. Details omitted for clarity, see the TI Reference Design for connections to the DLPC4420 controller.
- B. See the TMP411 data sheet for system board layout recommendation.
- C. See the TMP411 data sheet and the TI reference design for suggested component values for R1, R2, R3, R4, and C1.
- D. R5 =  $0\Omega$ . R6 =  $0\Omega$ . Zero ohm resistors need to be located close to the DMD package pins.

Figure 7-3. TMP411 Sample Schematic

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## 8 Power Supply Recommendations

The following power supplies are all required to operate the DMD:

- V<sub>SS</sub>
- V<sub>BIAS</sub>
- V<sub>CC</sub>
- V<sub>OFFSET</sub>
- V<sub>RESET</sub>

DMD power-up and power-down sequencing is strictly controlled by the ®DLP display controller.

#### CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to any of the prescribed power-up and power-down requirements may affect device reliability. See Figure 8-1.

 $V_{BIAS}$ ,  $V_{CC}$ ,  $V_{OFFSET}$ , and  $V_{RESET}$  power supplies must be coordinated during power-up and power-down operations. Failure to meet any of the below requirements will result in a significant reduction in the DMD reliability and lifetime. Common ground  $V_{SS}$  must also be connected.

## 8.1 DMD Power Supply Power-Up Procedure

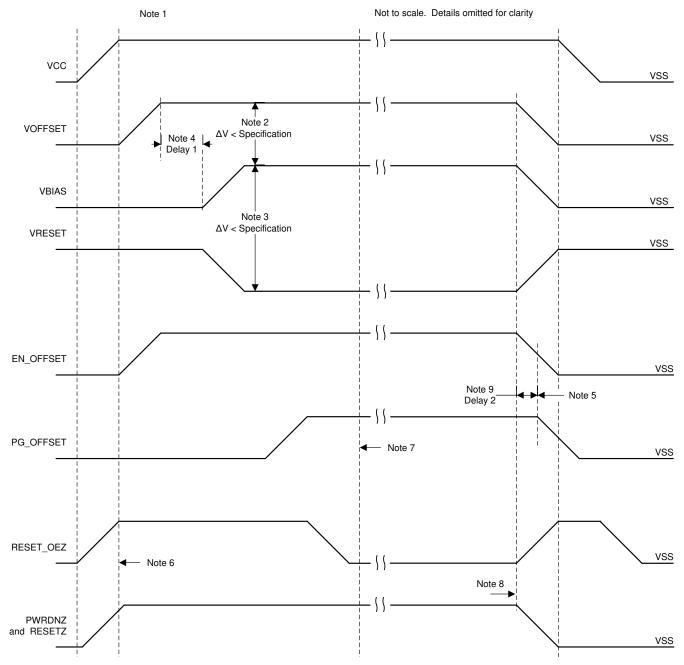
- During power-up, V<sub>CC</sub> must always start and settle before V<sub>OFFSET</sub> plus Delay1 specified in Table 8-1, V<sub>BIAS</sub>, and V<sub>RESET</sub> voltages are applied to the DMD.
- During power-up, it is a strict requirement that the voltage difference between V<sub>BIAS</sub> and V<sub>OFFSET</sub> must be within the specified limit shown in *Recommended Operating Conditions*.
- During power-up, there is no requirement for the relative timing of V<sub>RESET</sub> with respect to V<sub>BIAS</sub>.
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements specified in the Absolute Maximum Ratings, in the Recommended Operating Conditions, and in Figure 8-1.
- During power-up, LVCMOS input pins must not be driven high until after V<sub>CC</sub> have settled at operating voltages listed in the Recommended Operating Conditions.

### 8.2 DMD Power Supply Power-Down Procedure

- During power-down, V<sub>CC</sub> must be supplied until after V<sub>BIAS</sub>, V<sub>RESET</sub>, and V<sub>OFFSET</sub> are discharged to within the specified limit of ground. See Table 8-1.
- During power-down, it is a strict requirement that the voltage difference between V<sub>BIAS</sub> and V<sub>OFFSET</sub> must be within the specified limit shown in the *Recommended Operating Conditions*.
- During power-down, there is no requirement for the relative timing of V<sub>RESET</sub> with respect to V<sub>BIAS</sub>.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements specified in the Absolute Maximum Ratings, in the Recommended Operating Conditions, and in Figure 8-1.
- During power-down, LVCMOS input pins must be less than specified in the *Recommended Operating Conditions*.

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- A. See Recommended Operating Conditions, and the Pin Functions table.
- B. To prevent excess current, the supply voltage difference |V<sub>OFFSET</sub> V<sub>BIAS</sub>| must be less than the specified limit in the *Recommended Operating Conditions*
- C. To prevent excess current, the supply difference |V<sub>BIAS</sub> V<sub>RESET</sub>| must be less than the specified limit in the *Recommended Operating Conditions*.
- D. V<sub>BIAS</sub> must power up after V<sub>OFFSET</sub> has powered up, per the Delay1 specification in Table 8-1
- E. PG OFFSET must turn off after EN OFFSET has turned off, per the Delay2 specification in Table 8-1.
- F. \*\*DLP controller software enables the DMD power supplies V<sub>BIAS</sub>, V<sub>RESET</sub>, V<sub>OFFSET</sub> with V<sub>CC</sub> active after RESET\_OEZ is at logic high.
- G. ®DLP controller software initiates the global V<sub>BIAS</sub> command.
- H. After the DMD micromirror park sequence is complete, the  $^{@}$ DLP controller software initiates a hardware power-down that activates PWRDNZ and disables  $V_{BIAS}$ ,  $V_{RESET}$ , and  $V_{OFFSET}$ .

Under power-loss conditions where emergency DMD micromirror park procedures are being enacted by the ®DLP controller hardware, EN\_OFFSET may turn off after PG\_OFFSET has turned off. The OEZ signal goes high prior to PG\_OFFSET turning off to indicate the DMD micromirror has completed the emergency park procedures.

## Figure 8-1. DMD Power Supply Requirements

## **Table 8-1. DMD Power-Supply Requirements**

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
Delay1	Delay from $V_{\text{OFFSET}}$ settled at recommended operating voltage to $V_{\text{BIAS}}$ and $V_{\text{RESET}}$ power up	1	2		ms
Delay2	PG_OFFSET hold time after EN_OFFSET goes low	100			ns

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## 9 Layout

## 9.1 Layout Guidelines

The DLP470TE DMD is part of a chipset that is controlled by the DLPC4420 display controller in conjunction with the DLPA100 power and motor driver. These guidelines are targeted to help design a PCB board with the DLP470TE DMD. The DLP470TE DMD board is a high-speed multilayer PCB, with primarily high-speed digital logic using dual-edge clock rates up to 400MHz for DMD LVDS signals. The remaining traces are comprised of low-speed digital LVTTL signals. TI recommends that mini power planes are used for VOFFSET, VRESET, and VBIAS. Solid planes are required for DMD\_P3P3V(3.3V), DMD\_P1P8V, and Ground. The target impedance for the PCB is  $50\Omega \pm 10\%$  with the LVDS traces being  $100\Omega \pm 10\%$  differential. TI recommends using an 8-layer stack-up, as described in Table 9-1.

## 9.2 Layout Example

## 9.2.1 Layers

The layer stack-up and copper weight for each layer is shown in Table 9-1. Small subplanes are allowed on signal routing layers to connect components to major subplanes on top/bottom layers if necessary.

Table 5 1. Eayer Stack Sp								
LAYER NO.	LAYER NAME	COPPER WT. (oz.)	COMMENTS					
1	Side A - DMD only	1.5	DMD, escapes, low-frequency signals, power subplanes					
2	Ground	1	Solid ground plane (net GND)					
3	Signal	0.5	$50\Omega$ and $100\Omega$ differential signals					
4	Ground	1	Solid ground plane (net GND)					
5	DMD_P3P3V	1	+3.3V power plane (net DMD_P3P3V)					
6	Signal	0.5	$50\Omega$ and $100\Omega$ differential signals					
7	Ground	1	Solid ground plane (net GND)					
8	Side B - All other Components	1.5	Discrete components, low-frequency signals, power subplanes					

Table 9-1. Layer Stack-Up

### 9.2.2 Impedance Requirements

TI recommends that the board has matched impedance of  $50\Omega \pm 10\%$  for all signals. The exceptions are listed in Table 9-2.

Table 9-2. Special impedance Requirements						
Signal Type	Signal Name	Impedance (ohms)				
	D_AP(0:15), D_AN(0:15)					
A channel LVDS differential pairs	DCLKA_P, DCLKA_N	100 ±10% differential across each				
	SCTRL_AP, SCTRL_AN	- Pa				
	D_BP(0:15), D_BN(0:15)					
B channel LVDS differential pairs	DCLKB_P, DCLKB_N	100 ±10% differential across eac				
	SCTRL_BP, SCTRL_BN	- pan				
	D_CP(0:15), D_CN(0:15)					
C channel LVDS differential pairs	DCLKC_P, DCLKC_N	100 ±10% differential across each				
	SCTRL_CP, SCTRL_CN	- Pa				
	D_DP(0:15), D_DN(0:15)					
D channel LVDS differential pairs	DCLKD_P, DCLKD_N	100 ±10% differential across each pair				
	SCTRL_DP, SCTRL_DN					

Table 9-2. Special Impedance Requirements

Product Folder Links: DLP470TE



## 9.2.3 Trace Width, Spacing

Unless otherwise specified, TI recommends that all signals follow the 0.005-inch/0.005-inch design rule. Minimum trace clearance from the ground ring around the PWB has a 0.1-inch minimum. An analysis of impedance and stack-up requirements determine the actual trace widths and clearances.

### 9.2.3.1 Voltage Signals

**Table 9-3. Special Trace Widths, Spacing Requirements** 

SIGNAL NAME	MINIMUM TRACE WIDTH TO PINS (MIL)	LAYOUT REQUIREMENT			
GND	15	Maximize trace width to connecting pin			
DMD_P3P3V	15	Maximize trace width to connecting pin			
DMD_P1P8V	15	Maximize trace width to connecting pin			
VOFFSET	15	Create mini plane from U2 to U3			
VRESET	15	Create mini plane from U2 to U3			
VBIAS	15	Create mini plane from U2 to U3			
All U3 control connections	10	Use 10 mil etch to connect all signals/voltages to DMD pads			



## 10 Device and Documentation Support

## 10.1 Device Support

#### 10.1.1 Device Nomenclature

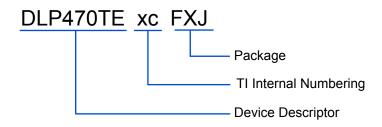


Figure 10-1. Part Number Description

#### 10.1.2 Device Markings

The device marking includes both human-readable information and a 2-dimensional matrix code. The human-readable information is described in Figure 10-2. The 2-dimensional matrix code is an alpha-numeric character string that contains the DMD part number, part 1 of the serial number, and part 2 of the serial number.

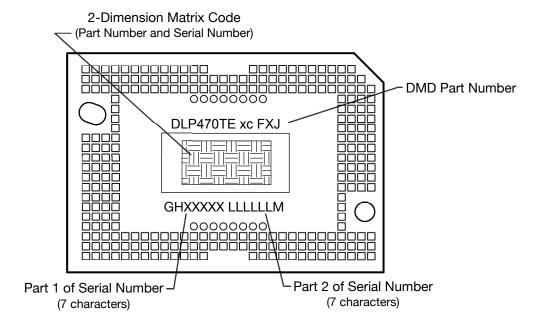


Figure 10-2. DMD Marking Locations

### 10.2 Third-Party Products Disclaimer

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Product Folder Links: *DLP470TE* 

### 10.3 Documentation Support

#### 10.3.1 Related Documentation

The following documents contain additional information related to the chipset components used with the DLP470TE.

- DLPC4420 Display Controller Data Sheet
- DLPA100 Power Management and Motor Driver Data Sheet

### 10.3.2 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### 10.3.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.4 Trademarks

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#### 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 10.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

### 11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

С	hanges from Revision B (September 2022) to Revision C (January 2025)	Page
•	Added links to DLP Products third-party search tools, and Getting Started With TI DLP Display Technology	ogy 1
•	Updated section Recommended Operating Conditions	11
•	Updated Micromirror Array Optical Characteristics Table	
•	Updated Micromirror Array Temperature Calculation	25

С	hanges from Revision A (June 2022) to Revision B (September 2022)	Page
•	Changed the controller to DLPC4420, linked the chipset components to product pages	1
•	Changed the controller to DLPC4420, updated the application diagram	1
•	Changed the controller to DLPC4420, added the lamp illumination section	11
•	Added the DMD efficiency specification	20
•	Changed the controller to DLPC4420	23
	Changed the controller to DLPC4420	
	Changed the controller to DLPC4420, added a table with legacy part numbers and mechanical ICD	

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## **DLP470TE**

## DLPS161C - APRIL 2019 - REVISED JANUARY 2025



•	Changed the controller to DLPC4420, updated the application diagrams	31
	Changed the controller to DLPC4420	
	Changed the controller to DLPC4420	
	Changed the controller to DLPC4420	
	Changed the controller to DLPC4420	
	Changed the controller to DLPC4420, updated the link	
	1	

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# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
DLP470TEAAFXJ	Active	Production	CLGA (FXJ)   257	33   JEDEC TRAY (5+1)	Yes	Call TI	N/A for Pkg Type	0 to 70	
DLP470TEAAFXJ.B	Active	Production	CLGA (FXJ)   257	33   JEDEC TRAY (5+1)	Yes	Call TI	N/A for Pkg Type	0 to 70	

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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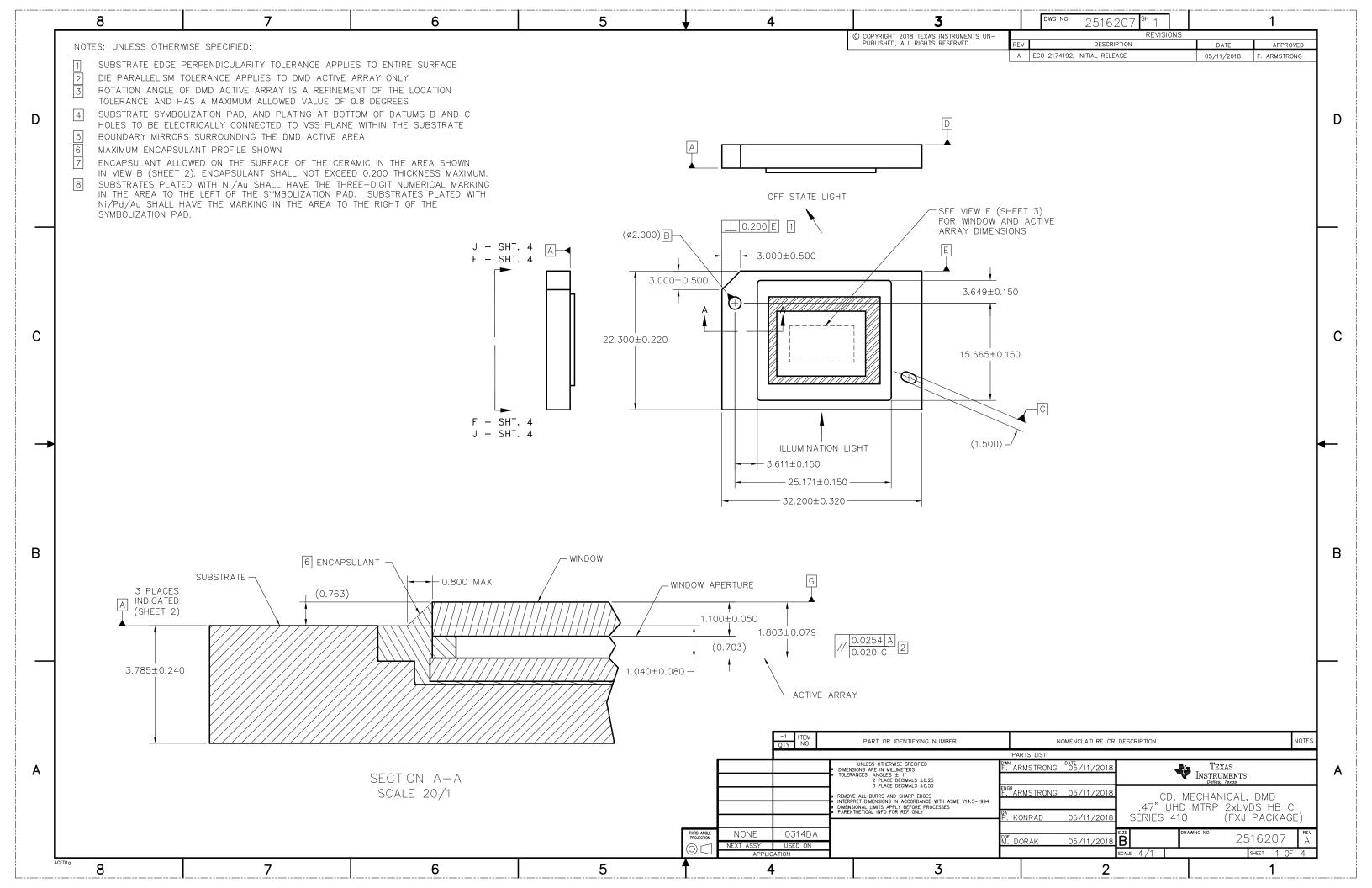
<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

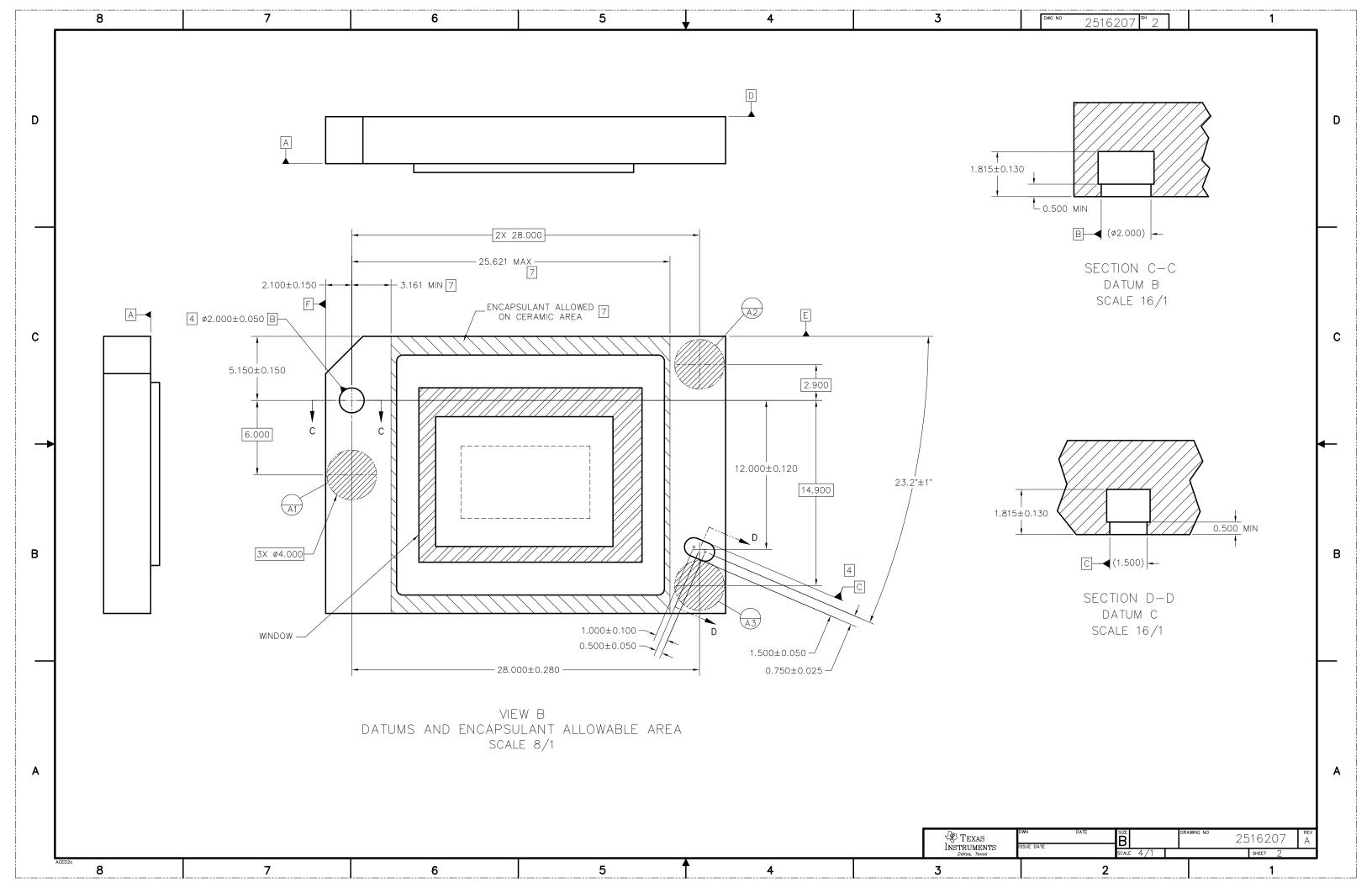
<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

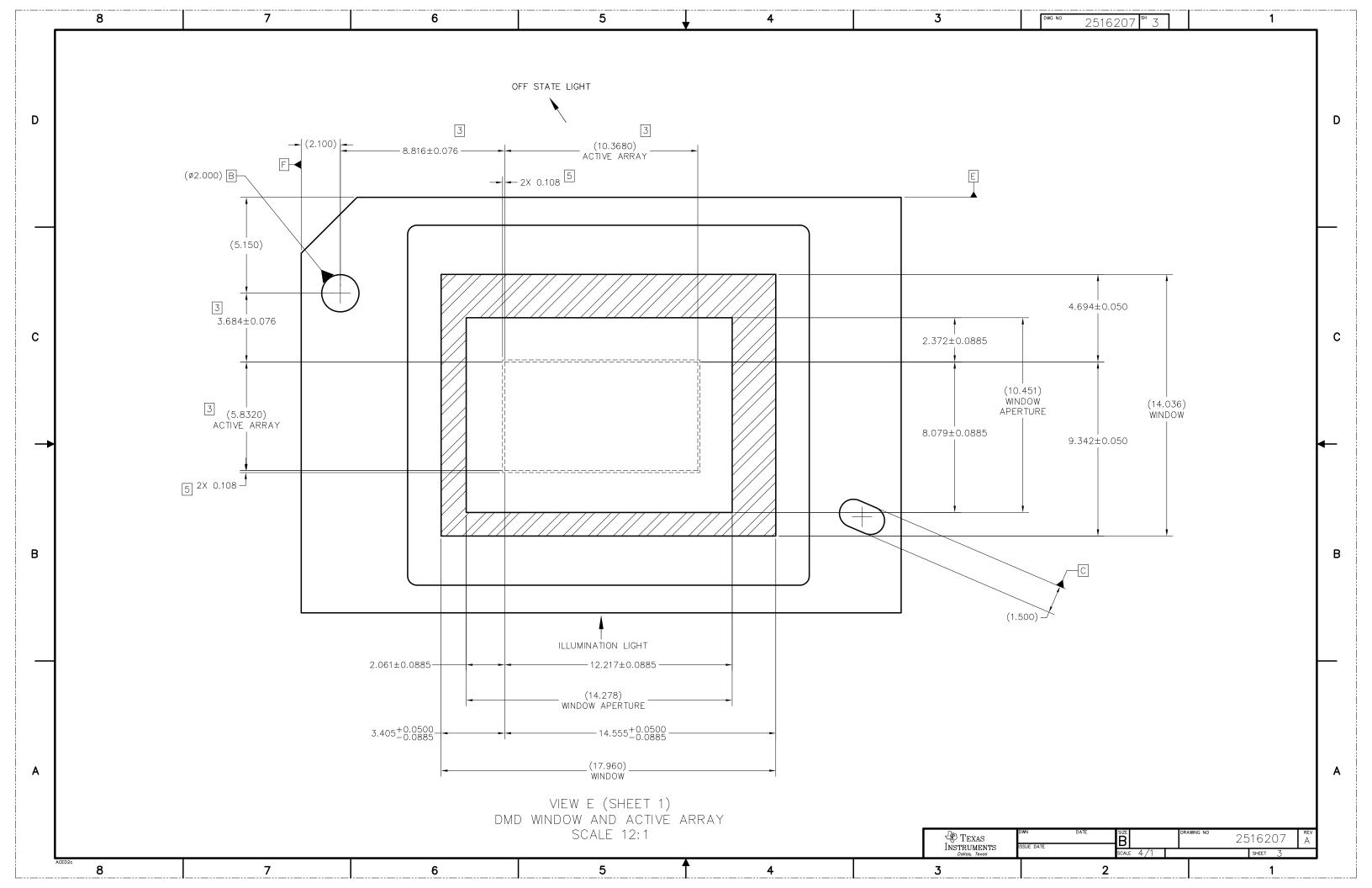
<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

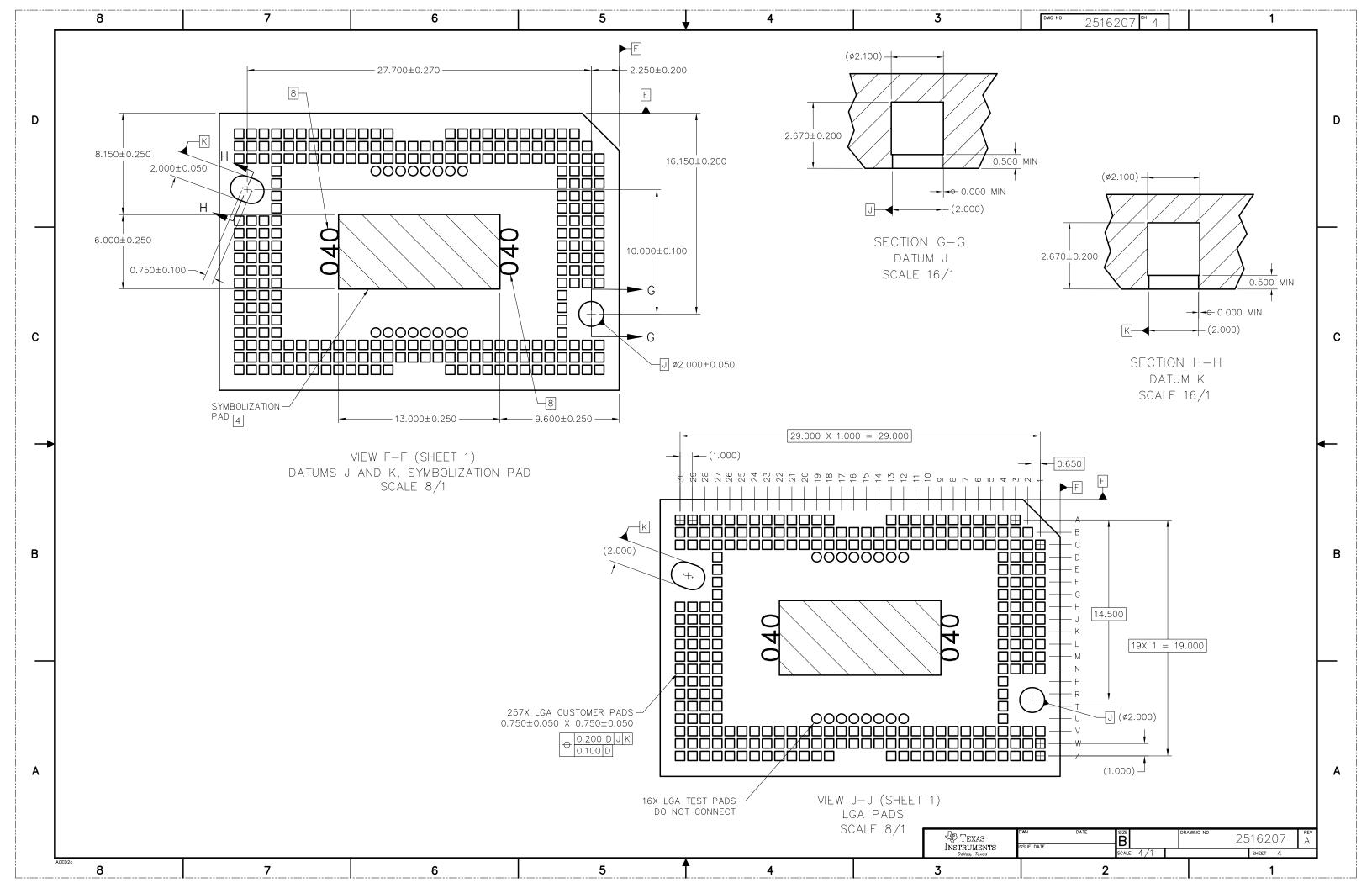
<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.









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