











DLP3034-Q1

DLPS176A - APRIL 2019-REVISED SEPTEMBER 2019

# DLP3034-Q1 0.3-Inch WVGA 405-nm DMD for Automotive Display

#### 1 Features

- Automotive qualified
  - 40°C to 105°C operating temperature range for DMD array
- Supports 405-nm illumination sources
- 0.3-inch diagonal micromirror array
  - 7.6-µm micromirror pitch
  - ±12° micromirror tilt angle (relative to flat state)
  - Side illumination for optimized efficiency
- WVGA (864 × 480) resolution
- Polarization independent spatial light modulator
  - Compatible with LED or laser light sources
- Low-power consumption: 105-mW (typical)
- Operating temperature range: –40°C to 105°C
- Hermetic package with 2.5°C/W thermal efficiency
- JTAG boundary scan to allow in-system validation
- Compatible with the DLPC120-Q1 automotive DMD controller
- 78-MHz DDR DMD interface

### 2 Applications

Transparent window display for front, side, and rear vehicle windows

## 3 Description

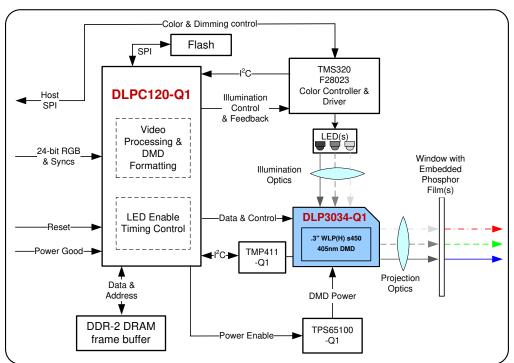
The DLP3034-Q1 automotive DMD is primarily targeted for transparent window display applications. This chipset can be coupled with 405-nm illumination sources (e.g. LEDs or lasers) in an optical projection system to project onto windows embedded with emissive phosphor films. When these transparent emissive films are excited with 405-nm light from a DLP3034-Q1 projector, the window becomes a display emitting light in the visible spectrum. In addition, this chipset enables high power optical systems with a wide dynamic range and fast switching speeds that do not vary with temperature.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLP3034-Q1	FYJ (149)	22.30 mm × 32.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

# DLP® DLP3034-Q1 Block System Diagram





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## 4 Revision History

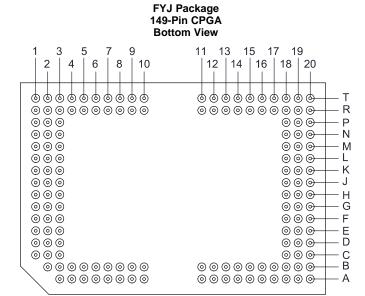
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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# 5 Pin Configuration and Functions



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# **Pin Configurations and Functions**

Pin Configurations and Functions					
PIN		I/O	DESCRIPTION	TRACE, mm <sup>(1)</sup>	
NAME	NO.	1/0	DECOKII NON	TICAOL, IIIII	
DATA(0)	F18				
DATA(1)	F20				
DATA(2)	G20				
DATA(3)	G19				
DATA(4)	H19				
DATA(5)	G18				
DATA(6)	J20		Data bus. Synahranaya ta riging adge and falling adge.		
DATA(7)	H20		Data bus. Synchronous to rising edge and falling edge of DCLK.	8.059	
DATA(8)	J19			0.000	
DATA(9)	K18				
DATA(10)	K19				
DATA(11)	L20				
DATA(12)	L18				
DATA(13)	K20				
DATA(14)	M18				
DCLK	N18	LVCMOS input	Data clock.		
LOADB	M20		Parallel latch load enable. Synchronous to rising edge and falling edge of DCLK.	10.939	
SCTRL	N19		Serial control (sync). Synchronous to rising edge and falling edge of DCLK.	6.596	
TRC	M19		Toggle rate control. Synchronous to rising edge and falling edge of DCLK.	8.617	
DAD_BUS	A7		Reset control serial bus. Synchronous to rising edge of SAC_CLK.	10.413	
RESET_OEZ	A5		Active low. Output enable signal for internal reset driver circuitry.	13.37	
RESET_STROBE	A10		Rising edge on RESET_STROBE latches in the control signals.	13.329	
SAC_BUS	В9		Stepped address control serial bus. Synchronous to rising edge of SAC_CLK.	12.586	
SAC_CLK	A8		Stepped address control clock.	12.668	
TCK	M2		JTAG clock.	10.489	
TDI	N3		JTAG data input. Synchronous to rising edge of TCK. Bond pad connects to internal pull up resistor.	11.04	
TDO	M3	LVCMOS output	JTAG data output. Synchronous to falling edge of TCK. Tri-state failsafe output buffer.	10.067	
TMS	R5	LVCMOS input	JTAG mode select. Synchronous to rising edge of TCK. Bond pad connects to internal pull up resistor.	10.413	
TEMP_MINUS	T10	Analog Innut	Calibrated temperature diode used to assist accurate	N/A	
TEMP_PLUS	T11	Analog Input	temperature measurements of DMD die.	N/A	
No Connect (Unused)	A3, A18, A19, A20, B2, B10, B18, B19, B20, C1, C20, D18, D19, D20, E18, E19, E20, N20, P20, R18, R19, R20, T18, T19, T20	N/A	N/A	N/A	

(1) Propagation delay is 10.24 ps/mm for the DMD Series 450 ceramic package trace lengths.



# Pin Configurations and Functions (continued)

PIN				(1)
NAME	NO.	I/O	DESCRIPTION	TRACE, mm <sup>(1)</sup>
V <sub>BIAS</sub> <sup>(2)</sup>	F3, K3, L3		Power supply for positive bias level of mirror reset signal.	N/A
V <sub>CC</sub> <sup>(2)</sup>	A9, A12, A14, A16, B13, B16, R12, R13, R16, R17, T13, T14, T16	Power	Power supply for low voltage CMOS logic. Power supply for normal high voltage at mirror address electrodes. Power supply for offset level of mirror reset signal during power down.	N/A
V <sub>CCH</sub>	P3, R3, T3, T4, T5, T6	Connect to GND	Reserved pin.	N/A
V <sub>OFFSET</sub> <sup>(2)</sup>	D1, E1, M1, N1		Power supply for high voltage CMOS logic. Power supply for stepped high voltage at mirror address electrodes. Power supply for offset level of mirror reset signal.	N/A
V <sub>REF</sub> <sup>(2)</sup>	B11, B12		Power supply for low voltage CMOS DDR interface.	N/A
V <sub>RESET</sub> <sup>(2)</sup>	B3, C3, E3		Power supply for negative reset level of mirror reset signal.	N/A
Vss <sup>(2)</sup>	A6, A11, A13, A15, A17, B4, B5, B8, B14, B15, B17, C2, C18, C19, F1, F2, F19, H1, H2, H3, H18, J18, K1, K2, L19, N2, P18, P19, R4, R14, R15, T7, T9, T12, T15, T17	Power	Common return for all power.	N/A
V <sub>SSH</sub>	P1, P2, R1, R2, T1, T2	Connect to GND	Reserved pin.	N/A
RESERVED_BIM	Т8			N/A
RESERVED_DT	R7	Connect to GND	Bond pad connects to internal pull down resistor.	N/A
RESERVED_RM	E2			N/A
RESERVED_R(0)	G1			N/A
RESERVED_R(1)	G2			N/A
RESERVED_R(2)	G3			N/A
RESERVED_R(3)	J1	Do not connect	Bond pad connects to 250k pull down resistor.	N/A
RESERVED_R(4)	J2	Do not connect	Manufacturing test.	N/A
RESERVED_R(5)	J3			N/A
RESERVED_R(6)	L1			N/A
RESERVED_R(7)	L2			N/A
RESERVED_PFE	R6			N/A
RESERVED_RA(0)	B6			N/A
RESERVED_RA(1)	D3	Connect to CND	Rond and connects to internal pull down register	N/A
RESERVED_RA(2)	В7	Connect to GND	Bond pad connects to internal pull down resistor.	N/A
RESERVED_RS(0)	A4			N/A
RESERVED_RS(1)	D2			N/A
RESERVED_SO	R9	Do not connect	Tri-state failsafe output buffer.	N/A
RESERVED_TP(0)	R8			N/A
RESERVED_TP(1)	R10	Connect to GND	Manufacturing test.	N/A
RESERVED_TP(2)	R11			N/A

<sup>(2)</sup> The following power supplies are required to operate the DMD:  $V_{BIAS}$ ,  $V_{CC}$ ,  $V_{OFFSET}$ ,  $V_{RESET}$ ,  $V_{SS}$ .

Product Folder Links: DLP3034-Q1

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### **Specifications**

### 6.1 Absolute Maximum Ratings

See (1)

		MIN	MAX	UNIT
SUPPLY VOLTAGE				
$V_{REF}$	LVCMOS logic supply voltage <sup>(2)</sup>	-0.5	4	V
V <sub>CC</sub>	LVCMOS logic supply voltage <sup>(2)</sup>	-0.5	4	V
V <sub>OFFSET</sub>	Mirror electrode and HVCMOS voltage (2)	-0.5	8.75	V
V <sub>BIAS</sub>	Mirror electrode voltage	-0.5	17	V
V <sub>BIAS</sub> - V <sub>OFFSET</sub>	Supply voltage delta <sup>(3)</sup>		8.75	V
V <sub>RESET</sub>	Mirror electrode voltage	-11	0.5	V
Input voltage: other Inputs	See (2)	-0.5	V <sub>REF</sub> + 0.3	V
f <sub>DCLK</sub>	Clock frequency	60	80	MHz
I <sub>TEMP_DIODE</sub>	Temperature diode current		500	μΑ
ENVIRONMENTAL				
T <sub>ARRAY</sub>	Operating DMD array temperature (4)	-40	105	°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Unless otherwise indicated, these are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

### 6.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system.

		MIN	MAX	UNIT
$T_{DMD}$	DMD storage temperature	-40	125	°C

### 6.3 ESD Ratings<sup>(1)</sup>

				VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (2)		±2000		
	Charmed devices model (CDM), man JECD22 C404 (3)	All pins	±500	V	
	Charged-device model (CDM), per JESD22-C101 (3)	Corner pins	±750		

All CMOS devices require proper electrostatic discharge (ESD) handling procedures.

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All voltage values are with respect to GND ( $V_{SS}$ ).  $V_{BIAS}$ ,  $V_{CC}$ ,  $V_{OFFSET}$ ,  $V_{REF}$ ,  $V_{RESET}$ , and  $V_{SS}$  are required to operate the DMD. To prevent excess current, the supply voltage delta  $|V_{BIAS} - V_{OFFSET}|$  must be less than or equal to 8.75 V.

See Micromirror Array Temperature Calculation section.

JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



## 6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

	e-air temperature range (uniess otherwise noted)		MIN	NOM	MAX	UNIT
SUPPLY VOLTAGE	RANGE	1				
V <sub>REF</sub>	LVCMOS interface power supply voltage (1)		1.65	1.8	1.95	V
V <sub>CC</sub>	LVCMOS logic power supply voltage <sup>(1)</sup>		2.25	2.5	2.75	V
V <sub>OFFSET</sub>	Mirror electrode and HVCMOS voltage <sup>(1)</sup>		8.25	8.5	8.75	V
V <sub>BIAS</sub>	Mirror electrode voltage		15.5	16	16.5	V
V <sub>BIAS</sub> - V <sub>OFFSET</sub>	Supply voltage delta <sup>(2)</sup>				8.75	V
V <sub>RESET</sub>	Mirror electrode voltage		-9.5	-10	-10.5	V
V <sub>P</sub> VT+	Positive going threshold voltage		0.4 × V <sub>REF</sub>		0.7 × V <sub>REF</sub>	V
V <sub>N</sub> VT-	Negative going threshold voltage		0.3 <b>x</b> V <sub>REF</sub>		0.6 × V <sub>REF</sub>	V
V <sub>H</sub> ΔVT	Hysteresis voltage (Vp – Vn)		0.1 × V <sub>REF</sub>		0.4 × V <sub>REF</sub>	V
I <sub>OH_TDO</sub>			-2	mA		
I <sub>OL_TDO</sub>	Low level output current @ Vol = 0.4 V, TDO, Vcc :	= 2.25 V			2	mA
TEMPERATURE DI	ODE					
I <sub>TEMP_DIODE</sub>	Max current source into temperature diode (3)				120	μΑ
ENVIRONMENTAL						
T <sub>ARRAY</sub>	Operating DMD array temperature (4)		-40		105	°C
ILL <sub>sub-385nm</sub>	Illumination, wavelength < 385 nm				2.0	mW/cm <sup>2</sup>
ILL <sub>385-to-395nm</sub>	Illumination, 385 nm < wavelength < 395 nm				250	mW/cm <sup>2</sup>
ILL <sub>395-to-400nm</sub>	Illumination, 395 nm < wavelength < 400 nm		800		800	mW/cm <sup>2</sup>
ILL <sub>400-to-420nmnm</sub>	Illumination, 400 nm < wavelength < 420 nm	mination, 400 nm < wavelength < 420 nm 8.0		W/cm <sup>2</sup>		
ILL <sub>VIS</sub>	Illumination, 420 nm < wavelength < 800 nm			Therma	Ily limited <sup>(5)</sup>	W/cm <sup>2</sup>
11.1	Illumination overfill maximum heat load in areas shown in Figure 1 $^{(6)}$	T <sub>ARRAY</sub> ≤ 75°C			26	mW/mm <sup>2</sup>
ILL <sub>OVERFILL</sub>	Illumination overfill maximum heat load in areas shown in Figure 1 (6)	T <sub>ARRAY</sub> > 75°C			20	mW/mm <sup>2</sup>

- $V_{BIAS}$ ,  $V_{CC}$ ,  $V_{OFFSET}$ ,  $V_{REF}$ ,  $V_{RESET}$ ,  $V_{SS}$  are required to operate the DMD. To prevent excess current, the supply voltage delta  $|V_{BIAS} V_{OFFSET}|$  must be less than or equal to 8.75 V. Temperature Diode is to allow accurate measurement of the DMD array temperature during operation.
- DMD active array temperature can be calculated as shown in *Micromirror Array Temperature Calculation* section. Additionally, the DMD array temperature is monitored in the system using the TMP411-Q1 and DLPC120-Q1 as shown in the system block diagram.
- Limited by the resulting micromirror array temperature. Refer to the calculation example in Micromirror Array Temperature Calculation section.
- The active area of the DLP303x-Q1 device is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area outside the active array can scatter and create adverse effects to the performance of an end application using the DMD. The illumination optical system should be designed to minimize light flux incident outside the active array. Depending on the particular system's optical architecture and assembly tolerances, the amount of overfill light on the outside of the active array may cause system performance degradation.



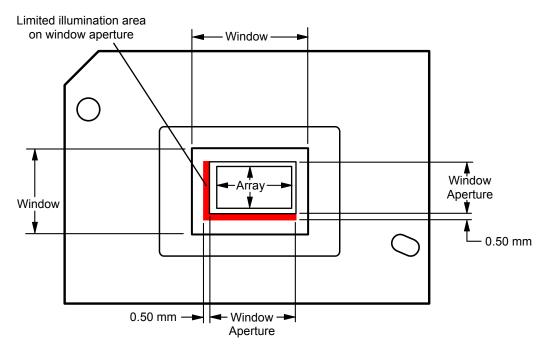


Figure 1. Illumination Overfill Diagram



#### 6.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DLP3034-Q1	
		FYJ (CPGA)	UNIT
		149 PINS	
Thermal resistance	Active area to test point 1 (TP1) <sup>(1)</sup>	2.5	°C/W

<sup>(1)</sup> The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the *Recommended Operating Conditions*. The total heat load on the DMD is largely driven by the incident light absorbed by the active area, although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

#### 6.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)(1)

	PARAMETER	TEST CONDITIONS (2)	MIN	TYP	MAX	UNIT
V	High level output voltage	VCC = 2.25 V	1.7			V
V <sub>OH</sub>	nigit level output voltage	$I_{OH} = -8 \text{ mA}$	1.7			V
V	Himb laval autout valta aa (3)	VREF = 1.8 V	4.44			17
V <sub>OH2</sub>	High level output voltage (3)	$I_{OH} = -2 \text{ mA}$	1.44			V
\/	Law lawal autout valta as	VCC = 2.75 V			0.4	V
V <sub>OL</sub>	Low level output voltage	$I_{OL} = 8 \text{ mA}$			0.4	V
M	1 1 (3)	VREF = 1.8 V			0.00	٧
V <sub>OL2</sub>	Low level output voltage (3)	$I_{OL} = 2 \text{ mA}$			0.36	V
		VREF = 1.95 V	-10			
	Output high importance account	$V_{OL} = 0 V$	-10			
l <sub>OZ</sub>	Output high impedance current	VREF = 1.95 V				μΑ
		V <sub>OH</sub> = VREF			10	
	Low level input current <sup>(4)</sup>	VREF = 1.95 V	-5			
I <sub>IL</sub>	Low level input current ??	$V_I = 0 V$	_o			μA
	High level input current <sup>(4)</sup>	VREF = 1.95 V		6	6	
I <sub>IH</sub>	night level input currents	V <sub>I</sub> = VREF			6	μA
	Law Javalianut august (5)	VREF = 1.95 V	705			
I <sub>IL2</sub>	Low level input current <sup>(5)</sup>	$V_I = 0 V$	-785			μA
	High level input ourrest (5)	VREF = 1.95 V			6	
I <sub>IH2</sub>	High level input current <sup>(5)</sup>	V <sub>I</sub> = VREF			6	μΑ
	Low level input current <sup>(6)</sup>	VREF = 1.95 V	-5			
I <sub>IL3</sub>	Low level input current.	$V_I = 0 V$	_s			μA
	High level input current <sup>(6)</sup>	VREF = 1.95 V			785	
I <sub>IH3</sub>	night level input current	$V_I = VREF$			765	μA
CURRENT						
I <sub>REF</sub>	Current at V <sub>REF</sub> = 1.95 V	f <sub>DCLK</sub> = 80 MHz			2.80	mA
I <sub>cc</sub>	Current at V <sub>CC</sub> = 2.75 V	f <sub>DCLK</sub> = 80 MHz			59.90	mA
I <sub>OFFSET</sub>	Current at V <sub>OFFSET</sub> = 8.75 V				2.93	mA
I <sub>BIAS</sub>	Current at V <sub>BIAS</sub> = 16.5 V				2.30	mA
I <sub>RESET</sub>	Current at V <sub>RESET</sub> = −10.5 V				-2.00	mA

- (1) Device electrical characteristics are over Recommended Operating Conditions unless otherwise noted.
- (2) All voltage values are with respect to the ground pins (V<sub>SS</sub>).
- 3) Specification is for LVCMOS JTAG output pin TDO.
- (4) Specification is for LVCMOS input pins, which do not have pull up or pull down resistors. See *Pin Configuration and Functions* section.
- (5) Specification is for LVCMOS input pins which do have pull up resistors (JTAG: TDI, TMS). See Pin Configuration and Functions section.
- (6) Specification is for LVCMOS input pins which do have pull down resistors. See Pin Configuration and Functions section.



# **Electrical Characteristics (continued)**

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	PARAMETER	TEST CONDITIONS (2)	MIN	TYP	MAX	UNIT
POWER <sup>(7)</sup>						
P <sub>REF</sub>	Power at V <sub>REF</sub> = 1.95 V	f <sub>DCLK</sub> = 80 MHz			5.46	mW
P <sub>CC</sub>	Power at V <sub>CC</sub> = 2.75 V	f <sub>DCLK</sub> = 80 MHz			164.73	mW
P <sub>OFFSET</sub>	Power at V <sub>OFFSET</sub> = 8.75 V				25.64	mW
P <sub>BIAS</sub>	Power at V <sub>BIAS</sub> = 16.5 V				37.95	mW
P <sub>RESET</sub>	Power at V <sub>RESET</sub> = −10.5 V				21.00	mW
P <sub>TOTAL</sub>	Total power at nominal conditions	f <sub>DCLK</sub> = 80 MHz		105	254.77	mW
CAPACITA	NCE	•	•		·	
C <sub>IN</sub>	Input pin capacitance	f = 1 MHz			20	pF
C <sub>A</sub>	Analog pin capacitance (TEMP_PLUS and TEMP_MINUS pins)	f = 1 MHz			65	pF
C <sub>o</sub>	Output pin capacitance	f = 1 MHz			20	pF

<sup>(7)</sup> The following power supplies are all required to operate the DMD:  $V_{DD}$ ,  $V_{DDI}$ ,  $V_{OFFSET}$ ,  $V_{BIAS}$ ,  $V_{RESET}$ . All  $V_{SS}$  connections are also required.

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# 6.7 Timing Requirements

Over Recommended Operating Conditions unless otherwise noted.

	ecommended Operating Conditions unless otherwise noted.	MIN	NOM	MAX	UNIT
DMD M	IIRROR AND SRAM CONTROL LOGIC SIGNALS				
t <sub>SU</sub>	Setup time SAC_BUS low before SAC_CLK↑	1.0			ns
t <sub>H</sub>	Hold time SAC_BUS low after SAC_CLK↑	1.0			ns
t <sub>SU</sub>	Setup time DAD_BUS high before SAC_CLK↑	1.0			ns
t <sub>H</sub>	Hold time DAD_BUS after SAC_CLK↑	1.0			ns
t <sub>C</sub>	Cycle time SAC_CLK	12.5		16.67	ns
t <sub>W</sub>	Pulse width 50% to 50% reference points: SAC_CLK high or low	5.0			ns
$t_R$	Rise time 20% to 80% reference points: SAC_CLK			2.5	ns
t <sub>F</sub>	Fall time 80% to 20% reference points: SAC_CLK			2.5	ns
DMD D	ATA PATH AND LOGIC CONTROL SIGNALS			·	
$t_{SU}$	Setup time DATA(14:0) before DCLK↑ or DCLK↓	1.0			ns
t <sub>H</sub>	Hold time DATA(14:0) after DCLK↑ or DCLK↓	1.0			ns
t <sub>SU</sub>	Setup time SCTRL before DCLK↑ or DCLK↓	1.0			ns
t <sub>H</sub>	Hold time SCTRL after DCLK↑ or DCLK↓	1.0			ns
t <sub>SU</sub>	Setup time TRC before DCLK↑ or DCLK↓	1.0			ns
t <sub>H</sub>	Hold time TRC after DCLK↑ or DCLK↓	1.0			ns
t <sub>SU</sub>	Setup time LOADB low before DCLK↑	1.0			ns
t <sub>H</sub>	Hold time LOADB low after DCLK↓	1.0			ns
t <sub>SU</sub>	Setup time RESET_STROBE high before DCLK↑	1.0			ns
t <sub>H</sub>	Hold time RESET_STROBE after DCLK↑	3.5			ns
$t_{C}$	Cycle time DCLK	12.5		16.67	ns
t <sub>W</sub>	Pulse width 50% to 50% reference points: DCLK high or low	5.0			ns
t <sub>W</sub> (L)	Pulse width 50% to 50% reference points: LOADB low	7.0			ns
t <sub>W</sub> (H)	Pulse width 50% to 50% reference points: RESET_STROBE high	7.0			ns
$t_R$	Rise time 20% to 80% reference points: DCLK, DATA, SCTRL, TRC, LOADB			2.5	ns
$t_{F}$	Fall time 80% to 20% reference points: DCLK, DATA, SCTRL, TRC, LOADB			2.5	ns
JTAG E	BOUNDARY SCAN CONTROL LOGIC SIGNALS			·	
$f_{TCK}$	Clock frequency TCK			10	MHz
$t_{C}$	Cycle time TCK	100			ns
$t_W$	Pulse width 50% to 50% reference points: TCK high or low	10			ns
t <sub>SU</sub>	Setup time TDI valid before TCK↑	5			ns
t <sub>H</sub>	Hold time TDI valid after TCK↑	25			ns
t <sub>SU</sub>	Setup time TMS valid before TCK↑	5			ns
t <sub>H</sub>	Hold time TMS valid after TCK↑	25			ns
t <sub>R</sub>	Rise time 20% to 80% reference points: TCK, TDI, TMS			2.5	ns
t <sub>R</sub>	Fall time 80% to 20% reference points: TCK, TDI, TMS			2.5	ns



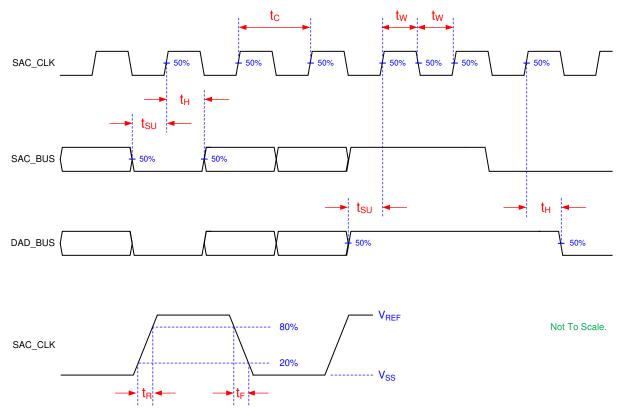


Figure 2. DMD Mirror and SRAM Control Logic Timing Requirements



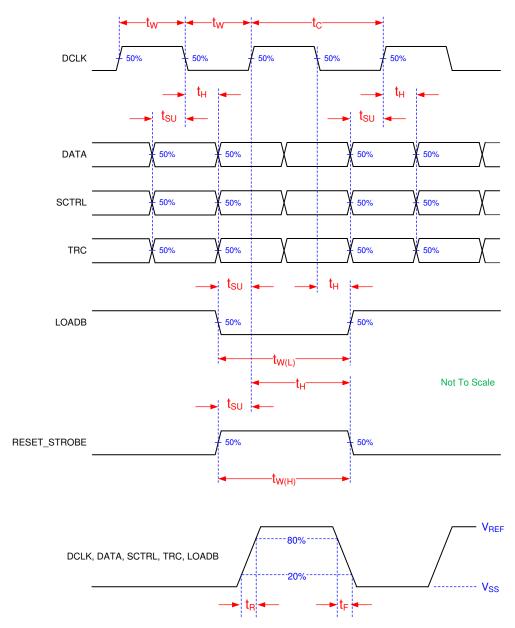
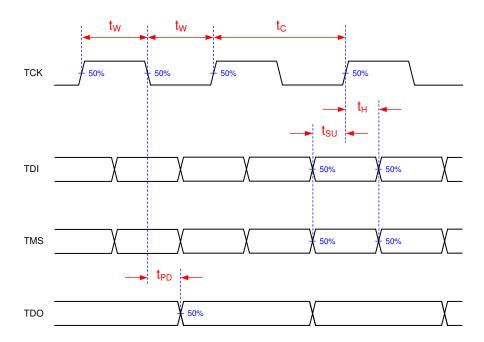


Figure 3. DMD Data Path and Control Logic Timing Requirements





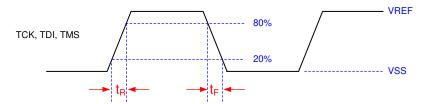


Figure 4. JTAG Boundary Scan Control Logic Timing Requirements

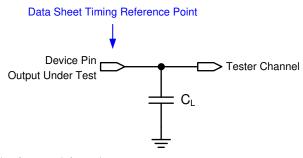


## 6.8 Switching Characteristics<sup>(1)</sup>

Over operating free-air temperature range (unless otherwise noted).

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PD</sub>	Output propagation, clock to Q (see Figure 4)	C <sub>L</sub> = 11 pF, from (Input) falling edge of TCK to (Output) TDO. See Figure 4.	3		25	ns

(1) Device electrical characteristics are over Recommended Operating Conditions unless otherwise noted.



See *Micromirror Array* section for more information.

Figure 5. Test Load Circuit for Output Propagation Measurement

### 6.9 System Mounting Interface Loads

PARAMETER	MIN NOM	MAX	UNIT		
Condition 1:					
Uniformly distributed within the Thermal Interface Area shown in Figure 6		11.30	kg		
Uniformly distributed within the Electrical Interface Area shown in Figure 6 11.34					
Condition 2:	<u> </u>				
Uniformly distributed within the Thermal Interface Area shown in Figure 6		0	kg		
Uniformly distributed within the Electrical Interface Area shown in Figure 6		22.64	kg		

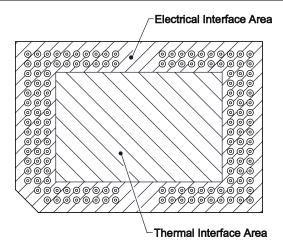


Figure 6. System Interface Loads



# 6.10 Physical Characteristics of the Micromirror Array

PARAMETE	VALUE	UNIT	
N Number of active columns	See Figure 7	684	micromirrors
M Number of active rows	See Figure 7	608	micromirrors
ε Micromirror (pixel) pitch – diagonal	See Figure 8	7.6	μm
P Micromirror (pixel) pitch – horizontal and vertical	See Figure 8	10.8	μm
Micromirror active array width	P x M + P / 2; see Figure 7	6.5718	mm
Micromirror active array height	(P x N) / 2 + P / 2; see Figure 7	3.699	mm
Micromirror active border	Pond of micromirror (POM) <sup>(1)</sup>	10	micromirrors/side

(1) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the POM. These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.

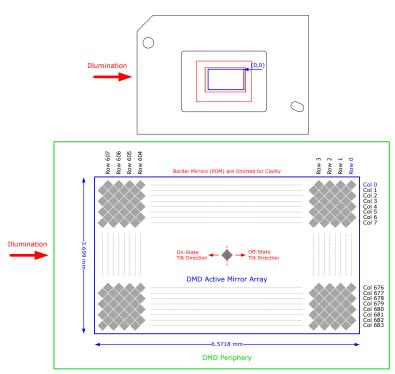


Figure 7. Micromirror Array Physical Characteristics

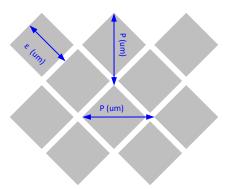


Figure 8. Mirror (Pixel) Pitch

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## 6.11 Micromirror Array Optical Characteristics

Table 1. Optical Parameters<sup>(1)</sup>

	PARAMET	ΓER	MIN	NOM	MAX	UNIT
α	Micromirror Tilt Angle, landed (on-state	e or off-state) (see <sup>(2)</sup> and Figure 9)		12		0
β	Micromirror Tilt Angle Variation, device	-1		1	0	
	DMD Efficiency, 400 nm - 680 nm (see		66%			
	Number of non-operational micromirrors (4)	Adjacent micromirrors	0		:	
		Non-adjacent micromirrors			10	micromirrors

- (1) Optical parameters are characterized at 25°C.
- (2) Mirror Tilt: Limits on variability of mirror tilt are critical in the design of the accompanying optical system. Variations in tilt angle within a device may result in apparent non-uniformities, such as line pairing and image mottling, across the projected image especially at higher system F/#. Variations in the average tilt angle between devices may result in colorimetry, brightness, and system contrast variations.
- (3) DMD efficiency is measured photopically under the following conditions: 24° illumination angle, F/2.4 illumination and collection apertures, uniform source spectrum (halogen), uniform pupil illumination, the optical system is telecentric at the DMD, and the efficiency numbers are measured with 100% electronic mirror duty cycle and do not include system optical efficiency or overfill loss. Note that this number is measured under conditions described above and deviations from these specified conditions could result in a different efficiency value in a different optical sytem. The factors that can incluence the DMD efficiency related to system application include: light source spectral distribution and diffraction efficiency at those wavelengths (especially with discrete light sources such as LEDs or lasers), and illumination and collection apertures (F/#) and diffraction efficiency. The interaction of these system factors as well as the DMD efficiency factors that are not system dependent are described in detail in the DMD Optical Efficiency Application Note, which can be accessed by contacting TI Applications Engineering.
- (4) A non-operational micromirror is defined as a micromirror that is unable to transition between the on-state and off-state positions.

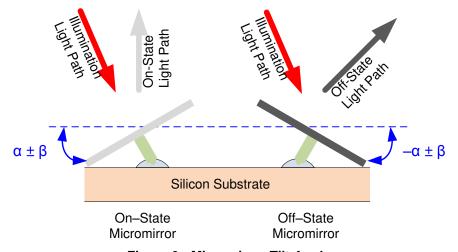


Figure 9. Micromirror Tilt Angle



#### 6.12 Window Characteristics

	PARAMETER	MIN	NOM	MAX	UNIT	
Window material designation		Cor	ning Eagle XG			
Window refractive index	at wavelength 546.1 nm		1.5119			
Window aperture <sup>(1)</sup>				See (1)		

<sup>(1)</sup> See the package mechanical ICD for details regarding the size and location of the window aperture.

### 6.13 Chipset Component Usage Specification

The DLP3034-Q1 DMD is a component of the DLP® chipset including the DLPC120-Q1 DMD controller. Reliable function and operation of the DMD requires that it be used in conjunction with DLPC120-Q1 controller.

#### **NOTE**

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously

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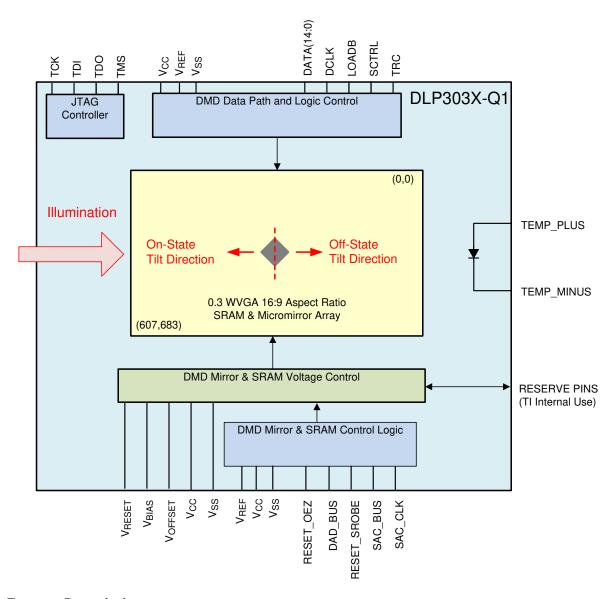


### 7 Detailed Description

#### 7.1 Overview

The DLP3034-Q1 DMD has a resolution of  $608 \times 684$  mirrors configured in a diamond format that results in an aspect ratio of 16:9, which combined with the DLPC120-Q1 image processing creates an effective resolution of  $864 \times 480$  square pixels. By configuring the pixels in a diamond format, the illumination input to the DMD enters from the side allowing for smaller mechanical packaging of the optical system. Additionally, side illumination can also enable increased optical efficiency compared to a corner illuminated square pixel design.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

To ensure reliable operation, the DLP3034-Q1 DMD must be used with the DLPC120-Q1 DMD Display controller.

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#### 7.3.1 Micromirror Array

The DLP3034-Q1 DMD consists of a two-dimensional array of 1-bit CMOS memory cells that determine the state of the each of the 608  $\times$  684 micromirrors in the array. Refer to Physical Characteristics of the Micromirror Array for a calculation of how the 608  $\times$  684 micromirror array represents a 16:9 dimensional aspect ratio to the user. Each micromirror is either "ON" (tilted +12°) or "OFF" (tilted -12°). Combined with appropriate projection optical system the DMD can be used to create clear, colorful, and vivid digital images.

#### 7.3.2 Double Data Rate (DDR) Interface

Each DMD micromirror and its associated SRAM memory cell is loaded with data from the DLPC120-Q1 via the DDR interface (DATA(14:0), DCLK, LOADB, SCRTL, and TRC). These signals are low voltage CMOS nominally operating at 1.8-V level to reduce power and switching noise. This high speed data input to the DMD allows for a maximum update rate of the entire micromirror array to be nearly 5 kHz, enabling the creation of seamless digital images using Pulse Width Modulation (PWM).

#### 7.3.3 Micromirror Switching Control

Once data is loaded onto the DMD, the mirrors are caused to switch position (+12° or -12°) based on the timing signal sent to the DMD Mirror and SRAM control logic. The DMD mirrors will be switched from OFF to ON or ON to OFF, or stay in the same position based on control signals DAD\_BUS, RESET\_STROBE, SAC\_BUS, and SAC\_CLK, which are coordinated with the data loading by the DLPC120-Q1. In general, the DLPC120-Q1 loads the DMD SRAM memory cells over the DDR interface, and then commands to the micromirrors to switch position.

At power down, the DMD Mirrors are commanded by the DLPC120-Q1 to move to a near flat (0°) position as shown in *Power Supply Recommendations* section. The flat state position of the DMD mirrors are referred to as the "Parked" state. To maintain long term DMD reliability, the DMD must be properly "Parked" prior to every power down of the DMD power supplies. Refer to the *DLPC120-Q1 Programmer's Guide* for information about properly parking the DMD.

### 7.3.4 DMD Voltage Supplies

The micromirrors switching requires unique voltage levels to control the mechanical switching. These voltages levels are nominally 16 V, 8.5 V, and -10 V ( $V_{BIAS}$ ,  $V_{OFFSET}$ , and  $V_{RESET}$ ). The specification values for  $V_{BIAS}$ ,  $V_{OFFSET}$ , and  $V_{RESET}$  are shown in *Recommended Operating Conditions*.

### 7.3.5 Logic Reset

Reset of the DMD is required and controlled by the DLPC120-Q1.

#### 7.3.6 Temperature Sensing Diode

The DMD includes a temperature sensing diode designed to be used with the TMP411-Q1 temperature monitoring device. The DLPC120-Q1 monitors the DMD array temperature via the TMP411-Q1 and temperature sense diode. The DLPC120-Q1 operation of the DMD is based in part on the DMD array temperature, and therefore, this connection is essential to ensure reliable operation of the DMD.

Figure 10 shows the typical connection between the DLPC120-Q1, TMP411-Q1, and the DLP3034-Q1 DMD. The signals to the temperature sense diode are sensitive to system noise, therefore, care should be taken in the routing and implementation of this circuit. See the *TMP411-Q1 Data Sheet* for detailed PCB layout recommendations.



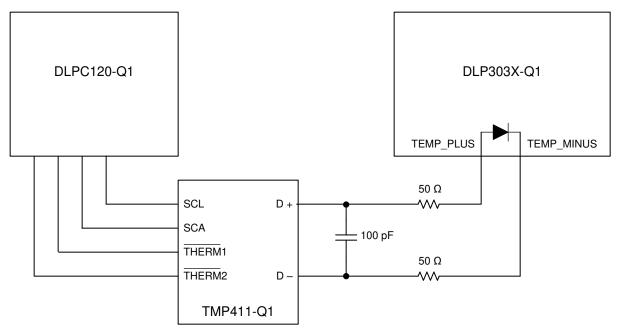


Figure 10. Temperature Sense Diode Typical Circuit Configuration

The DLPC120-Q1 automatically controls the DMD parking based on the temperature measured from the temperature sense diode; however, it is recommended that the host controller manage the parking via the proper methods described in the DLPC120-Q1 Programmer's Guide.

### 7.3.6.1 Temperature Sense Diode Theory

A temperature sensing diode is based on the fundamental current and temperature characteristics of a transistor. The diode is formed by connecting the transistor base to the collector. Two different known currents flow through the diode and the resulting diode voltage is measured in each case. The difference in their base-emitter voltages is proportional to the absolute temperature of the transistor.

Refer to the TMP411-Q1 Data Sheet for detailed information about temperature diode theory and measurement. Figure 11 and Figure 12 illustrate the relationship between the current and voltage through the diode.

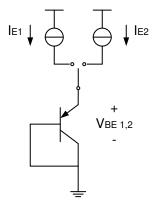


Figure 11. Temperature Measurement Theory

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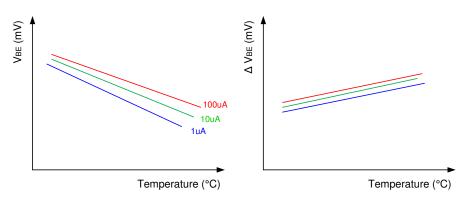


Figure 12. Example of Delta VBE vs Temperature

#### 7.3.7 DMD JTAG Interface

The DMD uses 4 standard JTAG signals for sending and receiving boundary scan test data. TCK is the test clock used to drive an IEEE 1149.1 TAP state machine and logic. TMS directs the next state of the TAP state machine. TDI is the scan data input and TDO is the scan data output.

The DMD does not support IEEE 1149.1 signals TRST (Test Logic Reset) and RTCK (Returned Test Clock). Boundary scan cells on the DMD are Observe-Only. To initiate the JTAG boundary scan operation on the DMD, a minimum of 6 TCK clock cycles are required after TMS is set to logic high.

Refer to Figure 13 for a JTAG system board routing example. The DLPC120-Q1 can be enabled to perform an in system boundary scan test. See *DLPC120-Q1 Programmer's Guide* for information about this test.

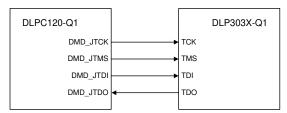


Figure 13. System Interface Connection to DLPC120-Q1

The DMD Device ID can be read via the JTAG interface. The ID and 32-bit shift order is shown in Figure 14.

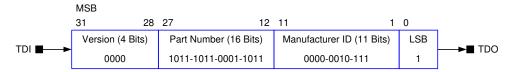


Figure 14. DMD Device ID and 32-bit Shift Order

Refer to Figure 15 for a JTAG boundary scan block diagram for the DMD. These show the pins and the scan order that are observed during the JTAG boundary scan.

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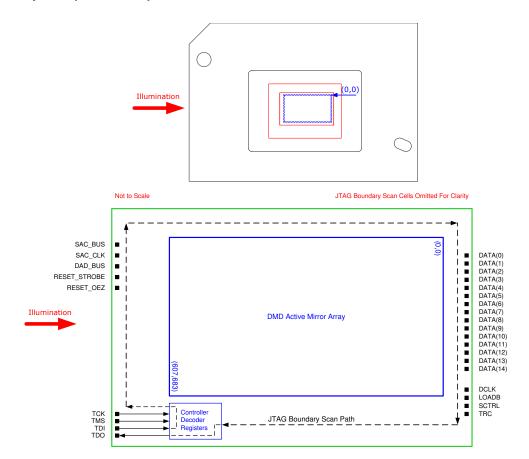


Figure 15. JTAG Boundary Scan Path

Refer to Figure 16 for a functional block diagram of the JTAG control logic.



Not to Scale. BSC = Boundary Scan Cell [Observe Only]
Note 1: Signal Routing Omitted for Clarity.

TAP = Test Access Port

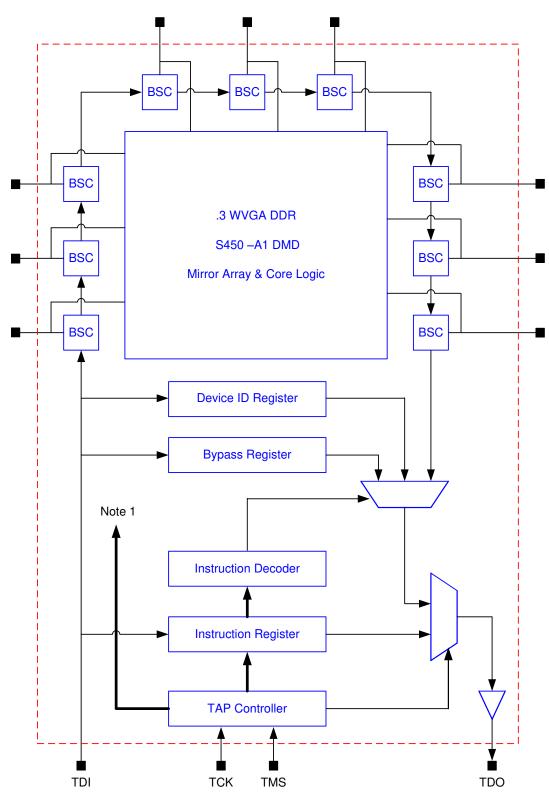


Figure 16. JTAG Functional Block Diagram



#### 7.4 System Optical Considerations

Optimizing system optical performance and image quality strongly relates to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described below.

#### 7.4.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block flat-state and stray light from passing through the projection lens. The mirror tilt angle defines DMD capability to separate the "On" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the mirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, contrast ratio can be reduced and objectionable artifacts in the image border and/or active area could occur.

### 7.4.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within two degrees of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the image border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

#### 7.4.3 Illumination Overfill and Alignment

Overfill light illuminating the area outside the active array can create artifacts from the mechanical features and other surfaces that surround the active array. These artifacts may be visible in the projected image. The illumination optical system should be designed to minimize light flux incident outside the active array and on the window aperture. Depending on the particular system's optical architecture and assembly tolerances, this amount of overfill light on the area outside of the active array may still cause artifacts to be visible. Illumination light and overfill can also induce undesirable thermal conditions on the DMD, especially if illumination light impinges directly on the DMD window aperture or near the edge of the DMD window. Refer to *Recommended Operating Conditions* for a specification on this maximum allowable heat load due to illumination overfill.

#### NOTE

TI ASSUMES NO RESPONSIBILITY FOR IMAGE QUALITY ARTIFACTS OR DMD FAILURES CAUSED BY OPTICAL SYSTEM OPERATING CONDITIONS EXCEEDING LIMITS DESCRIBED ABOVE.

### 7.5 Micromirror Array Temperature Calculation

Active array temperature can be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load.

Relationship between array temperature and the reference ceramic temperature (thermocouple location TP1 in Figure 17) is provided by the following equations.

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY-TO-CERAMIC})$$
 (1)

 $Q_{ARRAY} = Q_{ELECTRICAL} + (Q_{INCIDENT} \times DMD Absorption Constant)$ 

#### where

- T<sub>ARRAY</sub> = computed DMD array temperature (°C)
- T<sub>CERAMIC</sub> = measured ceramic temperature (TP1 location in Figure 17) (°C)
- R<sub>ARRAY-TO-CERAMIC</sub> = DMD package thermal resistance from array to TP1 (°C/watt) (see *Thermal Information*)
- Q<sub>ARRAY</sub> = total power, electrical plus absorbed, on the DMD array (watts)
- Q<sub>ELECTRICAL</sub> = nominal electrical power dissipation by the DMD (watts)
- Q<sub>INCIDENT</sub> = incident optical power to DMD (watts)
- DMD Absorption Constant = 0.42

(2)



## **Micromirror Array Temperature Calculation (continued)**

Electrical power dissipation of the DMD is variable and depends on the voltages, data rates and operating frequencies.

Absorbed power from the illumination source is variable and depends on the operating state of the mirrors and the intensity of the light source.

Equations shown previous are valid for a 1-chip DMD system with illumination distribution of 83.7% on the active array and 16.3% on the array border.

#### Sample calculation:

- Q<sub>ELECTRICAL</sub> = 0.105 W
- $T_{CERAMIC} = 55^{\circ}C$
- Q<sub>INCIDENT</sub> = 3 W

$$Q_{ARRAY} = 0.105 W + (3 W \times 0.42) = 1.37 W$$
 (3)

 $T_{ARRAY} = 55^{\circ}C + (1.37 \text{ W} \times 2.5^{\circ}C/\text{W}) = 58.4^{\circ}C$  (4)

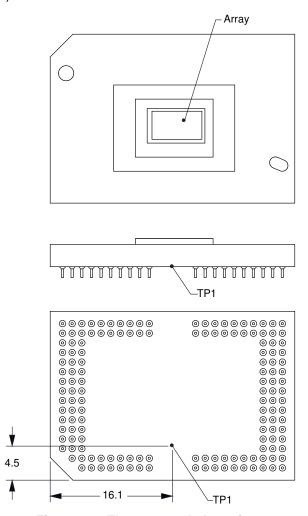


Figure 17. Thermocouple Locations

### 7.6 Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

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### Micromirror Landed-On/Landed-Off Duty Cycle (continued)

As an example, assuming a fully-saturated white pixel, a landed duty cycle of 90/10 indicates that the referenced pixel is in the ON state 90% of the time (and in the OFF state 10% of the time), whereas 10/90 would indicate that the pixel is in the OFF state 90% of the time. Likewise, 50/50 indicates that the pixel is ON 50% of the time and OFF 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.



### 8 Application and Implementation

#### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The DLP3034-Q1 DMD was designed to be used in automotive applications such as transparent window displays. The information shown in this section describes the transparent window display application based on the TI reference design. Contact TI application engineer for information on this design.

### 8.2 Typical Application

The DLP3034-Q1 DMD combined with the DLPC120-Q1 are the primary devices that make up the reference design for a transparent window display system as shown in the block diagram Figure 18.

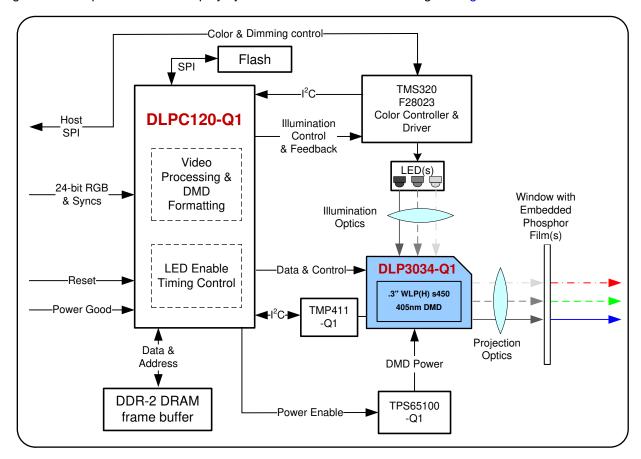


Figure 18. DLP3034-Q1 Reference Design Block Diagram

The DLPC120-Q1 accepts input video over the parallel RGB data interface up to 8 bits per color from a Video Graphics processor. The DLPC120-Q1 then processes the video data (864 × 480 manhattan orientation) by scaling the image to match the DMD resolution (608 × 684 diamond pixel), applies de-gamma correction, bezel adjustment, and then formats the data into DMD bit plane information and stores the data into the DDR2 DRAM. The DMD bit planes are read from DDR2 DRAM, and are then displayed on the DMD using Pulse Width Modulation (PWM) timing. The DLPC120-Q1 synchronizes the DMD bit plane data with the color enable timing for the LED color controller and Driver circuit. Finally, the DMD accepts the bit plane formatted data from the DLPC120-Q1 and displays the data according to the timing controlled by the DLPC120-Q1.

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### **Typical Application (continued)**

Due to the mechanical nature of the micromirrors, the latency of the DLP3034-Q1 and DLPC120-Q1 chipset is fixed across all temperature and operating conditions. The observed video latency is one frame, or 16.67 ms at an input frame rate of 60 Hz. However, please note that the use of the DLPC120-Q1 bezel adjustment feature, if enabled by the host controller, requires an additional frame of processing.

The DLPC120-Q1 is configured at power up by data stored in the flash file which stores configuration data, DMD and sequence timing information, LED drive information, and other information related to the system functions. See the *DLPC120-Q1 Programmer's Guide* for information about the this flash configuration data.

The transparent emissive display reference design from TI includes the TMS320F28023 Microcontroller (Piccolo), which is used to adjust the LED current levels in order to control the brightness levels and also the color point for systems with multiple color channels.

### 8.3 Application Mission Profile Consideration

Each application is anticipated to have different mission profiles, or number of operating hours at different temperatures. To assist in evaluation, the automotive DMD reliability lifetime estimates Application Report may be provided. See the TI Application team for more information.

#### 8.4 Illumination Mission Profile Considerations

TI has performed evaluations at 405-nm illumination wavelengths under certain conditions. These conditions should be considered when evaluating the final application's implementation. Please contact the TI Application team for details about this testing.



### 9 Power Supply Recommendations

### 9.1 Power Supply Sequencing Requirements

V<sub>BIAS</sub>, V<sub>CC</sub>, V<sub>OFFSET</sub>, V<sub>REF</sub>, V<sub>RESET</sub>, V<sub>SS</sub> are required to operate the DMD.

#### **CAUTION**

- For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to the prescribed power up and power down procedures may affect device reliability.
- The V<sub>CC</sub>, V<sub>REF</sub>, V<sub>OFFSET</sub>, V<sub>BIAS</sub>, and V<sub>RESET</sub> power supplies have to be coordinated during power up and power down operations. Failure to meet any of the below requirements will result in a significant reduction in the DMD's reliability and lifetime. Refer to Figure 19. V<sub>SS</sub> must also be connected.

## **DMD Power Supply Power Up Procedure:**

- During power up, V<sub>CC</sub> and V<sub>REF</sub> must always start and settle before V<sub>OFFSET</sub>, V<sub>BIAS</sub> and V<sub>RESET</sub> voltages are applied to the DMD.
- During power up, V<sub>BIAS</sub> does not have to start after V<sub>OFFSET</sub>. However, it is a strict requirement that the delta between V<sub>BIAS</sub> and V<sub>OFFSET</sub> must be within ±8.75 V (refer to Note 1 for Figure 19).
- During power up, the DMD's LVCMOS input pins shall not be driven high until after V<sub>CC</sub> and V<sub>REF</sub> have settled at operating voltage.
- During power up, there is no requirement for the relative timing of V<sub>RESET</sub> with respect to V<sub>OFFSET</sub> and V<sub>BIAS</sub>.
- Power supply slew rates during power up are flexible, provided that the transient voltage levels follow the requirements listed above and in Recommended Operating Conditions and in Figure 19.

#### **DMD Power Supply Power Down Procedure**

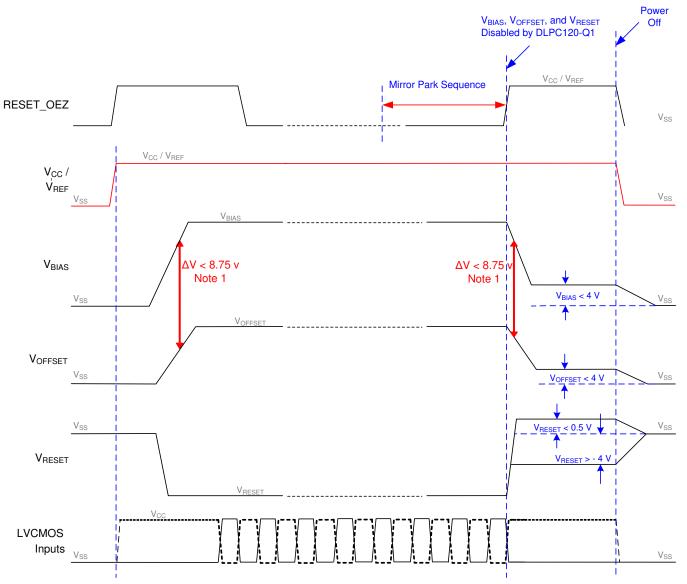
- $V_{CC}$  and  $V_{REF}$  must be supplied until after  $V_{BIAS}$ ,  $V_{RESET}$  and  $V_{OFFSET}$  are discharged to within 4 V of ground.
- During power down it is not mandatory to stop driving V<sub>BIAS</sub> prior to V<sub>OFFSET</sub>, but it is a strict requirement that the delta between V<sub>BIAS</sub> and V<sub>OFFSET</sub> must be within ± 8.75 V (refer to Note 1 for Figure 19).
- During power down, the DMD's LVCMOS input pins must be less than V<sub>REF</sub> + 0.3 V.
- During power down, there is no requirement for the relative timing of  $V_{RESET}$  with respect to  $V_{OFFSET}$  and  $V_{BIAS}$ .
- Power supply slew rates during power down are flexible, provided that the transient voltage levels follow the requirements listed above in *Recommended Operating Conditions* and in Figure 19.

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## **Power Supply Sequencing Requirements (continued)**

### 9.1.1 Power Up and Power Down



(1) ±8.75-V delta,  $\Delta V$ , shall be considered the max operating delta between  $V_{BIAS}$  and  $V_{OFFSET}$ . Customers may find that the most reliable way to ensure this is to power  $V_{OFFSET}$  prior to  $V_{BIAS}$  during power up and to remove  $V_{BIAS}$  prior to V<sub>OFFSET</sub> during power down.

Figure 19. Power Supply Sequencing Requirements (Power Up and Power Down)

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# 10 Layout

### 10.1 Layout Guidelines

Refer to *DLPC120-Q1 Data Sheet* for specific PCB layout and routing guidelines. For specific DMD PCB guidelines, use the following:

- V<sub>CC</sub> should have at least one 2.2-μF and four 0.1-μF capacitors evenly distributed among the 13 V<sub>CC</sub> pins.
- A 0.1-μF, X7R rated capacitor should be placed near every pin for the V<sub>REF</sub>, V<sub>BIAS</sub>, V<sub>RSET</sub>, and V<sub>OFF</sub>.

### 10.2 Temperature Diode Pins

The DMD has an internal diode (PN junction) that is intended to be used with an external TI TMP411-Q1 temperature sensing IC. PCB traces from the DMD's temperature diode pins to the TMP411-Q1 are sensitive to noise. See the TMP411-Q1 Data Sheet for specific routing recommendations.

Avoid routing the temperature diodes signals near other traces to avoid coupling of noise onto these signals.

### 10.3 Layout Example

Contact TI Application Engineering for access to the complete TI reference design PCB layout.

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# 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Device Nomenclature

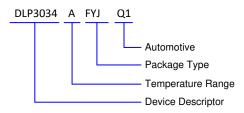


Figure 20. Part Number Description

### 11.1.2 Device Markings

The device marking is shown below. The marking will include both human-readable information and a 2-dimensional matrix code.

The human-readable information is described below. The 2-dimensional matrix code is an alpha-numeric character string that contains the DMD part number, part 1 of serial number, and part 2 of serial number.

The first character of the DMD serial number (part 1) is the manufacturing year. The second character of the DMD serial number (part 1) is the manufacturing month. The last character of the DMD serial number (part 2) is the bias voltage bin letter.

Example: \*DLP3034AFYJQ1 GHXXXXX LLLLLLM

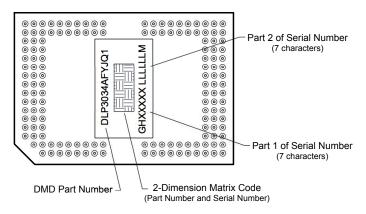


Figure 21. DMD Marking

A 3-dimensional modeled depiction of the DLP3034-Q1 device is shown below.

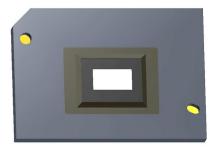


Figure 22. Image of DLP3034-Q1



### 11.2 Documentation Support

#### 11.2.1 Related Documentation

For related documentation see the following:

- DLPC120-Q1 product folder for the DLPC120-Q1 Data Sheet
- TMS320F2802x Piccolo™ Microcontrollers
- TMP411-Q1 ±1°C Remote and Local Temperature Sensor With N-Factor and Series Resistance Correction

### 11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.4 Community Resources

TI E2E<sup>TM</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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#### 11.5 Trademarks

E2E is a trademark of Texas Instruments.

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### 11.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.7 Device Handling

The DMD is an optical device so precautions should be taken to avoid damaging the glass window. Please see the DMD Handling application note for instructions on how to properly handle the DMD.

### 11.8 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

### 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

www.ti.com 10-Nov-2025

#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
	(1)	(2)			(5)	(4)	(5)		(0)
DLP3034AFYJQ1	Active	Production	CPGA (FYJ)   149	33   JEDEC TRAY (5+1)	Yes	Call TI	N/A for Pkg Type	-40 to 105	
DLP3034AFYJQ1.A	Active	Production	CPGA (FYJ)   149	33   JEDEC TRAY (5+1)	Yes	Call TI	N/A for Pkg Type	-40 to 105	
DLP3034AFYJQ1.B	Active	Production	CPGA (FYJ)   149	33   JEDEC TRAY (5+1)	-	Call TI	Call TI	-40 to 105	

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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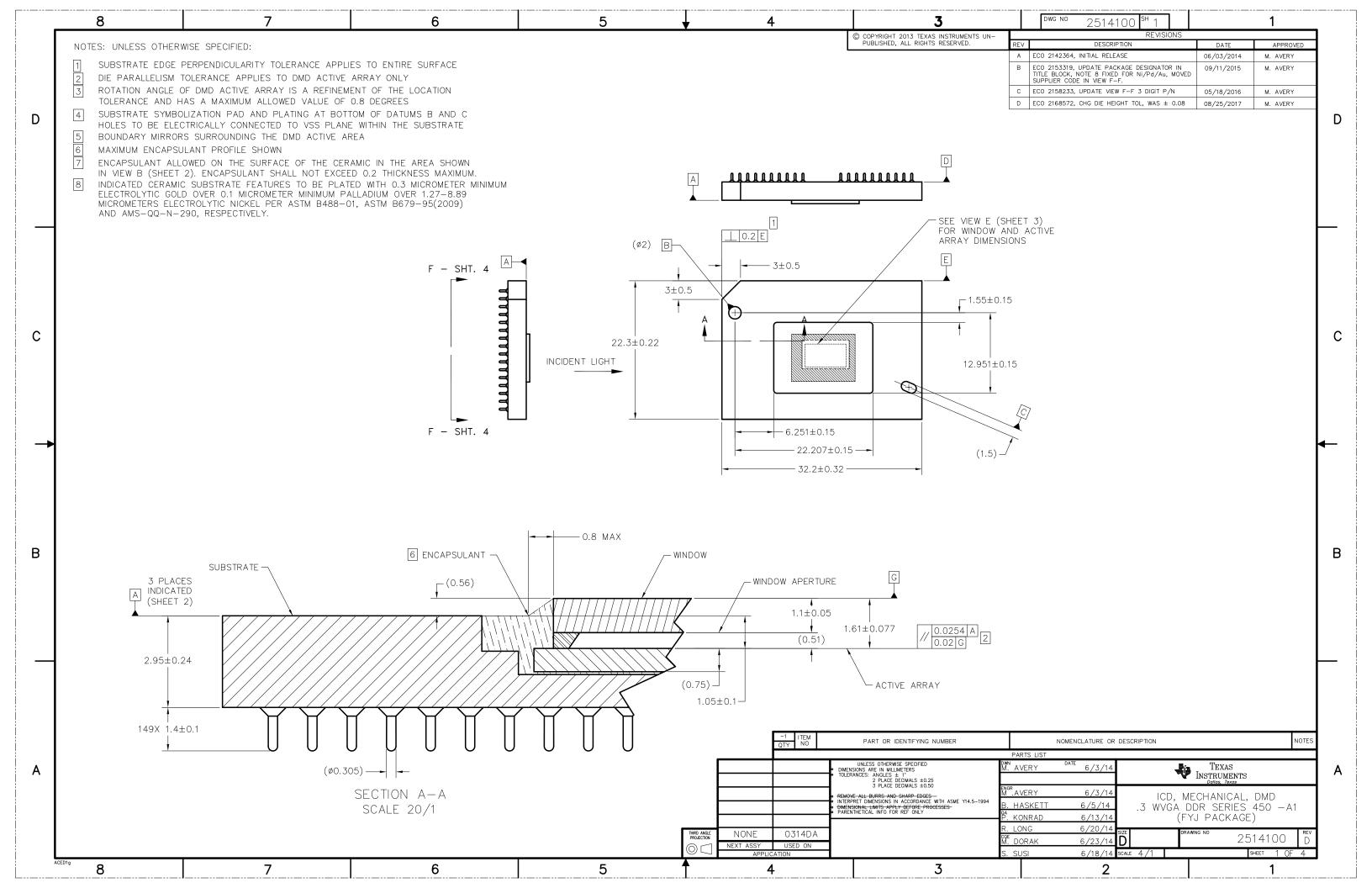
<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

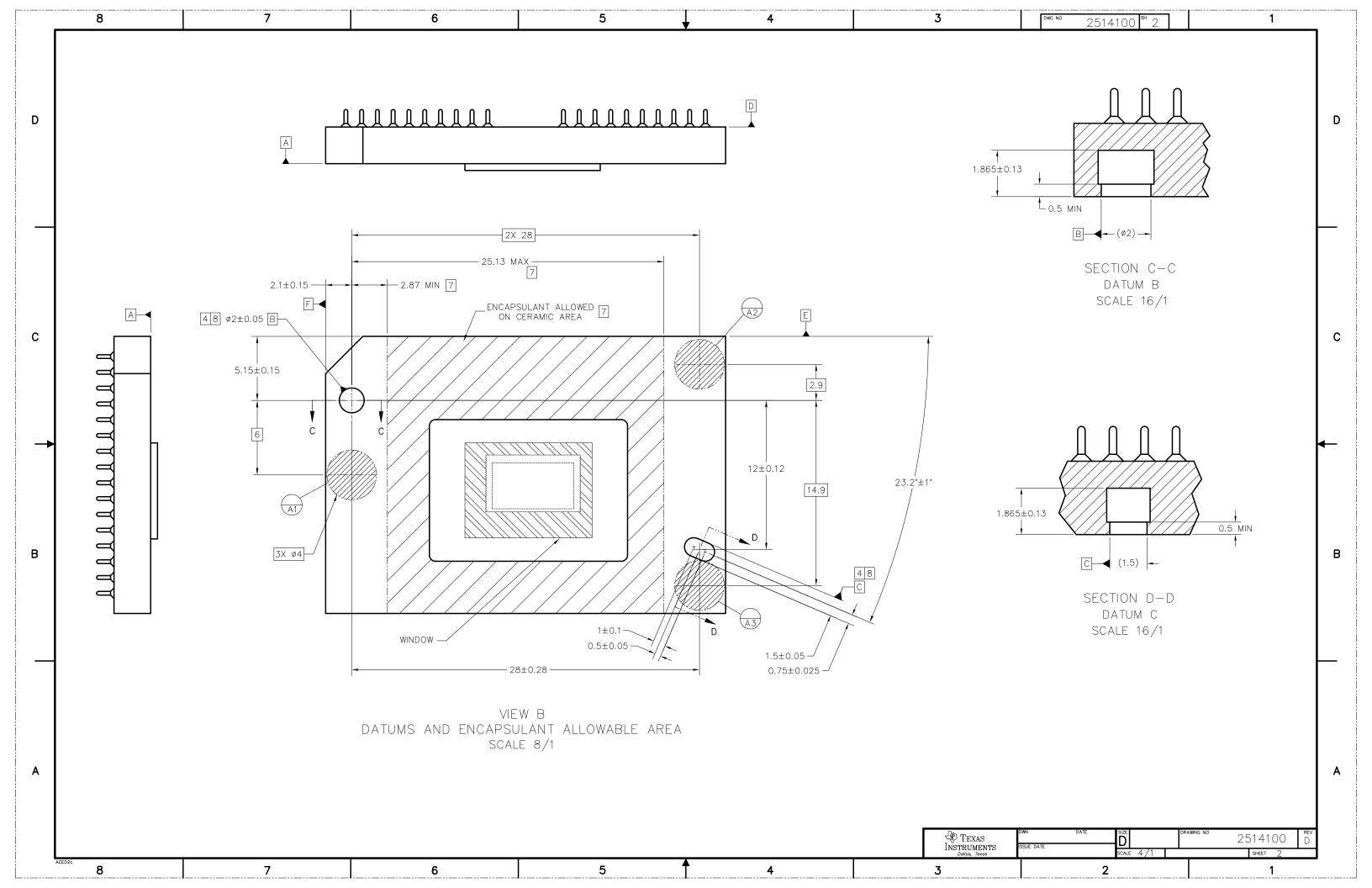
<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

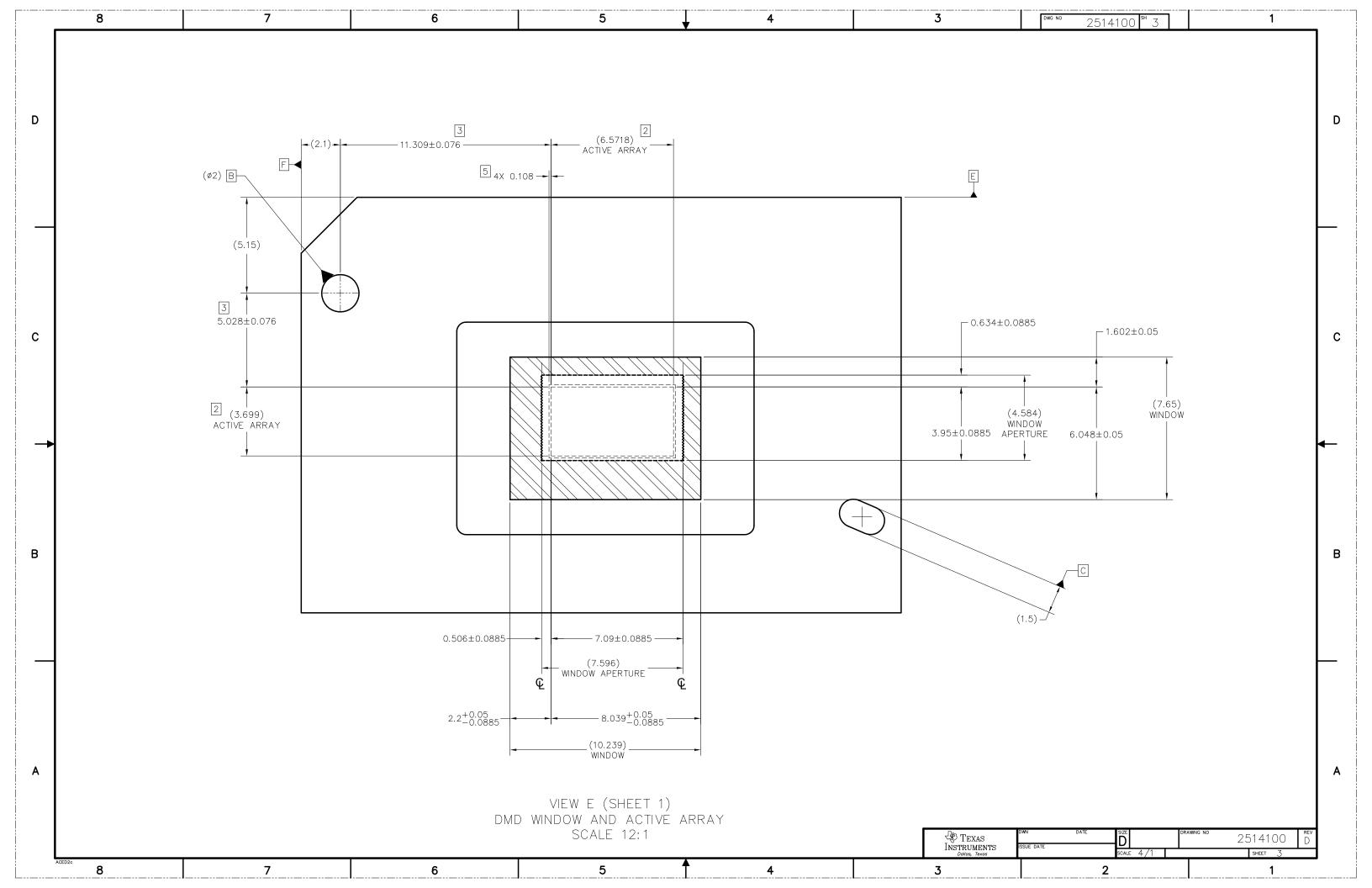
<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

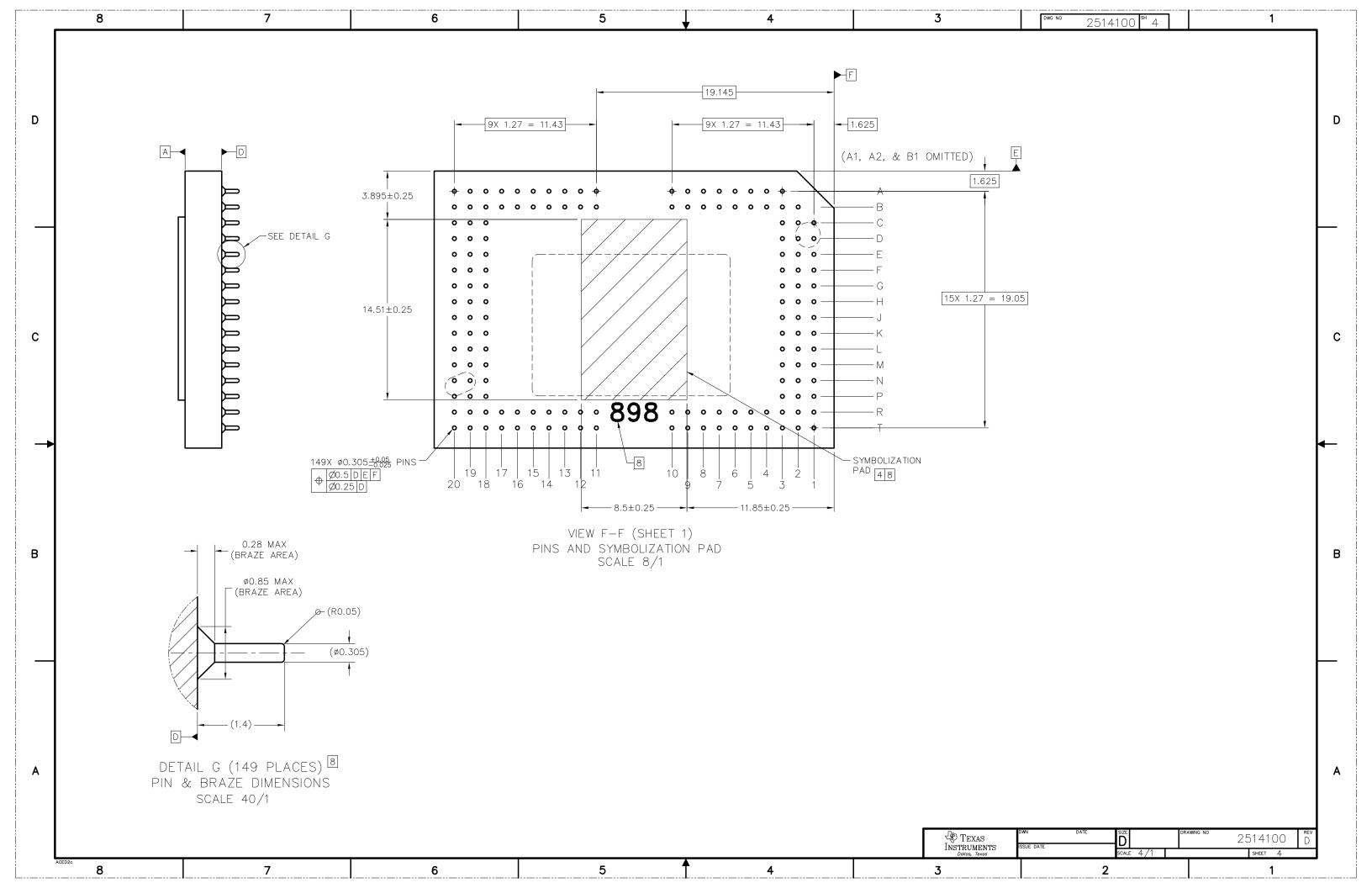
<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.









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