







**DLP300S** DLPS214B - JULY 2021 - REVISED MAY 2022

# DLP300S 0.3-Inch 3.6-Megapixel DMD for Low Cost TI DLP® 3D Printers

### 1 Features

- 0.3-Inch (7.93-mm) diagonal micromirror array
  - 1280 × 720 array of aluminum micrometersized mirrors, in an orthogonal layout
  - 3.6 Megapixels, 2560 x 1440 pixels on the resin
  - 5.4 micron micromirror pitch
  - ±17° micromirror tilt (relative to flat surface)
  - Side illumination for optimal efficiency and optical engine size
  - Polarization independent aluminum micromirror surface
- 8-Bit SubLVDS input data bus
- Dedicated DLPC1438 3D print controller and DLPA200x PMIC/LED driver for reliable operation

## 2 Applications

- TI DLP® 3D Printer
  - Additive manufacturing
  - Vat polymerization
  - Masked stereolithography (mSLA 3D printer)
- Light exposure: programmable spatial and temporal light exposure

## 3 Description

The DLP300S digital micromirror device (DMD) is a digitally controlled micro-opto-electromechanical system (MOEMS) spatial light modulator (SLM). When coupled to an appropriate optical system, the DMD displays a very crisp and high quality image. This DMD is part of the chipset comprising the DLP300S DMD, DLPC1438 3D print controller and DLPA200x PMIC/LED driver. The compact physical size of the DLP300S DMD coupled with the controller and the PMIC/LED driver provides a complete system solution that enables fast, high resolution, reliable DLP 3D printers.

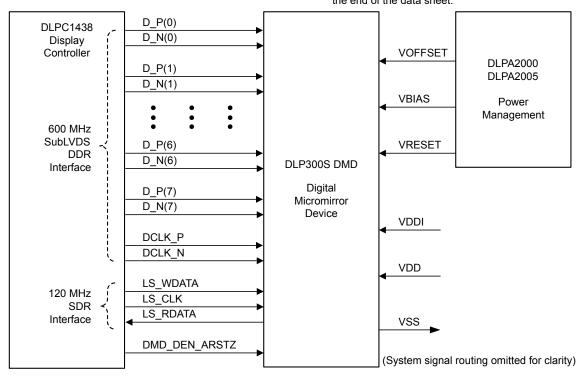
Get started with TI DLP® light-control technology page to learn how to get started with the DLP300S.

The DLP advanced light control resources on ti.com accelerate time to market, which include reference designs, optical module manufacturers, and DLP design network partners.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLP300S	FQK (57)	18.20-mm × 7.00-mm

For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Application



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# **4 Revision History**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2021) to Revision B (May 2022)	Page
Updated Absolute Maximum Ratings disclosure to the latest TI standard	6
Updated Micromirror Array Optical Characteristics	17
Added Third-Party Products Disclaimer	34
Changes from Revision (July 2021) to Revision A (August 2021)	Page
Changed the device status from Advance Information to Production Data	1
Updated Functional Block Diagram to show all high-speed data pairs	21



# **5 Pin Configuration and Functions**

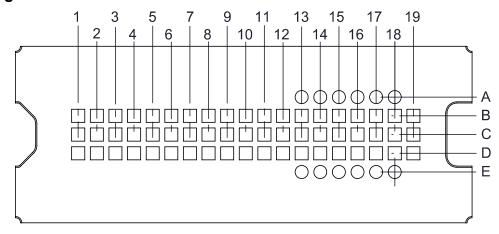


Figure 5-1. FQK Package 57-Pin LGA (Bottom View)

Table 5-1. Pin Functions – Connector Pins<sup>(1)</sup>

PIN		TYPE	TYPE SIGNAL DATA BATE		DESCRIPTION	PACKAGE NET	
NAME	NO.	TTPE	SIGNAL	DATA RATE	DESCRIPTION	LENGTH <sup>(2)</sup> (mm)	
DATA INPUTS				•			
D_N(0)	C9	ı	SubLVDS	Double	Data, Negative	10.54	
D_P(0)	В9	ı	SubLVDS	Double	Data, Positive	10.54	
D_N(1)	D10	I	SubLVDS	Double	Data, Negative	13.14	
D_P(1)	D11	I	SubLVDS	Double	Data, Positive	13.14	
D_N(2)	C11	I	SubLVDS	Double	Data, Negative	14.24	
D_P(2)	B11	I	SubLVDS	Double	Data, Positive	14.24	
D_N(3)	D12	ı	SubLVDS	Double	Data, Negative	14.35	
D_P(3)	D13	I	SubLVDS	Double	Data, Positive	14.35	
D_N(4)	D4	I	SubLVDS	Double	Data, Negative	5.89	
D_P(4)	D5	I	SubLVDS	Double	Data, Positive	5.89	
D_N(5)	C5	I	SubLVDS	Double	Data, Negative	5.45	
D_P(5)	B5	I	SubLVDS	Double	Data, Positive	5.45	
D_N(6)	D6	I	SubLVDS	Double	Data, Negative	8.59	
D_P(6)	D7	I	SubLVDS	Double	Data, Positive	8.59	
D_N(7)	C7	I	SubLVDS	Double	Data, Negative	7.69	
D_P(7)	В7	ı	SubLVDS	Double	Data, Positive	7.69	
DCLK_N	D8	ı	SubLVDS	Double	Clock, Negative	8.10	
DCLK_P	D9	ı	SubLVDS	Double	Clock, Positive	8.10	
CONTROL INPUTS			1	1			
LS_WDATA	C12	I	LPSDR <sup>(1)</sup>	Single	Write data for low speed interface.	7.16	
LS_CLK	C13	ı	LPSDR	Single	Clock for low-speed interface	7.89	
DMD_DEN_ARSTZ	C14	I	LPSDR		Asynchronous reset DMD signal. A low signal places the DMD in reset. A high signal releases the DMD from reset and places it in active mode.		
LS_RDATA	C15	0	LPSDR	Single	Read data for low-speed interface		
POWER (3)			Т	•			
VBIAS	C1	Power			Supply voltage for positive bias level at		
VBIAS	C18	Power			micromirrors		



## Table 5-1. Pin Functions – Connector Pins<sup>(1)</sup> (continued)

PIN	PIN					PACKAGE NET
NAME	NO.	TYPE	SIGNAL	DATA RATE	DESCRIPTION	LENGTH <sup>(2)</sup> (mm)
VOFFSET	D1	Power			Supply voltage for HVCMOS core	
VOFFSET	D17	Power			logic. Supply voltage for stepped high level at micromirror address electrodes. Supply voltage for offset level at micromirrors.	
VRESET	B1	Power			Supply voltage for negative reset level	
VRESET	B18	Power			at micromirrors.	
VDD	В6	Power				
VDD	B10	Power				
VDD	B19	Power				
VDD	C6	Power			Supply voltage for LVCMOS core logic.	
VDD	C10	Power			Supply voltage for LPSDR inputs. Supply voltage for normal high level at	
VDD	C19	Power				
VDD	D2	Power			micromirror address electrodes.	
VDD	D18	Power				
VDD	D19	Power				
VDDI	B2	Power				
VDDI	C2	Power			Complementary for Code DVDC management	
VDDI	C3	Power			Supply voltage for SubLVDS receivers.	
VDDI	D3	Power				
VSS	В3	Ground				
VSS	B4	Ground				
VSS	B8	Ground				
VSS	B12	Ground				
VSS	B13	Ground				
VSS	B14	Ground			Common return.	
VSS	B15	Ground			Ground for all power.	
VSS	B16	Ground				
VSS	B17	Ground				
VSS	C4	Ground				
VSS	C8	Ground				
VSS	C16	Ground				
VSS	C17	Ground				
VSS	D14	Ground				
VSS	D15	Ground				
VSS	D16	Ground				

<sup>(1)</sup> Low speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, Low Power Double Data Rate (LPDDR) JESD209B.

(2) Net trace lengths inside the package:

Relative dielectric constant for the FQK ceramic package is 9.8.

Propagation speed = 11.8 / sqrt (9.8) = 3.769 inches/ns.

Propagation delay = 0.265 ns/inch = 265 ps/inch = 10.43 ps/mm.

3) The following power supplies are all required to operate the DMD: VSS, VDD, VDDI, VOFFSET, VBIAS, VRESET.

## Table 5-2. Pin Functions – Test Pads

NUMBER	SYSTEM BOARD
A13	Do not connect
A14	Do not connect
A15	Do not connect
A16	Do not connect
A17	Do not connect
A18	Do not connect
E13	Do not connect
E14	Do not connect
E15	Do not connect
E16	Do not connect
E17	Do not connect
E18	Do not connect



## **6 Specifications**

### 6.1 Absolute Maximum Ratings

### See (1)

			MIN	MAX	UNIT
	VDD	Supply voltage for LVCMOS core logic <sup>(2)</sup> Supply voltage for LPSDR low speed interface	-0.5	2.3	V
	VDDI	Supply voltage for SubLVDS receivers <sup>(2)</sup>	-0.5	2.3	V
	VOFFSET	Supply voltage for HVCMOS and micromirror electrode <sup>(2) (3)</sup>	-0.5	11	V
Supply voltage	VBIAS	Supply voltage for micromirror electrode <sup>(2)</sup>	-0.5	19	V
	VRESET	Supply voltage for micromirror electrode <sup>(2)</sup>	-15	0.5	V
	VDDI–VDD	Supply voltage delta (absolute value) <sup>(4)</sup>		0.3	V
	VBIAS-VOFFSET	Supply voltage delta (absolute value) <sup>(5)</sup>		11	V
	VBIAS-VRESET	Supply voltage delta (absolute value) <sup>(6)</sup>		34	V
Input voltage	Input voltage for other in	puts LPSDR <sup>(2)</sup>	-0.5	VDD + 0.5	V
	Input voltage for other in	puts SubLVDS <sup>(2) (7)</sup>	-0.5	VDDI + 0.5	V
Input pipe	VID	SubLVDS input differential voltage (absolute value) <sup>(7)</sup>		810	mV
Supply voltage    Voltage	IID	SubLVDS input differential current		10	mA
Clock	$f_{clock}$	Clock frequency for low speed interface LS_CLK		130	MHz
frequency	$f_{clock}$	Clock frequency for high speed interface DCLK		560	MHz
	T and T	Temperature – operational <sup>(8)</sup>	-20	90	°C
	T <sub>ARRAY</sub> and T <sub>WINDOW</sub>	Temperature – non-operational <sup>(8)</sup>	-40	90	°C
Environmental	T <sub>DP</sub>	Dew Point Temperature - operating and non-operating (non-condensing)		81	°C
	T <sub>DELTA</sub>	Absolute Temperature delta between any point on the window edge and the ceramic test point TP1 <sup>(9)</sup>		30	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values are with respect to the ground terminals (VSS). The following power supplies are all required to operate the DMD: VSS, VDD, VDDI, VOFFSET, VBIAS, and VRESET.
- (3) VOFFSET supply transients must fall within specified voltages.
- (4) Exceeding the recommended allowable absolute voltage difference between VDDI and VDD may result in excessive current draw.
- (5) Exceeding the recommended allowable absolute voltage difference between VBIAS and VOFFSET may result in excessive current draw.
- (6) Exceeding the recommended allowable absolute voltage difference between VBIAS and VRESET may result in excessive current draw
- (7) This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. Sub-LVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
- (8) The highest temperature of the active array (as calculated in Section 7.6) or of any point along the Window Edge as defined in Figure 7-1. The locations of thermal test points TP2 and TP3 in Figure 7-1 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, that point should be used.
- (9) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in Figure 7-1. The window test points TP2 and TP3 shown in Figure 7-1 are intended to result in the worst case delta. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.

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## **6.2 Storage Conditions**

Applicable for the DMD as a component or non-operational in a system

		М	IN MAX	UNIT
T <sub>DMD</sub>	DMD storage temperature	_4	10 85	°C
T <sub>DP-AVG</sub>	Average dew point temperature, (non-condensing) <sup>(1)</sup>		24	°C
T <sub>DP-ELR</sub>	Elevated dew point temperature range, (non-condensing) <sup>(2)</sup>	2	8 36	°C
CT <sub>ELR</sub>	Cumulative time in elevated dew point temperature range		6	Months

<sup>(1)</sup> The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.

## 6.3 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V

<sup>(1)</sup> JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

## **6.4 Recommended Operating Conditions**

Over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	NOM	MAX	UNIT
SUPPLY VOLTAGE I	RANGE <sup>(3)</sup>			-	
VDD	Supply voltage for LVCMOS core logic Supply voltage for LPSDR low-speed interface	1.65	1.8	1.95	V
VDDI	Supply voltage for SubLVDS receivers	1.65	1.8	1.95	V
VOFFSET	Supply voltage for HVCMOS and micromirror electrode <sup>(4)</sup>	9.5	10	10.5	V
VBIAS	Supply voltage for mirror electrode	17.5	18	18.5	V
VRESET	Supply voltage for micromirror electrode	-14.5	-14	-13.5	V
VDDI-VDD	Supply voltage delta (absolute value) <sup>(5)</sup>			0.3	V
VBIAS-VOFFSET	Supply voltage delta (absolute value) <sup>(6)</sup>			10.5	V
VBIAS-VRESET	Supply voltage delta (absolute value) <sup>(7)</sup>			33	V
CLOCK FREQUENC	Y			'	
$f_{clock}$	Clock frequency for low speed interface LS_CLK <sup>(8)</sup>	108		120	MHz
$f_{ m clock}$	Clock frequency for high speed interface DCLK <sup>(9)</sup>	300		540	MHz
	Duty cycle distortion DCLK	44%		56%	
SUBLVDS INTERFA	CE <sup>(9)</sup>				
V <sub>ID</sub>	SubLVDS input differential voltage (absolute value) Figure 6-9, Figure 6-10	150	250	350	mV
V <sub>CM</sub>	Common mode voltage Figure 6-9, Figure 6-10	700	900	1100	mV
V <sub>SUBLVDS</sub>	SubLVDS voltage Figure 6-9, Figure 6-10	575		1225	mV
Z <sub>LINE</sub>	Line differential impedance (PWB/trace)	90	100	110	Ω
Z <sub>IN</sub>	Internal differential termination resistance Figure 6-11	80	100	120	Ω
	100-Ω differential PCB trace	6.35		152.4	mm

<sup>(2)</sup> Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT<sub>ELR</sub>.



## 6.4 Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	NOM	MAX	UNIT
ENVIRONMENTAL	L				
T <sub>ARRAY</sub>	Array Temperature – long-term operational <sup>(10)</sup> (11) (12)	0		40	
	Array Temperature - short-term operational, 25 hr max <sup>(11)</sup> (13)	-20		-10	°C
	Array Temperature - short-term operational, 500 hr max <sup>(11)</sup> (13)	-10		0	
T <sub>DELTA</sub>	Absolute Temperature difference between any point on the window edge and the ceramic test point TP1 (14)			15	°C
T <sub>WINDOW</sub>	Window temperature – operational <sup>(15)</sup>			85	°C
T <sub>DP-AVG</sub>	Average dew point temperature (non-condensing) <sup>(16)</sup>			24	°C
T <sub>DP-ELR</sub>	Elevated dew point temperature range (non-condensing)(17)	28		36	°C
CT <sub>ELR</sub>	Cumulative time in elevated dew point temperature range			6	Months
Q <sub>AP-ILL</sub>	Illumination overfill in critical areal <sup>(19)</sup> (20)			0	W/cm <sup>2</sup>
ILL <sub>UV</sub>	Illumination wavelengths < 380 nm <sup>(10)</sup>			2	mW/cm <sup>2</sup>
ILL <sub>380 - 390 nm</sub>	Illumination wavelengths between 380 nm and 390 nm			55	mW/cm <sup>2</sup>
ILL <sub>390 - 400 nm</sub>	Illumination wavelengths between 390 nm and 400 nm			450	mW/cm <sup>2</sup>
ILL <sub>400 - 550 nm</sub>	Illumination wavelengths between 400 nm and 550 nm			3	W/cm <sup>2</sup>
ILL <sub>&gt; 550 nm</sub>	Illumination wavelengths > 550 nm			10	mW/cm <sup>2</sup>
ILL <sub>θ</sub>	Illumination marginal ray angle <sup>(18)</sup>			55	deg

- (1) Section 6.4 is applicable after the DMD is installed in the final product.
- (2) The functional performance of the device specified in this datasheet is achieved when operating the device within the limits defined by Section 6.4. No level of performance is implied when operating the device above or below the Section 6.4 limits.
- (3) All voltage values are with respect to the ground pins (VSS).
- (4) VOFFSET supply transients must fall within specified maximum voltages.
- (5) To prevent excess current, the supply voltage delta |VDDI VDD| must be less than specified limit.
- (6) To prevent excess current, the supply voltage delta |VBIAS VOFFSET| must be less than specified limit.
- (7) To prevent excess current, the supply voltage delta |VBIAS VRESET| must be less than specified limit.
- (8) LS\_CLK must run as specified to ensure internal DMD timing for reset waveform commands.
- (9) Refer to the SubLVDS timing requirements in Section 6.7.
- (10) Simultaneous exposure of the DMD to the maximum limits in Section 6.4 for temperature and UV illumination will reduce device lifetime.
- (11) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in Figure 7-1 and the Package Thermal Resistance using Section 7.6.
- (12) Long-term is defined as the usable life of the device.
- (13) Short-term is the total cumulative time over the useful life of the device.
- (14) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge shown in Figure 7-1. The window test points TP2 and TP3 shown in Figure 7-1 are intended to result in the worst case delta temperature. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.
- (15) Window temperature is the highest temperature on the window edge shown in Figure 7-1. The locations of thermal test points TP2 and TP3 in Figure 7-1 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to result in a higher temperature, that point should be used.
- (16) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
- (17) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT<sub>ELR</sub>.
- (18) The maximum marginal ray angle of the incoming illumination light at any point in the micromirror array, including Pond of Micromirrors (POM), should not exceed 55 degrees from the normal to the device array plane. The device window aperture has not necessarily been designed to allow incoming light at higher maximum angles to pass to the micromirrors, and the device performance has not been tested nor qualified at angles exceeding this. Illumination light exceeding this angle outside the micromirror array (including POM) will contribute to thermal limitations described in this document, and may negatively affect lifetime.
- (19) The active area of the device is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The window aperture is sized to anticipate several optical operating conditions. Overfill light directly illuminating the window aperture can create adverse imaging effects, and additional device heating leading to reduced device lifetime. Direct incident illumination should be prevented from striking the DMD window aperture.
- (20) Applies to the region in red in Figure 6-1, at the inside plane of the glass window where the physical aperture is located.

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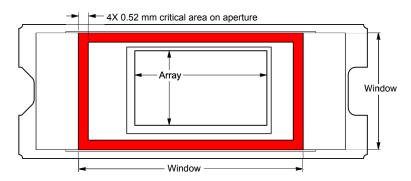


Figure 6-1. Illumination Overfill Diagram - Critical Area

#### 6.5 Thermal Information

		DLP300S	
	THERMAL METRIC <sup>(1)</sup>	FQK (LGA)	UNIT
		57 PINS	
Thermal resistance	Active area to test point 1 (TP1) <sup>(1)</sup>	5.4	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the Section 6.4. The total heat load on the DMD is largely driven by the incident light absorbed by the active area although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

### **6.6 Electrical Characteristics**

Over operating free-air temperature range (unless otherwise noted)(10)

	PARAMETER	TEST CONDITIONS(2)	MIN	TYP	MAX	UNIT
CURRENT	Г					
	Complete company (DD(3) (5)	VDD = 1.95 V			60.5	Л
I <sub>DD</sub>	Supply current: VDD <sup>(3) (5)</sup>	VDD = 1.8 V		54		mA
	Complete company (100) (5)	VDDI = 1.95 V			16.5	Л
I <sub>DDI</sub>	Supply current: VDDI <sup>(3)</sup> (5)	VDD = 1.8 V		11.3		mA
	O 1 VOFFOFT(4) (6)	VOFFSET = 10.5 V			2.2	4
I <sub>OFFSET</sub>	Supply current: VOFFSET <sup>(4)</sup> (6)	VOFFSET = 10 V		1.5		mA
	O	VBIAS = 18.5 V			0.6	1
I <sub>BIAS</sub>	Supply current: VBIAS <sup>(4)</sup> (6)	VBIAS = 18 V		0.3		mA
	Owner to American American	VRESET = -14.5 V			2.4	4
I <sub>RESET</sub>	Supply current: VRESET <sup>(6)</sup>	VRESET = -14 V		1.7		mA
POWER <sup>(1)</sup>	)					
_	O	VDD = 1.95 V			118	\^/
P <sub>DD</sub>	Supply power dissipation: VDD <sup>(3) (5)</sup>	VDD = 1.8 V		95		mW
_	O	VDDI = 1.95 V			32	\^/
P <sub>DDI</sub>	Supply power dissipation: VDDI <sup>(3)</sup> (5)	VDD = 1.8 V		20		mW
_	Supply power dissipation:	VOFFSET = 10.5 V			23	\^/
P <sub>OFFSET</sub>	VOFFSET <sup>(4)</sup> (6)	VOFFSET = 10 V		15		mW
_	O	VBIAS = 18.5 V			11	\^/
P <sub>BIAS</sub>	Supply power dissipation: VBIAS <sup>(4)</sup> (6)	VBIAS = 18 V		6		mW
_	Owner to a second disciplation (ADEOFT(6))	VRESET = -14.5 V		,	35	\^/
P <sub>RESET</sub>	Supply power dissipation: VRESET <sup>(6)</sup>	VRESET = -14 V		24		mW
P <sub>TOTAL</sub>	Supply power dissipation: Total			160	219	mW



### **6.6 Electrical Characteristics (continued)**

Over operating free-air temperature range (unless otherwise noted)(10)

	PARAMETER	TEST CONDITIONS <sup>(2)</sup>	MIN	TYP MAX	UNIT
LPSDR IN	PUT <sup>(7)</sup>				
V <sub>IH(DC)</sub>	DC input high voltage <sup>(9)</sup>		0.7 × VDD	VDD + 0.3	V
V <sub>IL(DC)</sub>	DC input low voltage <sup>(9)</sup>		-0.3	0.3 × VDD	V
V <sub>IH(AC)</sub>	AC input high voltage <sup>(9)</sup>		0.8 × VDD	VDD + 0.3	V
V <sub>IL(AC)</sub>	AC input low voltage <sup>(9)</sup>		-0.3	0.2 × VDD	V
$\Delta V_T$	Hysteresis ( V <sub>T+</sub> – V <sub>T-</sub> )	Figure 6-12	0.1 × VDD	0.4 × VDD	V
I <sub>IL</sub>	Low-level input current	VDD = 1.95 V; V <sub>I</sub> = 0 V	-100		nA
I <sub>IH</sub>	High-level input current	VDD = 1.95 V; V <sub>I</sub> = 1.95 V		100	nA
LPSDR O	UTPUT <sup>(8)</sup>				
V <sub>OH</sub>	DC output high voltage	I <sub>OH</sub> = -2 mA	0.8 × VDD		V
V <sub>OL</sub>	DC output low voltage	I <sub>OL</sub> = 2 mA		0.2 × VDD	V
CAPACITA	ANCE				
_	Input capacitance LPSDR	f = 1 MHz		10	pF
C <sub>IN</sub>	Input capacitance SubLVDS	f = 1 MHz		10	pF
C <sub>OUT</sub>	Output capacitance	f = 1 MHz		10	pF

- The following power supplies are all required to operate the DMD: VSS, VDD, VDDI, VOFFSET, VBIAS, VRESET.
- (2)
- (3)
- All voltage values are with respect to the ground pins (VSS).

  To prevent excess current, the supply voltage delta |VDDI VDD| must be less than specified limit.

  To prevent excess current, the supply voltage delta |VBIAS VOFFSET| must be less than specified limit.
- Supply power dissipation based on non-compressed commands and data. (5)
- Supply power dissipation based on 3 global resets in 200 µs.
- LPSDR specifications are for pins LS CLK and LS WDATA.
- LPSDR specification is for pin LS\_RDATA.
- Low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, Low-Power Double Data Rate (LPDDR) JESD209B.
- (10) Device electrical characteristics are over Section 6.4 unless otherwise noted.

### 6.7 Timing Requirements

Device electrical characteristics are over Section 6.4 unless otherwise noted.

			MIN	NOM	MAX	UNIT
LPSDR					'	
t <sub>r</sub>	Rise slew rate <sup>(1)</sup>	(30% to 80%) × VDD, Figure 6-3	1		3	V/ns
$t_f$	Fall slew rate <sup>(1)</sup>	(70% to 20%) × VDD, Figure 6-3	1		3	V/ns
t <sub>r</sub>	Rise slew rate <sup>(2)</sup>	(20% to 80%) × VDD, Figure 6-4	0.25			V/ns
$t_f$	Fall slew rate <sup>(2)</sup>	(80% to 20%) × VDD, Figure 6-4	0.25			V/ns
t <sub>c</sub>	Cycle time LS_CLK,	Figure 6-2	7.7	8.3		ns
t <sub>W(H)</sub>	Pulse duration LS_CLK high	50% to 50% reference points, Figure 6-2	3.1			ns
t <sub>W(L)</sub>	Pulse duration LS_CLK low	50% to 50% reference points, Figure 6-2	3.1			ns
t <sub>su</sub>	Setup time	LS_WDATA valid before LS_CLK ↑, Figure 6-2	1.5			ns
t <sub>h</sub>	Hold time	LS_WDATA valid after LS_CLK ↑, Figure 6-2	1.5			ns
t <sub>WINDOW</sub>	Window time <sup>(1) (4)</sup>	Setup time + Hold time, Figure 6-2	3			ns
t <sub>DERATING</sub>	Window time derating <sup>(1) (4)</sup>	For each 0.25 V/ns reduction in slew rate below 1 V/ns, Figure 6-6		0.35		ns
SubLVDS			1			

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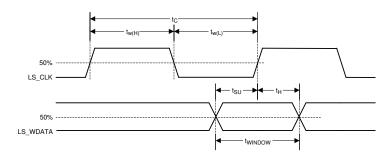
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## 6.7 Timing Requirements (continued)

Device electrical characteristics are over Section 6.4 unless otherwise noted.

			MIN	NOM	MAX	UNIT
t <sub>r</sub>	Rise slew rate	20% to 80% reference points, Figure 6-5	0.7	1		V/ns
$t_f$	Fall slew rate	80% to 20% reference points, Figure 6-5	0.7	1		V/ns
t <sub>c</sub>	Cycle time DCLK,	Figure 6-7	1.79	1.85		ns
t <sub>W(H)</sub>	Pulse duration DCLK high	50% to 50% reference points, Figure 6-7	0.79			ns
t <sub>W(L)</sub>	Pulse duration DCLK low	50% to 50% reference points, Figure 6-7	0.79			ns
t <sub>su</sub>	Setup time	D(0:3) valid before DCLK ↑ or DCLK ↓, Figure 6-7				
t <sub>h</sub>	Hold time	D(0:3) valid after DCLK ↑ or DCLK ↓, Figure 6-7				
t <sub>WINDOW</sub>	Window time	Setup time + Hold time, Figure 6-7, Figure 6-8			0.3	ns
t <sub>LVDS-</sub> ENABLE+REFGEN	Power-up receiver <sup>(3)</sup>				2000	ns

- (1) Specification is for LS\_CLK and LS\_WDATA pins. Refer to LPSDR input rise slew rate and fall slew rate in Figure 6-3.
- (2) Specification is for DMD\_DEN\_ARSTZ pin. Refer to LPSDR input rise and fall slew rate in Figure 6-4.
- (3) Specification is for SubLVDS receiver time only and does not take into account commanding and latency after commanding.
- (4) Window time derating example: 0.5-V/ns slew rate increases the window time by 0.7 ns, from 3 to 3.7 ns.



Low-speed interface is LPSDR and adheres to the Section 6.6 and AC/DC Operating Conditions table in JEDEC Standard No. 209B, Low Power Double Data Rate (LPDDR) JESD209B.

Figure 6-2. LPSDR Switching Parameters

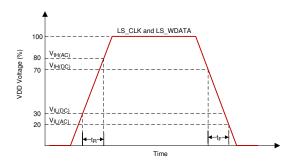


Figure 6-3. LPSDR Input Slew Rate



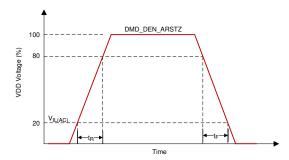


Figure 6-4. LPSDR Input Slew Rate

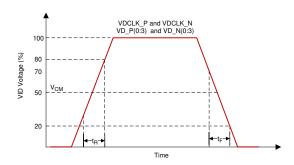
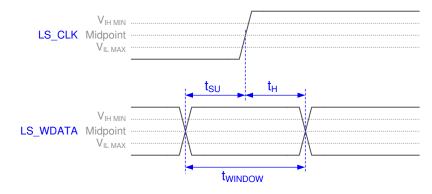


Figure 6-5. SubLVDS Input Rise and Fall Slew Rate



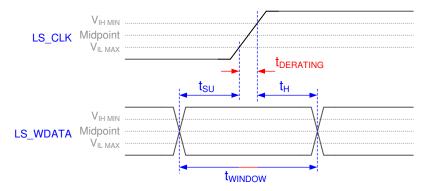


Figure 6-6. Window Time Derating Concept

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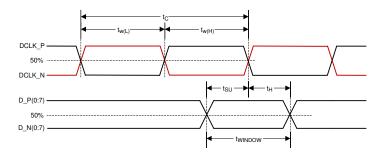
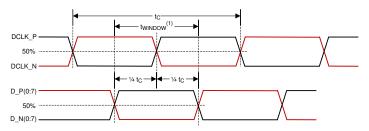


Figure 6-7. SubLVDS Switching Parameters



- (1) High-speed training scan window
- (2) Refer to Section 7.3.3 for details

Figure 6-8. High-Speed Training Scan Window

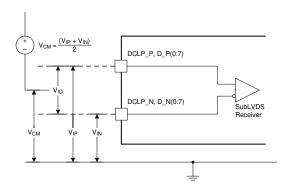


Figure 6-9. SubLVDS Voltage Parameters

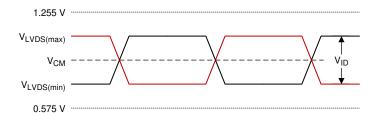


Figure 6-10. SubLVDS Waveform Parameters

$$V_{SubLVDS(max)} = V_{CM(max)} + \frac{1}{2} \times |V_{ID(max)}|$$

$$V_{SubLVDS(min)} = V_{CM(min)} - \frac{1}{2} \times |V_{ID(max)}|$$



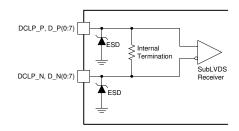


Figure 6-11. SubLVDS Equivalent Input Circuit

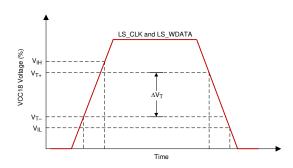


Figure 6-12. LPSDR Input Hysteresis

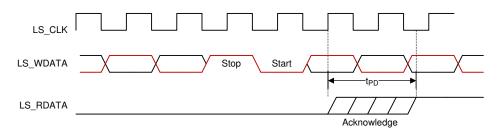
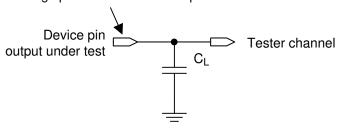


Figure 6-13. LPSDR Read Out

Timing specification reference point



See Section 7.3.4 for more information.

Figure 6-14. Test Load Circuit for Output Propagation Measurement

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## 6.8 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted).(1)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output propagation, Clock to Q, rising edge of LS_CLK input to LS_RDATA output. Figure 6-13	Output propagation, Clock to Q, rising	C <sub>L</sub> = 5 pF			11.1	ns
	C <sub>L</sub> = 10 pF			11.3	ns	
	output. Figure 6-13	C <sub>L</sub> = 85 pF			15	ns
	Slew rate, LS_RDATA		0.5			V/ns
	Output duty cycle distortion, LS_RDATA		40%	-	60%	

<sup>(1)</sup> Device electrical characteristics are over Section 6.4 unless otherwise noted.

## 6.9 System Mounting Interface Loads

PARAMETER		MIN	NOM	MAX	UNIT
, ,	Electrical Interface Area (see Figure 6-15)			125	N
	Clamping and Thermal Interface Area (see Figure 6-15)			67	N

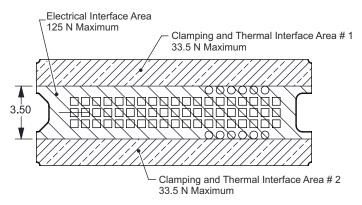


Figure 6-15. System Interface Loads



## **6.10 Micromirror Array Physical Characteristics**

	PARAMETER			UNIT
	Number of active columns	See Figure 6-16	1280	micromirrors
	Number of active rows	See Figure 6-16	720	micromirrors
ε	Micromirror (pixel) pitch	See Figure 6-17	5.4	μm
	Micromirror active array width	Micromirror pitch × number of active columns; see Figure 6-16	6.912	mm
	Micromirror active array height	Micromirror pitch × number of active rows; see Figure 6-16	3.888	mm
	Micromirror active border	Pond of micromirror (POM) <sup>(1)</sup>	20	micromirrors/ side

(1) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the POM. These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.

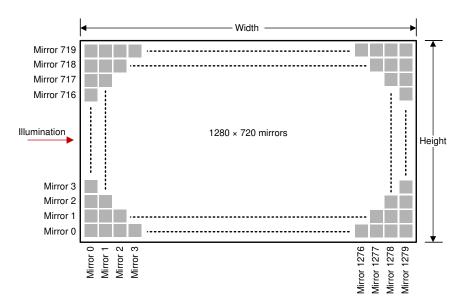


Figure 6-16. Micromirror Array Physical Characteristics

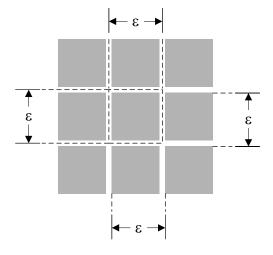


Figure 6-17. Mirror (Pixel) Pitch



### 6.11 Micromirror Array Optical Characteristics

ı	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Micromirror tilt ang	le	DMD landed state <sup>(1)</sup>		17		degree
Micromirror tilt ang	le tolerance <sup>(2) (3) (4) (5)</sup>		-1.4		1.4	degree
Micromirror tilt dira	otion (6) (7)	Landed ON state		180		dograe
Micromirror tilt direction (6) (7)		Landed OFF state		270		degree
Micromirror crosso	ver time <sup>(8)</sup>	Typical performance		1	3	
Micromirror switchi	ng time <sup>(9)</sup>	Typical performance	10			μs
	Bright pixel(s) in active area	Gray 10 Screen (12)			0	
	Bright pixel(s) in the POM (13)	Gray 10 Screen (12)			1	
Image performance <sup>(10)</sup>	Dark pixel(s) in the active area (14)	White Screen			4	micromirrors
	Adjacent pixel(s) (15)	Any Screen			0	
	Unstable pixel(s) in active area (16)	Any Screen			0	

- (1) Measured relative to the plane formed by the overall micromirror array.
- (2) Additional variation exists between the micromirror array and the package datums.
- (3) Represents the landed tilt angle variation relative to the nominal landed tilt angle.
- (4) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
- (5) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations, or system contrast variations.
- (6) When the micromirror array is landed (not parked), the tilt direction of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in the ON state direction. A binary value of 0 results in a micromirror landing in the OFF state direction. See Figure 6-18.
- (7) Micromirror tilt direction is measured as in a typical polar coordinate system: Measuring counter-clockwise from a 0° reference which is aligned with the +X Cartesian axis.
- (8) The time required for a micromirror to nominally transition from one landed state to the opposite landed state.
- (9) The minimum time between successive transitions of a micromirror.
- (10) Conditions of Acceptance: All DMD image quality returns will be evaluated using the following projected image test conditions:

Test set degamma shall be linear

Test set brightness and contrast shall be set to nominal

The diagonal size of the projected image shall be a minimum of 20 inches

The projections screen shall be 1X gain

The projected image shall be inspected from a 38 inch minimum viewing distance

The image shall be in focus during all image quality tests

- (11) Bright pixel definition: A single pixel or mirror that is stuck in the ON position and is visibly brighter than the surrounding pixels
- (12) Gray 10 screen definition: All areas of the screen are colored with the following settings:

Red = 10/255

Green = 10/255

Blue = 10/255

- (13) POM definition: Rectangular border of off-state mirrors surrounding the active area
- (14) Dark pixel definition: A single pixel or mirror that is stuck in the OFF position and is visibly darker than the surrounding pixels
- (15) Adjacent pixel definition: Two or more stuck pixels sharing a common border or common point, also referred to as a cluster
- (16) Unstable pixel definition: A single pixel or mirror that does not operate in sequence with parameters loaded into memory. The unstable pixel appears to be flickering asynchronously with the image



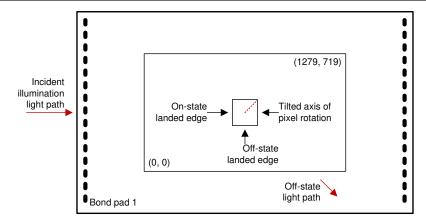


Figure 6-18. Landed Pixel Orientation and Tilt



#### 6.12 Window Characteristics

PARAMETER <sup>(3)</sup>		MIN	TYP	MAX	UNIT
Window material			Corning Eagle XG		
Window aperture <sup>(1)</sup>				See (1)	
Illumination overfill <sup>(2)</sup>				See (2)	
Window transmittance, single-pass through both surfaces and glass (4)	Minimum within the wavelength range 390 nm to 450 nm, 0-30° AOI.	93%	99%		
	Average within the wavelength range 390 nm to 450 nm, 0-30° AOI.	98%	99%		
	Minimum within the wavelength range 450 nm to 550 nm. 0-30° AOI.	75%	90%		

- (1) See the package mechanical characteristics for details regarding the size and location of the window aperture.
- (2) The active area of the device is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The window aperture is sized to anticipate several optical operating conditions. Overfill light directly illuminating the window aperture can create adverse imaging effects, and additional device heating leading to reduced device lifetime. Direct incident illumination should be prevented from striking the DMD window aperture.
- (3) See <u>Section</u> 7.5 for more information.
- (4) See the TI application report DLPA031, Wavelength Transmittance Considerations for DLP DMD Window.

## 6.13 Chipset Component Usage Specification

The DLP300S is a component of one or more TI DLP® chipsets. Reliable function and operation of the DLP300S requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology is the TI technology and devices for operating or controlling a DLP DMD.

#### Note

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

#### 6.14 Software Requirements

#### **CAUTION**

The DMD has mandatory software requirements. Refer to *Software Requirements for TI DLP®Pico® TRP Digital Micromirror Devices* application report for additional information. Failure to use the specified software results in failure at power up.



## 7 Detailed Description

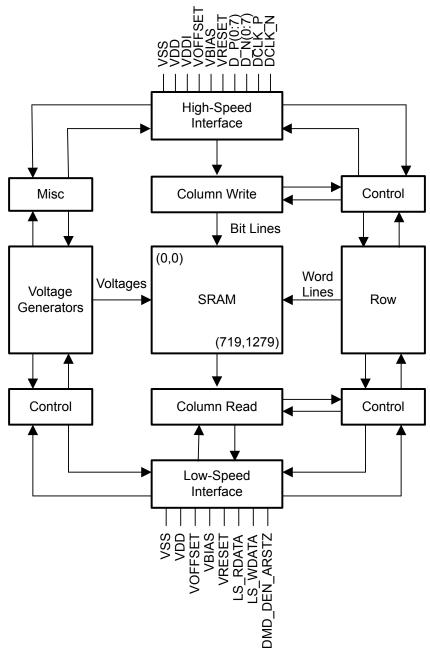
### 7.1 Overview

The DLP300S DMD is a 0.3 inch diagonal spatial light modulator of aluminum micromirrors. Pixel array size is 1280 columns by 720 rows in a square grid pixel arrangement. The fast switching speed of the DMD micromirrors combined with advanced DLP image processing algorithms enable each micromirror to display 4 distinct pixels on the screen during every frame, resulting in a full 3.6MP image being displayed. The electrical interface is Sub Low Voltage Differential Signaling (SubLVDS) data.

This DMD is part of the chipset that includes the DLP300S DMD, DLPC1438 display and light controller and DLPA200x PMIC/LED driver. To ensure reliable operation, this DMD must always be used with DLPC1438 display and light controller and DLPA200x PMIC/LED driver.



# 7.2 Functional Block Diagram



- A. Details omitted for clarity
- B. Orientation is not representative of optical system
- C. Scale is not representative of layout



### 7.3 Feature Description

#### 7.3.1 Power Interface

The power management IC, DLPA200x, contains 3 regulated DC supplies for the DMD reset circuitry: VBIAS, VRESET and VOFFSET, as well as the 2 regulated DC supplies for the DLPC1438 controller.

### 7.3.2 Low-Speed Interface

The Low Speed Interface handles instructions that configure the DMD and control reset operation. LS\_CLK is the low–speed clock, and LS\_WDATA is the low speed data input.

### 7.3.3 High-Speed Interface

The purpose of the high-speed interface is to transfer pixel data rapidly and efficiently, making use of high speed DDR transfer and compression techniques to save power and time. The high-speed interface is composed of differential SubLVDS receivers for inputs, with a dedicated clock.

#### **7.3.4 Timing**

The data sheet provides timing test results at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be considered. The Test Load Circuit Output Propagation Measurement shows an equivalent test load circuit for the output under test. Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. TI recommends that system designers use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is intended for characterization and measurement of AC timing signals only. This load capacitance value does not indicate the maximum load the device is capable of driving.

#### 7.4 Device Functional Modes

DMD functional modes are controlled by the DLPC1438 controller. See the DLPC1438 controller data sheet or contact a TI applications engineer.

### 7.5 Optical Interface and System Image Quality Considerations

#### Note

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

#### 7.5.1 Optical Interface and System Image Quality

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

## 7.5.1.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area is typically the same. Ensure this angle does not exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination or projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle (and vice versa), contrast degradation and objectionable artifacts in the display border or active area may occur.

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#### 7.5.1.2 Pupil Match

The optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display border or active area. These artifacts may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

#### 7.5.1.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The window aperture is sized to anticipate several optical operating conditions. Overfill light directly illuminating the window aperture can create adverse imaging effects, and additional device heating leading to reduced device lifetime. Direct incident illumination should be prevented from striking the DMD window aperture.

## 7.6 Micromirror Array Temperature Calculation

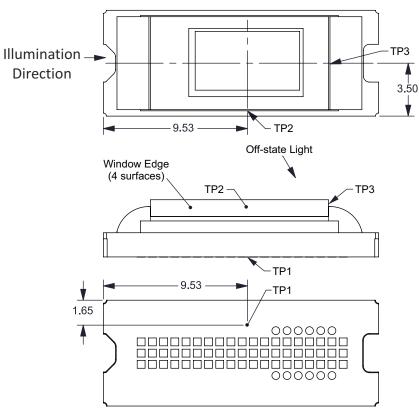


Figure 7-1. Thermal Test Point Location - FQK Package

Micromirror array temperature cannot be measured directly, therefore it must be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The relationship between array temperature and the reference ceramic temperature shown as TP1 in Figure 7-1 is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY-TO-CERAMIC})$$
 (1)

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION}$$
 (2)

#### where

- T<sub>ARRAY</sub> = Computed micromirror array temperature (°C)
- T<sub>CFRAMIC</sub> = Measured ceramic temperature (°C) (TP1 location)



- R<sub>ARRAY-TO-CERAMIC</sub> = Thermal resistance of package specified in Section 6.5 from array to ceramic TP1 (°C/W)
- Q<sub>ARRAY</sub> = Total DMD power on the array (electrical + absorbed) (W)
- Q<sub>ELECTRICAL</sub> = Nominal electrical power (W)
- Q<sub>INCIDENT</sub> = measured total illumination optical power at DMD (W)
- Q<sub>ILLUMINATION</sub> = (Q<sub>INCIDENT</sub> × DMD average thermal absortivity) (W)
- DMD average thermal absortivity = 0.40

. . . . . .

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 0.1 W. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for each DMD chip in a system. It assumes illumination distribution of 83.7% on the active array and 16.3% on the area outside the array.

Q <sub>ELECTRICAL</sub> = 0.1 W	(3)

$$Q_{INCIDENT} = 0.9 \text{ W (measured)}$$
 (4)

$$T_{CERAMIC} = 35.0 \,^{\circ}C \, (measured)$$
 (5)

$$Q_{ARRAY} = 0.1 \text{ W} + (0.9 \text{ W} \times 0.40) = 0.46 \text{ W}$$
 (6)

$$T_{ARRAY} = 35.0 \text{ °C} + (0.46 \text{ W x } 5.4 \text{ °C /W}) = 37.5 \text{ °C}$$
 (7)

## 7.7 Micromirror Landed-On/Landed-Off Duty Cycle

### 7.7.1 Definition of Micromirror Landed-On and Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

As an example, a landed duty cycle of 75/25 indicates that the referenced pixel is in the ON state 75% of the time (and in the OFF state 25% of the time), whereas 25/75 indicates that the pixel is in the OFF state 75% of the time. Likewise, 50/50 indicates that the pixel is ON 50% of the time and OFF 50% of the time.

When assessing landed duty cycle, the time spent switching from the current state to the opposite state is considered negligible and is thus ignored.

Because a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) nominally add to 100. In practice, image processing algorithms in the DLP chipset can result a total of less that 100.

### 7.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the usable life of the DMD.

The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

### 7.7.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD temperature and landed duty cycle interact to affect the usable life of the DMD. This interaction can be used to reduce the impact that an asymmetrical landed duty cycle has on the useable life of the DMD.

#### 7.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the landed duty cycle of a given pixel depends on the image content being displayed by that pixel. To enhance reliability, when coupled with the DLPC1438 controller, the DLP300S DMD operates at a maximum 78/22 duty cycle and a minimum of 22/78 duty cycle.

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In the simplest case for example, when the system displays maximum full scale brightness on a given pixel for a given time period, that pixel operates very close to a 78/22 landed duty cycle during that time period. Likewise, when the system displays a pixel value of zero, the pixel operates very close to a 22/78 landed duty cycle.

The nominal landed duty cycle is additionally biased from the worst case above toward 50/50 during the time between print layers. The duty cycle approaches 50/50 when the illuminated print time is the same as the between layer time.



## 8 Application and Implementation

#### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

The DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application depends primarily on the optical architecture of the system and format of the data coming into the DLPC1438 controller. Applications include:

- DLP 3D Printer
  - Additive manufacturing
  - Vat polymerization
  - Masked stereolithography (mSLA 3D printer)
- · Light exposure: programmable spatial and temporal light exposure

DMD power-up and power-down sequencing is strictly controlled by the DLPA2000/DLPA2005. Refer to *Section* 9 for power-up and power-down specifications. For reliable operation, the DLP300S DMD must be used with the DLPC1438 controller and DLPA2000/DLPA2005 PMIC/LED driver.

### 8.2 Typical Application

Figure 8-1 and Figure 8-2 show typical DLP 3D printer system block diagrams using the DLP300S DMD, DLPC1438 controller, and DLPA200x PMIC/LED driver.

Product Folder Links: DLP300S

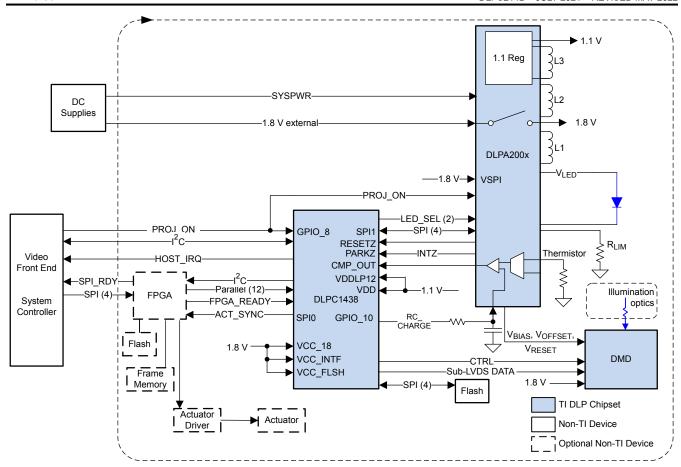


Figure 8-1. With FPGA



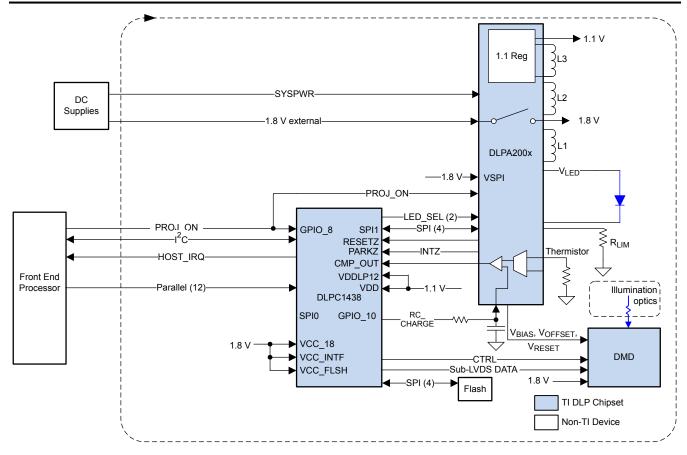


Figure 8-2. Without FPGA

#### 8.2.1 Design Requirements

A DLP 3D printer can be created using the DLP300S, DLPC1438, and DLPA200x PMIC/LED driver. In addition to the DLP chipset, other IC components may be needed including a flash device to store the software and firmware to control the DLPC1438.

A 405nm LED typically supplies the illumination for the DMD. In addition to LEDs, other light sources are supported.

### 8.2.2 Detailed Design Procedure

The optical engine, which includes the LED, DMD, and sometimes the electronics is typically supplied by an optical OEM who specializes in designing optics for DLP projectors.

#### 8.2.3 Application Curve

This device drives current though the LED(s). As the LED current increases, the brightness of the optical engine increases. This increase is somewhat non-linear, and the curve for typical optical output power changes with LED currents as shown in Figure 8-3.

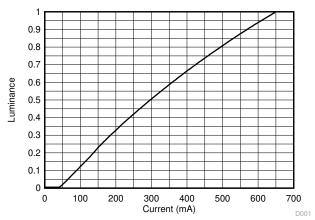


Figure 8-3. Optical Output vs LED Current



## 9 Power Supply Recommendations

The following power supplies are all required to operate the DMD:

- V<sub>SS</sub>
- V<sub>BIAS</sub>
- V<sub>DD</sub>
- V<sub>DDI</sub>
- V<sub>OFFSET</sub>
- V<sub>RESET</sub>

DMD power-up and power-down sequencing is strictly controlled by the DLPAxxxx device.

#### CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to any of the prescribed power-up and power-down requirements may affect device reliability. See the DMD power supply sequencing requirements in Figure 9-1.

 $V_{BIAS}$ ,  $V_{DD}$ ,  $V_{DDI}$ ,  $V_{OFFSET}$ , and  $V_{RESET}$  power supplies must be coordinated during power-up and power-down operations. Failure to meet any of the below requirements significantly reduces DMD reliability and lifetime. Common ground  $V_{SS}$  must also be connected.

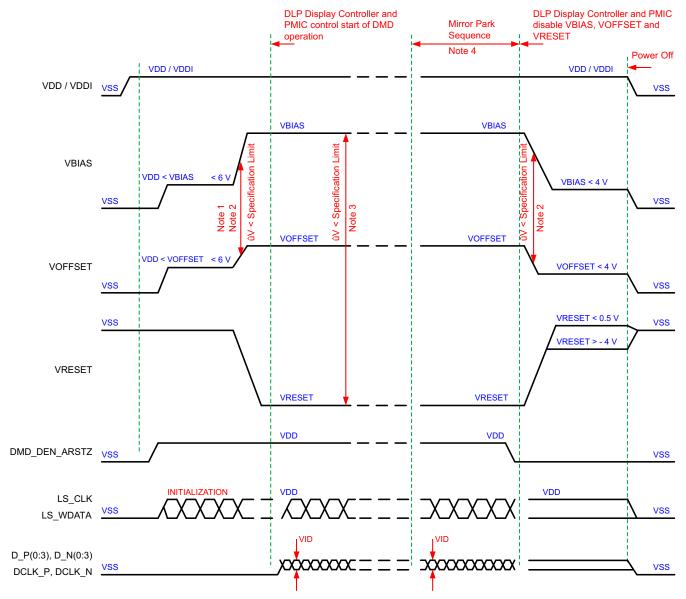
### 9.1 DMD Power Supply Power-Up Procedure

- During power-up, V<sub>DD</sub> and V<sub>DDI</sub> must always start and settle before V<sub>OFFSET</sub>, V<sub>BIAS</sub>, and V<sub>RESET</sub> voltages are applied to the DMD.
- During power-up, it is a strict requirement that the voltage difference between V<sub>BIAS</sub> and V<sub>OFFSET</sub> must be within the specified limit shown in Section 6.4. Refer to Table 9-1 for power-up delay requirements.
- During power-up, there is no requirement for the relative timing of V<sub>RESET</sub> with respect to V<sub>BIAS</sub> and V<sub>OFFSET</sub>.
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements specified in Section 6.1, in Section 6.4, and in Section 9.3.
- During power-up, LPSDR input pins must not be driven high until after V<sub>DD</sub> /V<sub>DDI</sub> have settled at operating voltages listed in Section 6.4.

### 9.2 DMD Power Supply Power-Down Procedure

- Power-down sequence is the reverse order of the previous power-up sequence. During power-down, V<sub>DD</sub> and V<sub>DDI</sub> must be supplied until after V<sub>BIAS</sub>, V<sub>RESET</sub>, and V<sub>OFFSET</sub> are discharged to within 4 V of ground.
- During power-down, it is a strict requirement that the voltage difference between V<sub>BIAS</sub> and V<sub>OFFSET</sub> must be within the specified limit shown in Section 6.4.
- During power-down, there is no requirement for the relative timing of V<sub>RESET</sub> with respect to V<sub>BIAS</sub> and V<sub>OFFSET</sub>.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements specified in Section 6.1, in Section 6.4, and in Section 9.3.
- During power-down, LPSDR input pins must be less than V<sub>DD</sub> /V<sub>DDI</sub> specified in Section 6.4.

## 9.3 Power Supply Sequencing Requirements



- A. Refer to Table 9-1 and Figure 9-2 for critical power-up sequence delay requirements.
- B. To prevent excess current, the supply voltage delta |V<sub>BIAS</sub> V<sub>OFFSET</sub>| must be less than specified in Section 6.4. OEMs may find that the most reliable way to ensure this is to power V<sub>OFFSET</sub> prior to V<sub>BIAS</sub> during power-up and to remove V<sub>BIAS</sub> prior to V<sub>OFFSET</sub> during power-down. Refer to Table 9-1 and Figure 9-2 for power-up delay requirements.
- C. To prevent excess current, the supply voltage delta |V<sub>BIAS</sub> V<sub>RESET</sub>| must be less than specified limit shown in Section 6.4.
- D. When system power is interrupted, the ASIC driver initiates hardware power-down that disables V<sub>BIAS</sub>, V<sub>RESET</sub> and V<sub>OFFSET</sub> after the Micromirror Park Sequence. Software power-down disables V<sub>BIAS</sub>, V<sub>RESET</sub>, and V<sub>OFFSET</sub> after the Micromirror Park Sequence through software control.
- Drawing is not to scale and details are omitted for clarity.

Figure 9-1. Power Supply Sequencing Requirements (Power Up and Power Down)

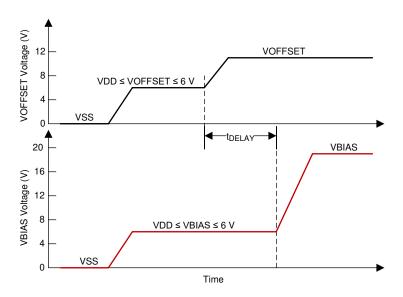
Table 9-1. Power-Up Sequence Delay Requirement

PARAMETER		MIN	MAX	UNIT
t <sub>DELAY</sub>	Delay requirement from V <sub>OFFSET</sub> power up to V <sub>BIAS</sub> power up	2		ms
V <sub>OFFSET</sub>	Supply voltage level during power–up sequence delay (see Figure 9-2)		6	V



Table 9-1. Power-Up Sequence Delay Requirement (continued)

	PARAMETER	MIN MAX	UNIT
V <sub>BIAS</sub>	Supply voltage level during power–up sequence delay (see Figure 9-2)	6	V



A. Refer to Table 9-1 for  $V_{OFFSET}$  and  $V_{BIAS}$  supply voltage levels during power-up sequence delay.

Figure 9-2. Power-Up Sequence Delay Requirement

## 10 Layout

## 10.1 Layout Guidelines

There are no specific layout guidelines for the DMD as typically DMD is connected using a board to board connector to a flex cable. Flex cable provides the interface of data and control signals between the DLPC1438 controller and the DLP300S DMD. For detailed layout guidelines refer to the layout design files. Some layout guideline for the flex cable interface with DMD are:

- Match lengths for the LS\_WDATA and LS\_CLK signals.
- Minimize vias, layer changes, and turns for the HS bus signals. Refer Figure 10-1.
- Minimum of two 100-nF decoupling capacitor close to VBIAS. Capacitor C6 and C7 in Figure 10-1.
- Minimum of two 100-nF decoupling capacitor close to VRST. Capacitor C9 and C8 in Figure 10-1.
- Minimum of two 220-nF decoupling capacitor close to VOFS. Capacitor C5 and C4 in Figure 10-1.
- Minimum of four 100-nF decoupling capacitor close to VDDI and VDD. Capacitor C1, C2, C3 and C10 in Figure 10-1.

## 10.2 Layout Example

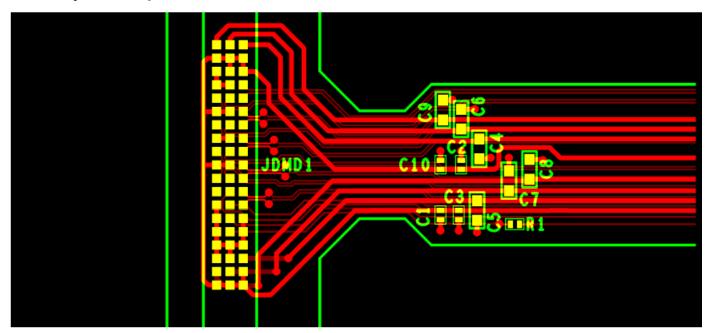


Figure 10-1. Power Supply Connections



## 11 Device and Documentation Support

### 11.1 Device Support

## 11.1.1 Third-Party Products Disclaimer

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#### 11.1.2 Device Nomenclature

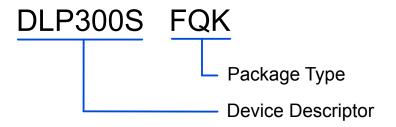


Figure 11-1. Part Number Description

### 11.1.3 Device Markings

The device marking includes the legible character string GHJJJJK DLP300SFQK. GHJJJJK is the lot trace code. DLP300SFQK is the orderable device number.

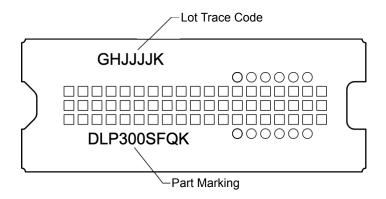


Figure 11-2. DMD Marking

## 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 11.3 Related Links

Table 11-1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 11-1. Related Links

APTS PRODUCT FOLDER SAMPLE & PLIX TECHNICAL

PARTS	PRODUCT FOLDER	SAMPLE & BUY TECHNICAL DOCUMENTS		TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DLP300S	Click here	Click here	Click here	Click here	Click here

Submit Document Feedback

Table 11-1. Related Links (continued)

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY	
DLPC1438	Click here	Click here	Click here	Click here	Click here	
DLPA2000	Click here	Click here	Click here	Click here	Click here	
DLPA2005	Click here	Click here	Click here	Click here	Click here	

### 11.4 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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### 11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.7 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

www.ti.com 9-Nov-2025

#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
DLP300SFQK	Active	Production	CLGA (FQK)   57	120   JEDEC TRAY (5+1)	Yes	NIAU	N/A for Pkg Type	0 to 40	
DLP300SFQK.B	Active	Production	CLGA (FQK)   57	120   JEDEC TRAY (5+1)	Yes	NIAU	N/A for Pkg Type	0 to 40	

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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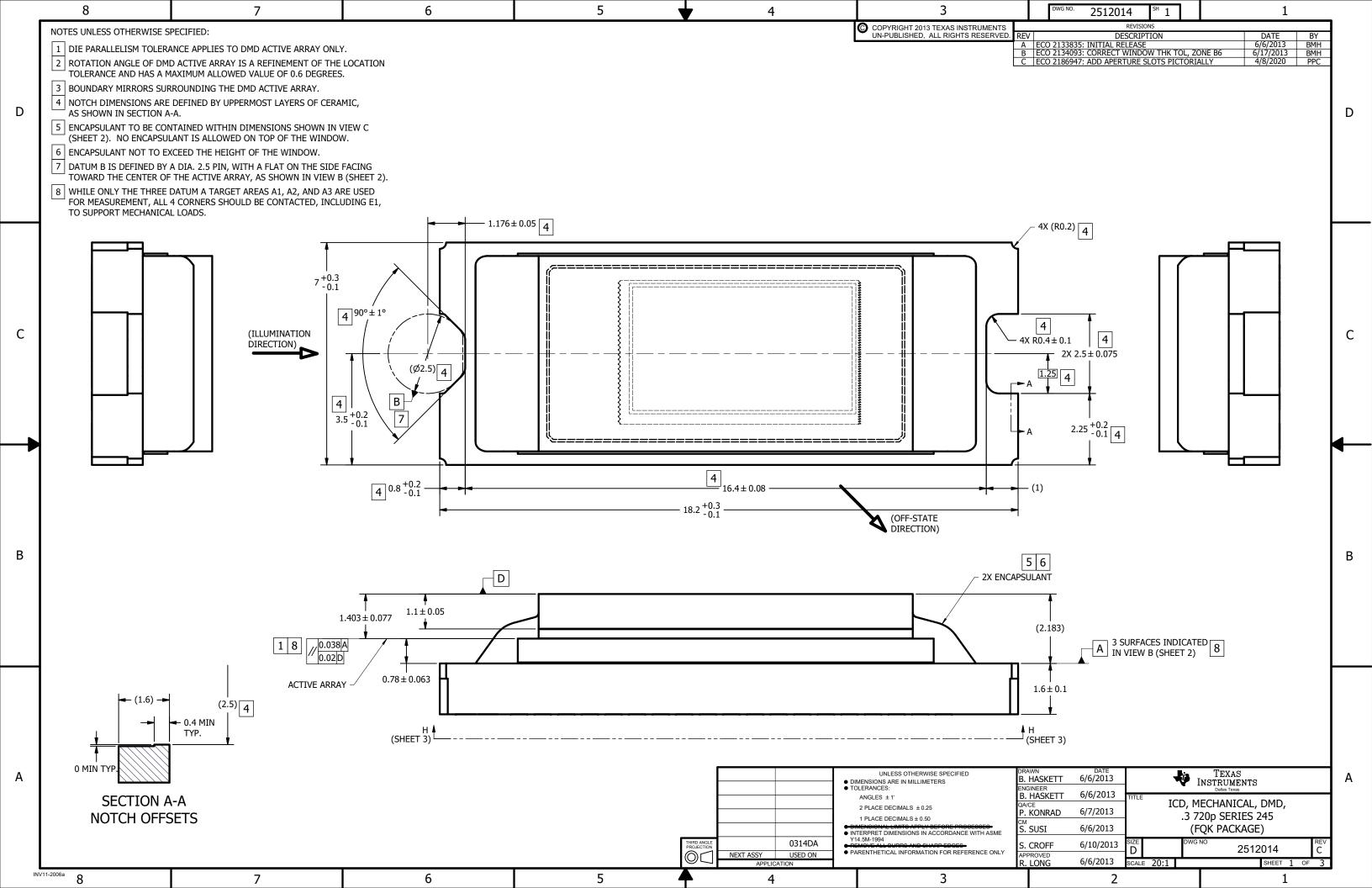
<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

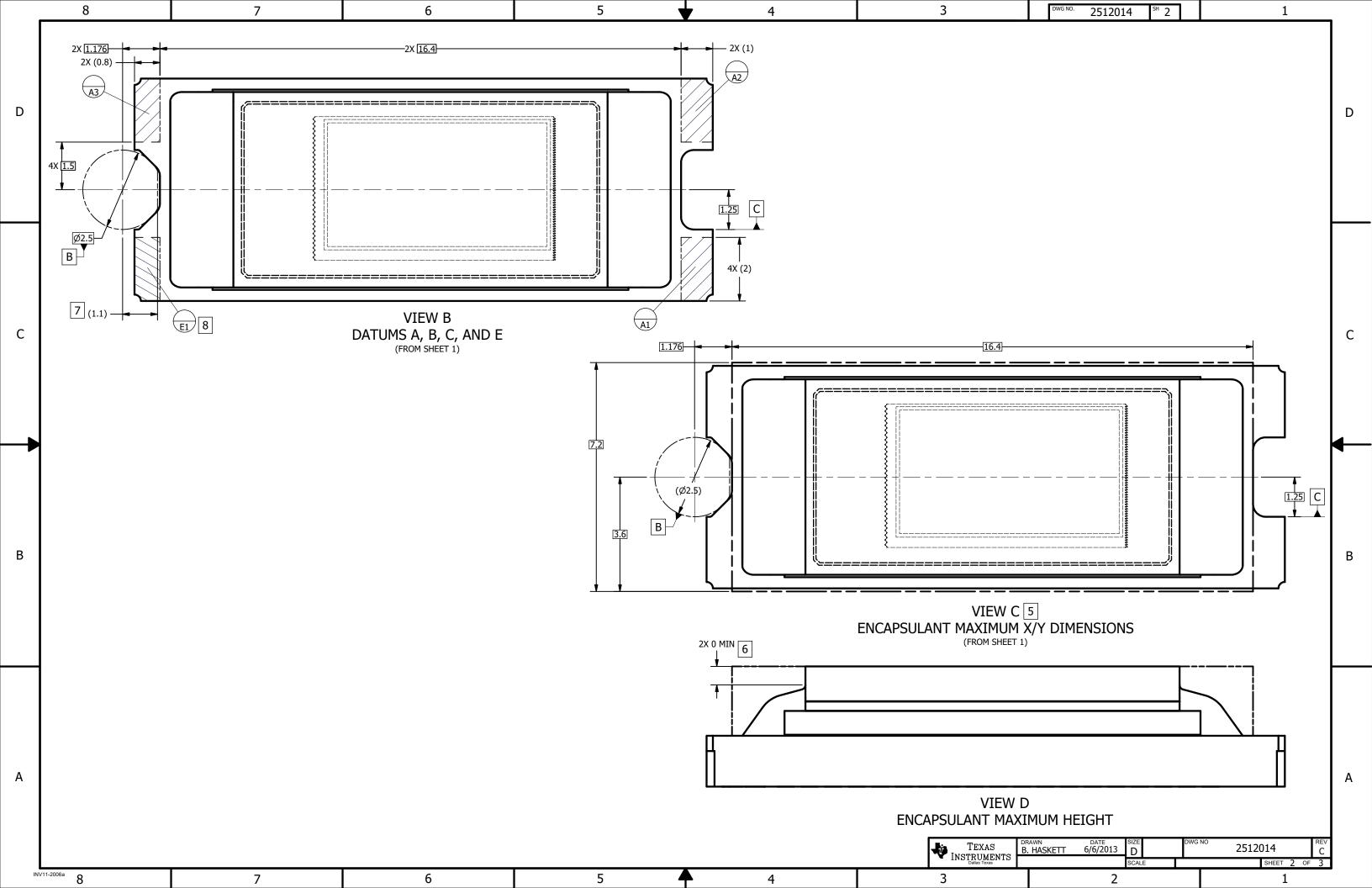
<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

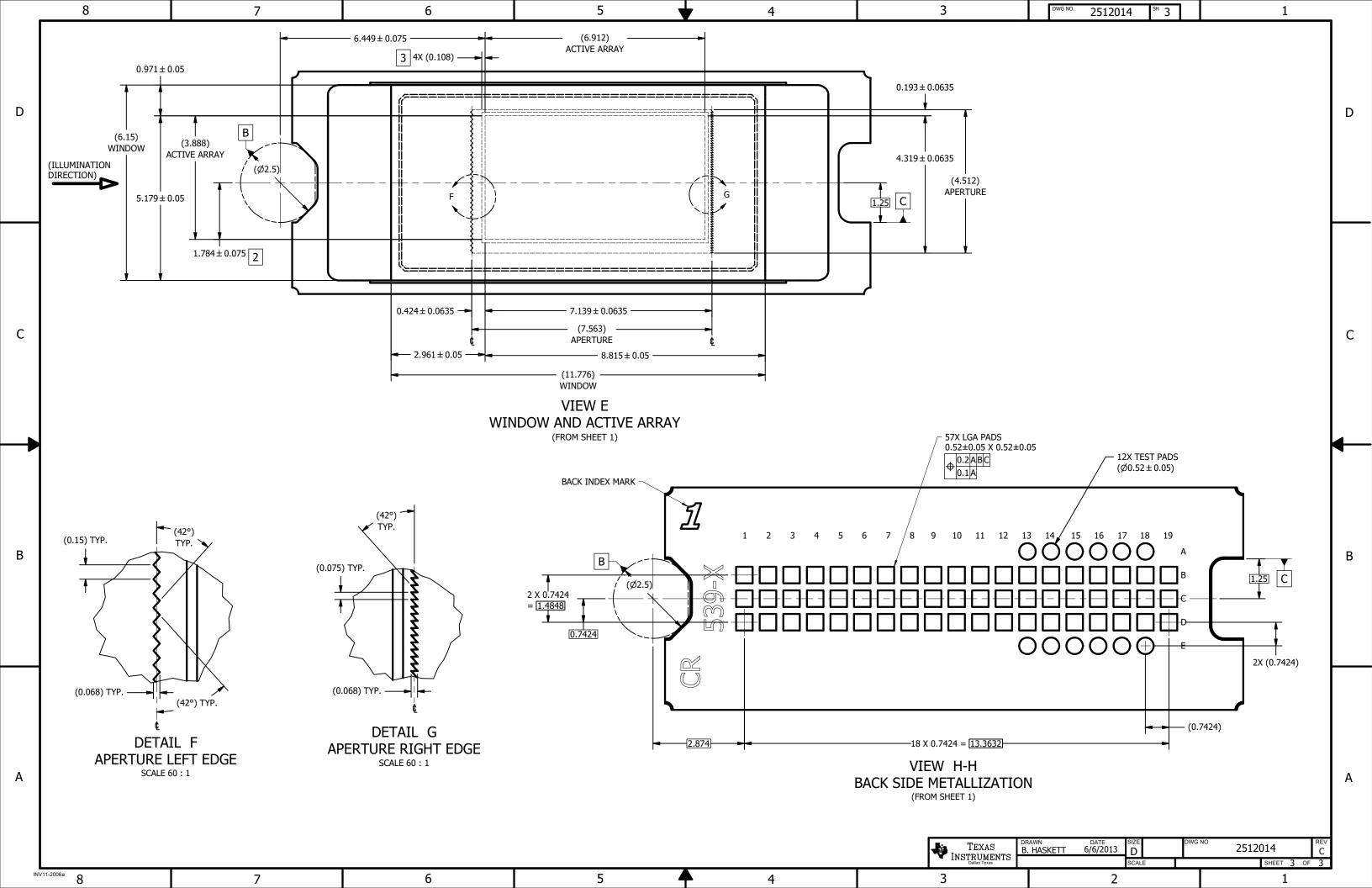
<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.







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