

16-Bit, Ultra-Low Power, Voltage-Output Digital-to-Analog Converter

FEATURES

- 16-Bit Resolution
- 2.7 V to 5.5 V Single-Supply Operation
- Very Low Power: 15 μW for 3 V Power
- High Accuracy, INL: 1 LSB
- Low Noise: 18n V/√Hz
- Fast Settling: 1.0 μS
- Fast SPI™ Interface, up to 50 MHz
- Reset to Mid-Code
- Schmitt-Trigger Inputs for Direct Optocoupler Interface

APPLICATIONS

- Portable Equipment
- Automatic Test Equipment
- Industrial Process Control
- Data Acquisition Systems
- Optical Networking

DESCRIPTION

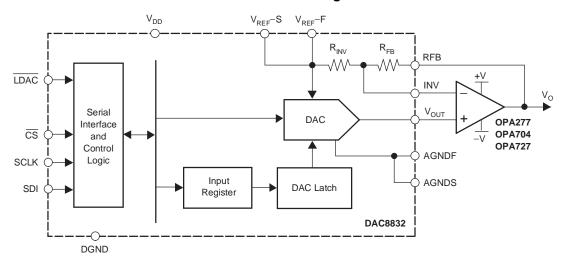
The DAC8832 is a single, 16-bit, serial-input, voltage-output digital-to-analog converter (DAC) operating from a single 3 V to 5 V power supply. The DAC8832 provides excellent linearity (1 LSB INL), low glitch, low noise, and fast settling (1.0 μ S to 1/2 LSB of full-scale output) over the specified temperature range of -40°C to +85°C. The output is unbuffered, which reduces the power consumption and the error introduced by the buffer.

This device features a standard high-speed (clock up to 50MHz), 3 V or 5 V SPI serial interface to communicate with a DSP or microprocessor.

The DAC8832 provides unipolar or bipolar output $(\pm V_{REF})$ when working with an external buffer, and is reset to mid-code after power-up. For optimum performance, a set of Kelvin connections to the external reference and the analog ground input are provided.

The DAC8832 is available in a QFN-14 package, and is pin-to-pin compatible with the DAC8831IRGY, which is reset to zero code after power-up.

Functional Block Diagram



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	POWER- ON RESET VALUE	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	PACKAGE- LEAD	PACKAGE DESIGNATOR	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC8832IRGY	±4	±1	Mid Code	-40°C to +85°C	88321	QFN-14	RGY	DAC8832IRGYT	Tape and Reel, 250
DAC6632ING I	±4	±Ι	Mid Code	-40 C to +65 C	00321	QFN-14	KGT	DAC8832IRGYR	Tape and Reel, 1000
DAC8832IBRGY	±2	.4	Mid Code	-40°C to +85°C	88321	QFN-14	RGY	DAC8832IBRGYT	Tape and Reel, 250
DAC6632IBRG I	±2	±1	Mid Code	-40°C 10 +65°C	00321	QFN-14	RGT	DAC8832IBRGYR	Tape and Reel, 1000
DAC8832ICRGY	.1	.1	Mid Code	-40°C to +85°C	88321	QFN-14	RGY	DAC8832ICRGYT	Tape and Reel, 250
DAC6632ICRG1	±1	±1	IVIIU CODE	-40 C (0 +85°C	00321	QFIN-14	NGT	DAC8832ICRGYR	Tape and Reel, 1000

⁽¹⁾ For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)(1)

	DAC8832	UNIT
V _{DD} to AGND	-0.3 to +7	V
Digital input voltage to DGND	$-0.3 \text{ to +V}_{DD} + 0.3$	V
V _{OUT} to AGND	-0.3 to +V _{DD} + 0.3	V
AGND, AGNDF, AGNDS to DGND	-0.3 to +0.3	V
Operating temperature range	-40 to +85	°C
Storage temperature range	-65 to +150	°C
Junction temperature range (T _J max)	+150	°C
Power dissipation	$(T_J max - T_A) / \theta_{JA}$	W
Thermal impedance, θ_{JA}	54.9	°C/W

⁽¹⁾ Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

Product Folder Link(s): DAC8832



ELECTRICAL CHARACTERISTICS

All specifications at $T_A = T_{MIN}$ to T_{MAX} , $V_{DD} = +3$ V or $V_{DD} = +5$ V, $V_{REF} = +2.5$ V unless otherwise noted.

				DAC8832			
PARA	METER	CONDITIONS	MIN	TYP	MAX	UNIT	
TIC PERFORMANC	E	,	<u>'</u>		'		
Resolution			16			bits	
	DAC8832ICRGY			±0.5	±1		
Linearity error	DAC8832IBRGY			±0.5	±2	LSE	
	DAC8832IRGY			±0.5	±4		
Differential linearity error		All grades		±0.5	±1	LSE	
0 :		T _A = +25°C		±1	±5		
Gain error		$T_A = -40^{\circ}C$ to $+85^{\circ}C$			±7	LSB	
Gain drift				±0.1		ppm/	
		T _A = +25°C		±0.25	±1	1.00	
Zero code error		$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$			±2	LSE	
Zero code drift				±0.05		ppm/	
PUT CHARACTERI	STICS	,	1		,		
Voltage output (1)		Unipolar operation	0		+V _{REF}	V	
voltage output (*)		Bipolar operation	-V _{REF}		+V _{REF}	V	
Output impedance	Э			6.25		kΩ	
Settling time		To $1/2$ LSB of FS, $C_L = 10$ pF		1		μs	
Slew rate ⁽²⁾		C _L = 10 pF		25		V/µs	
Digital-to-analog	glitch	1 LSB change around major carry		35		nV-	
Digital feedthroug	h ⁽³⁾			0.2		nV-	
Output noise		T _A = +25°C		18		nV/√l	
Power-supply reje	ection	V _{DD} varies ±10%			±1	LSE	
Dinolog register	atabina	R _{FB} / R _{INV}		1		Ω/Ω	
Bipolar resistor m	atching	Ratio error		±0.0015	±0.0076	%	
		T _A = +25°C		±0.25	±5	1.05	
Bipolar zero error		$T_A = -40^{\circ}C$ to $+85^{\circ}C$			±7	LSE	
Bipolar zero drift				±0.2		ppm/°	

See the *Bipolar Output Operation* section for details.
Slew rate is measured from 10% to 90% of transition when the output changes from 0 to full-scale.

Digital feedthrough is defined as the impulse injected into the analog output from the digital input. It is measured when the DAC output does not change; $\overline{\text{CS}}$ is held high, while SCLK and DIN signals are toggled.



ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A = T_{MIN}$ to T_{MAX} , $V_{DD} = +3$ V or $V_{DD} = +5$ V, $V_{REF} = +2.5$ V unless otherwise noted.

				DAC8832		
	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
REF	ERENCE INPUT					
	Reference input voltage range		1.25		V_{DD}	V
	D-((4)	Unipolar mode	9			1.0
	Reference input impedance ⁽⁴⁾	Bipolar mode	7.5			kΩ
	Reference –3 dB bandwidth, BW	Code = FFFFh		1.3		MHz
	Reference feedthrough	Code = 0000h, V _{REF} = 1 V _{PP} at 100 kHz		1		mV
	Signal-to-noise ratio, SNR			92		dB
	B. (Code = 0000h		75		_
	Reference input capacitance	Code = FFFFh		120		pF
DIGI	TAL INPUTS					
.,	Input low voltage	V _{DD} = 2.7 V			0.6	V
V_{IL}		V _{DD} = 5 V			0.8	V
. ,		V _{DD} = 2.7 V	2.1			
V_{IH}	Input high voltage	V _{DD} = 5 V	2.4			V
	Input current				±1	μΑ
	Input capacitance				10	pF
	Hysteresis voltage			0.4		V
POW	ER SUPPLY					
V_{DD}	Power-supply voltage		2.7		5.5	V
	Development .	V _{DD} = 3 V		5	20	^
I _{DD}	Power-supply current	V _{DD} = 5 V		5	20	μΑ
	Devices	V _{DD} = 3 V		15	60	\^/
	Power	V _{DD} = 5 V		25	100	μW
TEM	PERATURE RANGE	·				
	Specified performance		-40		+85	°C

⁽⁴⁾ Reference input resistance is code-dependent, minimum at 8555h.



PIN CONFIGURATION (NOT TO SCALE)

RFB 1

0

SCLK

7 CS

NOTE: (1) Exposed thermal pad must be connected to analog ground.

4

[5] [6]

TERMINAL FUNCTIONS

TER	MINAL	DESCRIPTION
NO.	NAME	DESCRIPTION
1	RFB	Feedback resistor. Connect to the output of external operational amplifier in bipolar mode.
2	V _{OUT}	Analog output of DAC
3	AGNDF	Analog ground (Force)
4	AGNDS	Analog ground (Sense)
5	V_{REF} -S	Voltage reference input (Sense). Connect to external voltage reference
6	V _{REF-} F	Voltage reference input (Force). Connect to external voltage reference
7	CS	Chip select input (active low). Data are not clocked into SDI unless CS is low.
8	SCLK	Serial clock input.
9	NC	No internal connection
10	SDI	Serial data input. Data are latched into input register on the rising edge of SCLK.
11	LDAC	Load DAC control input. Active low. When $\overline{\text{LDAC}}$ is Low, the DAC latch is simultaneously updated with the content of the input register.
12	DGND	Digital ground
13	INV	Junction point of internal scaling resistors. Connect to external operational amplifier inverting input in bipolar mode.
14	V_{DD}	Analog power supply, +3 V to +5 V.

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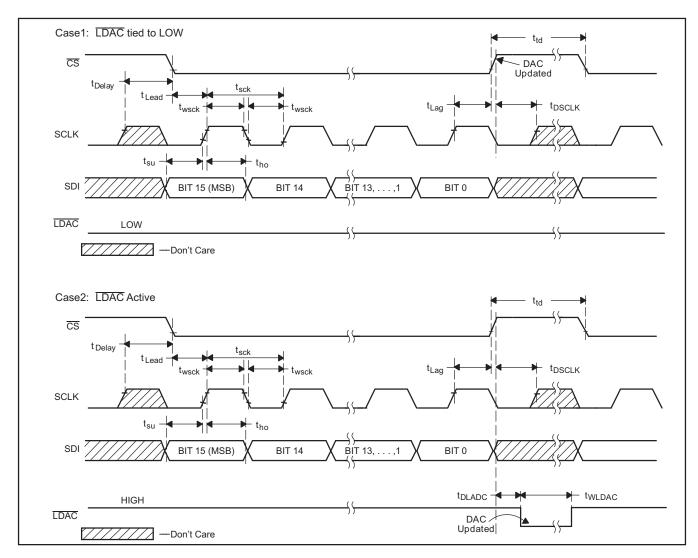


Figure 1. DAC8832 Timing Diagram



TIMING CHARACTERISTICS: $V_{DD} = +5 V^{(1)(2)}$

At -40°C to +85°C, unless otherwise noted.

	PARAMETER	MIN	MAX	UNIT
t _{sck}	SCLK period	20		ns
t _{wsck}	SCLK high or low time	10		ns
t _{Delay}	Delay from SCLK high to CS low	10		ns
t _{Lead}	CS enable lead time	10		ns
t _{Lag}	CS enable lag time	10		ns
t _{DSCLK}	Delay from CS high to SCLK high	10		ns
t _{td}	CS high between active period	30		ns
t _{su}	Data setup time (input)	10		ns
t _{ho}	Data hold time (input)	0		ns
t _{WLDAC}	LDAC width	30		ns
t _{DLDAC}	Delay from CS high to LDAC low	30		ns
	V _{DD} high to $\overline{\text{CS}}$ low (power-up delay)	10		μs

TIMING CHARACTERISTICS: $V_{DD} = +3 V^{(1)(2)}$

At -40°C to +85°C, unless otherwise noted.

	PARAMETER	MIN	MAX	UNIT
t _{sck}	SCLK period	20		ns
t _{wsck}	SCLK high or low time	10		ns
t _{Delay}	Delay from SCLK high to CS low	10		ns
t _{Lead}	CS enable lead time	10		ns
t _{Lag}	CS enable lag time	10		ns
t _{DSCLK}	Delay from CS high to SCLK high	10		ns
t _{td}	CS high between active period	30		ns
t _{su}	Data setup time (input)	10		ns
t _{ho}	Data hold time (input)	0		ns
twldac	LDAC width	30		ns
DLDAC	Delay from CS high to LDAC low	30		ns
	V _{DD} high to $\overline{\text{CS}}$ low (power-up delay)	10		μs

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Assured by design. Not production tested. Sample tested during the initial release and after any redesign or process changes that may affect this parameter.

⁽¹⁾ Assured by design. Not production tested.(2) Sample tested during the initial release and after any redesign or process changes that may affect this parameter.



TYPICAL CHARACTERISTICS: V_{DD} = +5 V

At $T_A = +25^{\circ}C$, $V_{REF} = +2.5 \text{ V}$ unless otherwise noted.

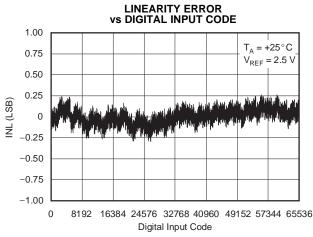


Figure 2.

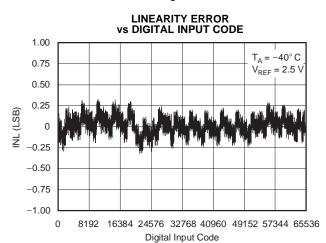
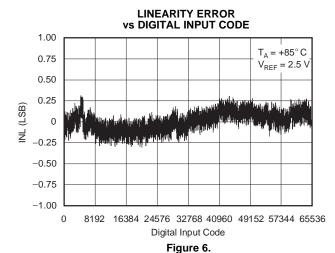
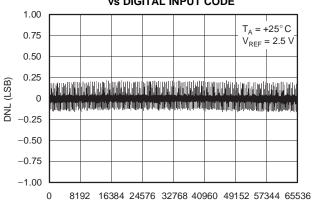


Figure 4.



DIFFERENTIAL LINEARITY ERROR VS DIGITAL INPUT CODE



Digital Input Code

Figure 3.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

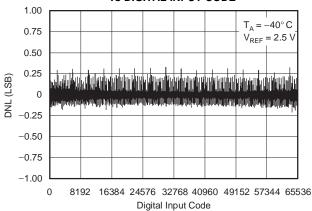
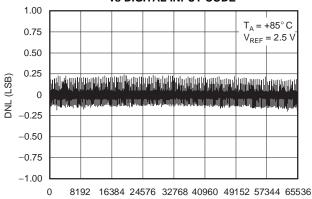


Figure 5.

DIFFERENTIAL LINEARY ERROR vs DIGITAL INPUT CODE



Digital Input Code

Figure 7.



TYPICAL CHARACTERISTICS: V_{DD} = +5 V (continued)

At $T_A = +25$ °C, $V_{REF} = +2.5$ V unless otherwise noted.

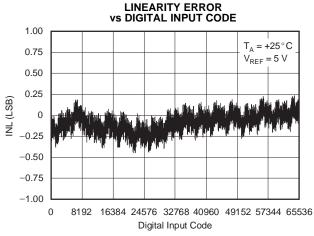


Figure 8.

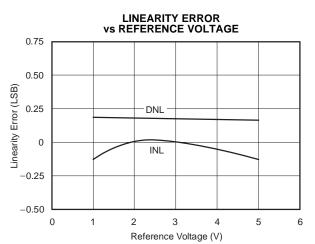
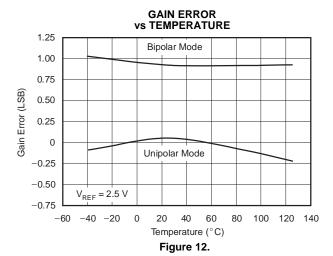


Figure 10.



DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

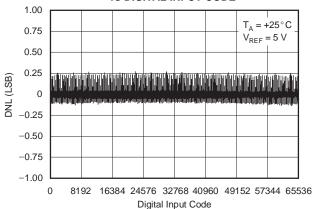


Figure 9.



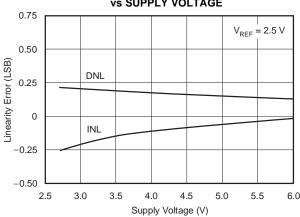


Figure 11.

ZERO-CODE ERROR

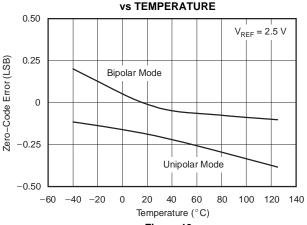


Figure 13.



TYPICAL CHARACTERISTICS: V_{DD} = +5 V (continued)

At $T_A = +25$ °C, $V_{REF} = +2.5$ V unless otherwise noted.

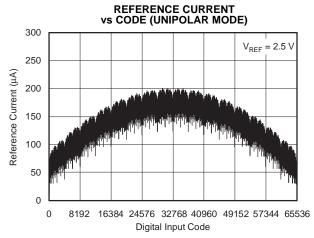
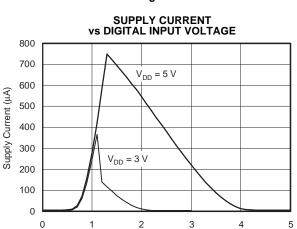
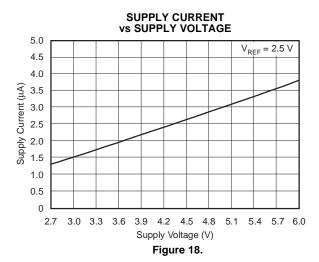


Figure 14.



Digital Input Voltage (V) Figure 16.



REFERENCE CURRENT vs CODE (BIPOLAR MODE)

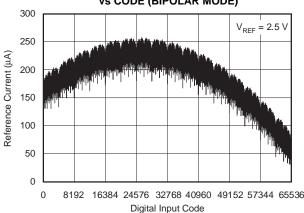


Figure 15.



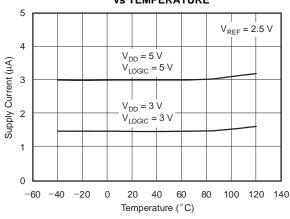


Figure 17.

SUPPLY CURRENT VS REFERENCE VOLTAGE

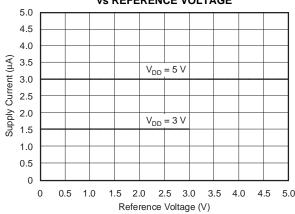
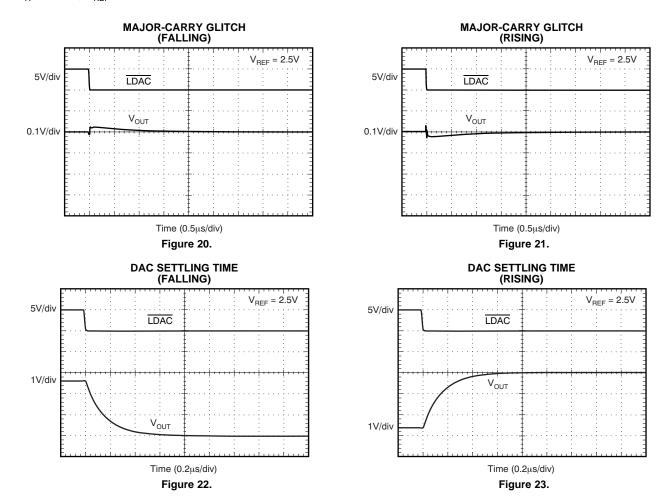


Figure 19.



TYPICAL CHARACTERISTICS: V_{DD} = +5 V (continued)

At $T_A = +25^{\circ}C$, $V_{REF} = +2.5 \text{ V}$ unless otherwise noted.



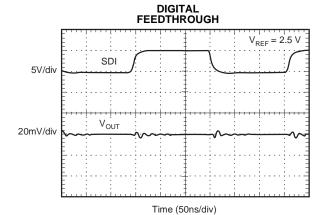


Figure 24.



TYPICAL CHARACTERISTICS: V_{DD} = +3 V

At $T_A = +25^{\circ}C$, $V_{REF} = +2.5 \text{ V}$ unless otherwise noted.

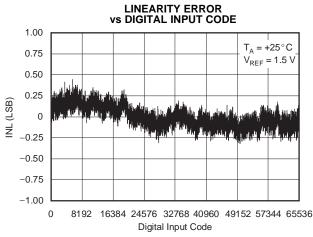


Figure 25.

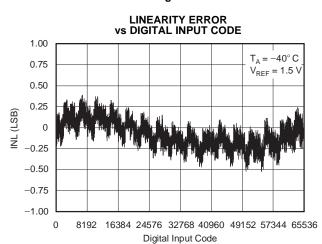
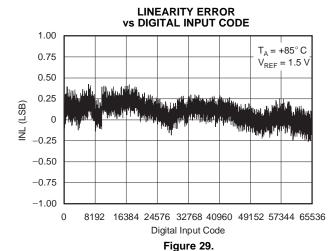
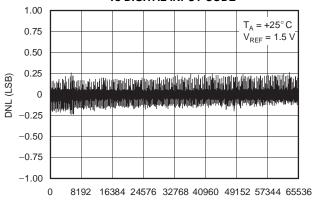


Figure 27.



DIFFERENTIAL LINEARITY ERROR VS DIGITAL INPUT CODE



Digital Input Code

Figure 26.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

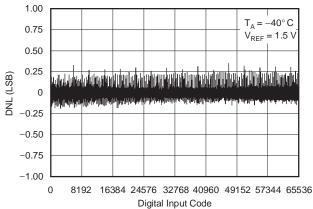
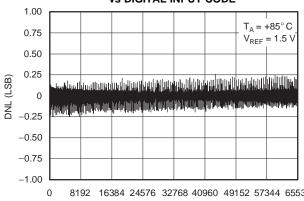


Figure 28.

DIFFERENTIAL LINEARY ERROR vs DIGITAL INPUT CODE



8192 16384 24576 32768 40960 49152 57344 65536 Digital Input Code

Figure 30.



TYPICAL CHARACTERISTICS: $V_{DD} = +3 \text{ V (continued)}$

At $T_A = +25$ °C, $V_{REF} = +2.5$ V unless otherwise noted.

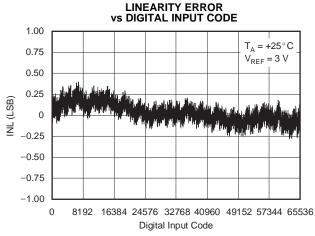


Figure 31.



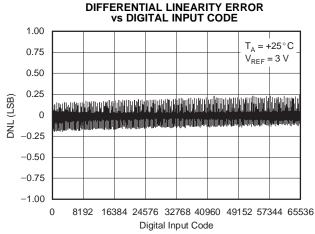


Figure 32.

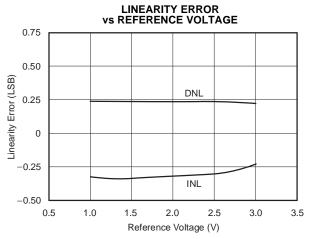
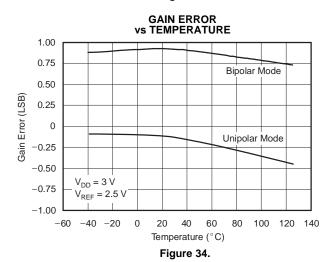


Figure 33. **ZERO-CODE ERROR**



REFERENCE CURRENT

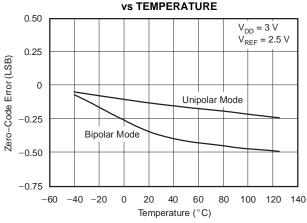


Figure 35.

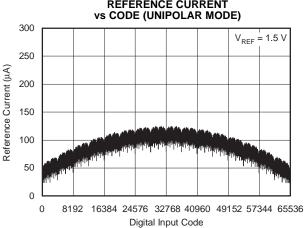
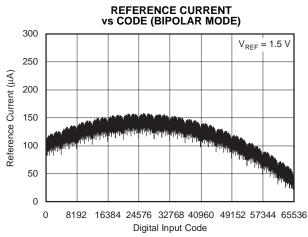


Figure 36.



TYPICAL CHARACTERISTICS: $V_{DD} = +3 \text{ V (continued)}$

At $T_A = +25$ °C, $V_{REF} = +2.5$ V unless otherwise noted.



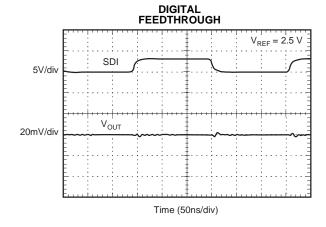
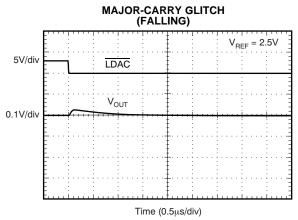


Figure 37.

Figure 38.



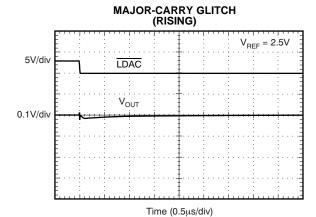
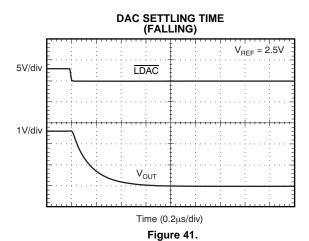


Figure 39.

Figure 40.



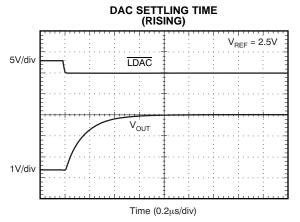


Figure 42.



THEORY OF OPERATION

GENERAL DESCRIPTION

The DAC8832 is a single, 16-bit, serial-input, voltage-output DAC. It operates from a single supply ranging from 2.7 V to 5 V, and typically consumes 5 μ A. Data are written to this device in a 16-bit word format, via an SPI serial interface. To ensure a known power-up state, the DAC8832 is designed with a power-on reset function. The DAC8832 is reset to mid-scale code. In unipolar mode, the DAC8832 is reset to $1/2 \times V_{REF}$, and in bipolar mode, is reset to 0 V. Kelvin sense connections for the reference and analog ground are also included.

DIGITAL-TO-ANALOG SECTIONS

The DAC architecture consists of two matched DAC sections and is segmented. A simplified circuit diagram is shown in Figure 43. The four MSBs of the 16-bit data word are decoded to drive 15 switches, E1 to E15. Each of these switches connects one of 15 matched resistors to either AGND or V_{REF} . The remaining 12 bits of the data word drive switches S0 to S11 of a 12-bit voltage mode R-2R ladder network.

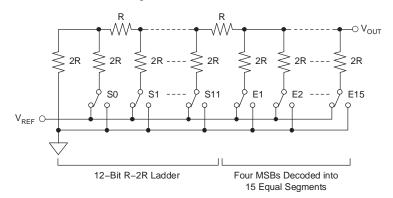


Figure 43. DAC Architecture

OUTPUT RANGE

The output of the DAC is:

 $V_{OUT} = (V_{REF} \times Code)/65536$

Where Code is the decimal data word loaded to the DAC latch.



POWER-ON RESET

The DAC8832 has a power-on reset function to ensure the output is at a known state upon power-up. Upon power-up, the DAC latch and input register contain mid-scale code until new data are loaded from the input serial shift register. Therefore, after power-up, the output from pin V_{OUT} is $0.5 \times V_{REF}$ in unipolar mode, and 0 V in bipolar mode.

However, the serial register is not cleared on power-up, so its contents are undefined. When loading data initially to the device, 16 bits or more should be loaded to prevent erroneous data appearing on the output. If more than 16 bits are loaded, the last 16 are kept; if less than 16 are loaded, bits will remain from the previous word. If the device must be interfaced with data shorter than 16 bits, the data should be padded with 0s at the LSBs.

SERIAL INTERFACE

The digital interface is standard 3-wire connection compatible with SPI, QSPITM, MicrowireTM, and TI DSP interfaces, which can operate at speeds up to 50 M-bits/sec. The data transfer is framed by \overline{CS} , the chip select signal. The DAC works as a bus slave. The bus master generates the synchronize clock, SCLK, and initiates the transmission. When \overline{CS} is high, the DAC is not accessed, and the clock SCLK and serial input data SDI are ignored. The bus master accesses the DAC by driving pin \overline{CS} low. Immediately following the high-to-low transition of \overline{CS} , the serial input data on pin SDI is shifted out from the bus master synchronously on the falling edge of SCLK, and latched on the rising edge of SCLK into the input shift register, MSB first. The low-to-high transition of \overline{CS} transfers the contents of the input shift register to the input register. All data registers are 16-bit. It takes 16 clocks of SCLK to transfer one data word to the parts. To complete a whole data word, \overline{CS} must go high immediately after 16 SCLKs are clocked in. If more than 16 SCLKs are applied during the low state of \overline{CS} , the last 16 bits are transferred to the input register on the rising edge of \overline{CS} . However, if \overline{CS} is not kept low during the entire 16 SCLK cycles, the data are corrupted. In this case, reload the DAC with a new 16-bit word.

The DAC8832 has an $\overline{\text{LDAC}}$ pin allowing the DAC latch to be updated asynchronously by bringing $\overline{\text{LDAC}}$ low after $\overline{\text{CS}}$ goes high. In this case, $\overline{\text{LDAC}}$ must be maintained high while $\overline{\text{CS}}$ is low. If $\overline{\text{LDAC}}$ is tied permanently low, the DAC latch is updated immediately after the input register is loaded (caused by the low-to-high transition of $\overline{\text{CS}}$).



APPLICATION INFORMATION

UNIPOLAR OUTPUT OPERATION

The DAC8832 is capable of driving unbuffered loads of $60 \text{ k}\Omega$. Unbuffered operation results in low supply current (typically 5 μ A) and a low offset error. The DAC8832 can be configured to output both unipolar and bipolar voltages. Figure 44 shows a typical unipolar output voltage circuit. The code table for this mode of operation is shown in Table 1.

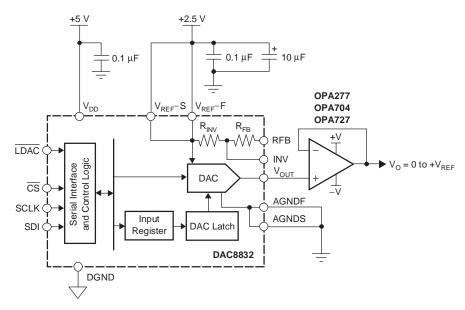


Figure 44. Unipolar Output Mode

Table 1. Unipolar Code

DAC LATCH CONTENTS	
MSB LSB	ANALOG OUTPUT
1111 1111 1111 1111	V _{REF} × (65,535/65,536)
1000 0000 0000 0000	$V_{REF} \times (32,768/65,536) = 1/2 V_{REF}$
0000 0000 0000 0001	V _{REF} × (1/65,536)
0000 0000 0000 0000	0 V

Assuming a perfect reference, the worst-case output voltage may be calculated in the following equation:

Unipolar Mode Worst-Case Output:

$${\rm V_{OUT_UNI}} = \frac{\rm D}{\rm 2^{16}} \times \left({\rm V_{REF}} + {\rm V_{GE}}\right) + {\rm V_{ZSE}} + {\rm INL}$$

Where:

V_{OUT_UNI} = Unipolar mode worst-case output

D = Code loaded to DAC

 V_{RFF} = Reference voltage applied to part

 V_{GE} = Gain error in volts

 V_{ZSE} = Zero scale error in volts

INL = Integral nonlinearity in volts

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BIPOLAR OUTPUT OPERATION

With the aid of an external operational amplifier, the DAC8832 may be configured to provide a bipolar voltage output. A typical circuit of such an operation is shown in Figure 45. The matched bipolar offset resistors R_{FB} and R_{INV} are connected to an external operational amplifier to achieve this bipolar output swing; typically, $R_{FB} = R_{INV} = 28 \text{ k}\Omega$.

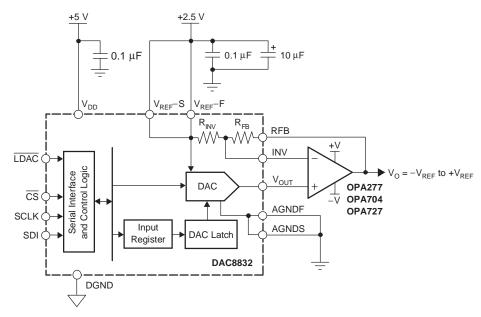


Figure 45. Bipolar Output Mode

Table 2 shows the transfer function for this output operating mode. The DAC8832 also provides a set of Kelvin connections to the analog ground and external reference inputs.

Table 2. Bipolar Code

Assuming a perfect reference, the worst-case output voltage may be calculated from the following equation:

Bipolar Mode Worst-Case Output:

$$V_{OUT_BIP} = \frac{\left[\left(V_{OUT_UNI} + V_{OS}\right)(2 + RD) - V_{REF}(1 + RD)\right]}{1 + \left(\frac{2 + RD}{A}\right)}$$

Where:

V_{OS} = External operational amplifier input offset voltage

 $RD = R_{FB}$ and R_{IN} resistor matching error

A = Operational amplifier open-loop gain



OUTPUT AMPLIFIER SELECTION

For bipolar mode, a precision amplifier should be used, supplied from a dual power supply. This provides the $\pm V_{REF}$ output.

In a single-supply application, selection of a suitable operational amplifier may be more difficult because the output swing of the amplifier does not usually include the negative rail; in this case, AGND. This output swing can result in some degradation of the specified performance unless the application does not use codes near 0.

The selected operational amplifier needs to have low-offset voltage (the DAC LSB is 38 μ V with a 2.5 V reference), eliminating the need for output offset trims. Input bias current should also be low because the bias current multiplied by the DAC output impedance (approximately 6.25 k Ω) adds to the zero-code error.

Rail-to-rail input and output performance are required. For fast settling, the slew rate of the operational amplifier should not impede the settling time of the DAC. Output impedance of the DAC is constant and code-independent, but in order to minimize gain errors the input impedance of the output amplifier should be as high as possible. The amplifier should also have a 3 dB bandwidth of 1 MHz or greater. The amplifier adds another time constant to the system, thus increasing the settling time of the output. A higher 3 dB amplifier bandwidth results in a shorter effective settling time of the combined DAC and amplifier.

REFERENCE AND GROUND

Since the input impedance is code-dependent, the reference pin should be driven from a low impedance source. The DAC8832 operates with a voltage reference ranging from 1.25 V to V_{DD} . References below 1.25 V result in reduced accuracy.

The DAC full-scale output voltage is determined by the reference. Table 1 and Table 2 outline the analog output voltage for particular digital codes.

For optimum performance, Kelvin sense connections are provided. If the application does not require separate force and sense lines, they should be tied together close to the package to minimize voltage drops between the package leads and the internal die.

POWER SUPPLY AND REFERENCE BYPASSING

For accurate high-resolution performance, it is recommended that the reference and supply pins be bypassed with a 10 μ F tantalum capacitor in parallel with a 0.1 μ F ceramic capacitor.

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11-Apr-2011

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
DAC8832IBRGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
DAC8832IBRGYRG4	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
DAC8832IBRGYT	ACTIVE	VQFN	RGY	14	250	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
DAC8832IBRGYTG4	ACTIVE	VQFN	RGY	14	250	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
DAC8832ICRGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
DAC8832ICRGYRG4	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
DAC8832ICRGYT	ACTIVE	VQFN	RGY	14	250	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
DAC8832ICRGYTG4	ACTIVE	VQFN	RGY	14	250	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
DAC8832IRGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
DAC8832IRGYRG4	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
DAC8832IRGYT	ACTIVE	VQFN	RGY	14	250	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
DAC8832IRGYTG4	ACTIVE	VQFN	RGY	14	250	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
DAC8832IBRGYT	Active	Production	VQFN (RGY) 14	250 SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	BQW
DAC8832IBRGYT.A	Active	Production	VQFN (RGY) 14	250 SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	BQW
DAC8832ICRGYR	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	BQW
DAC8832ICRGYR.A	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	BQW
DAC8832ICRGYT	Active	Production	VQFN (RGY) 14	250 SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	BQW
DAC8832ICRGYT.A	Active	Production	VQFN (RGY) 14	250 SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	BQW
DAC8832IRGYR	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	BQW
DAC8832IRGYR.A	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	BQW
DAC8832IRGYRG4	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	BQW
DAC8832IRGYT	Active	Production	VQFN (RGY) 14	250 SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	BQW
DAC8832IRGYT.A	Active	Production	VQFN (RGY) 14	250 SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	BQW

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

www.ti.com 11-Nov-2025

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8832IBRGYT	VQFN	RGY	14	250	180.0	12.4	3.85	3.85	1.35	8.0	12.0	Q1
DAC8832ICRGYR	VQFN	RGY	14	3000	330.0	12.4	3.85	3.85	1.35	8.0	12.0	Q1
DAC8832ICRGYT	VQFN	RGY	14	250	180.0	12.4	3.85	3.85	1.35	8.0	12.0	Q1
DAC8832IRGYR	VQFN	RGY	14	3000	330.0	12.4	3.85	3.85	1.35	8.0	12.0	Q1
DAC8832IRGYT	VQFN	RGY	14	250	180.0	12.4	3.85	3.85	1.35	8.0	12.0	Q1



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*All dimensions are nominal

7 III CHILOTOGO CHO TIOTIII CH							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8832IBRGYT	VQFN	RGY	14	250	210.0	185.0	35.0
DAC8832ICRGYR	VQFN	RGY	14	3000	350.0	350.0	43.0
DAC8832ICRGYT	VQFN	RGY	14	250	210.0	185.0	35.0
DAC8832IRGYR	VQFN	RGY	14	3000	350.0	350.0	43.0
DAC8832IRGYT	VQFN	RGY	14	250	210.0	185.0	35.0

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
 The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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