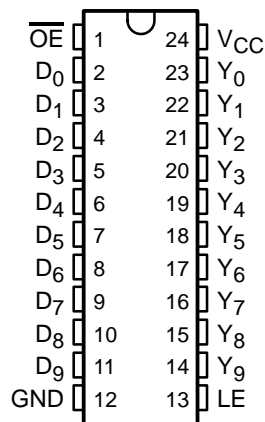


CY54FCT841T, CY74FCT841T 10-BIT LATCHES WITH 3-STATE OUTPUTS

SCCS035A – SEPTEMBER 1994 – REVISED OCTOBER 2001

- Function, Pinout, and Drive Compatible With FCT, F, and AM29841 Logic
- Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- Matched Rise and Fall Times
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Fully Compatible With TTL Input and Output Logic Levels
- High-Speed Parallel Latches
- Buffered Common Latch-Enable Input
- 3-State Outputs
- CY54FCT841T
 - 32-mA Output Sink Current
 - 12-mA Output Source Current
- CY74FCT841T
 - 64-mA Output Sink Current
 - 32-mA Output Source Current

CY54FCT841T . . . D PACKAGE
CY74FCT841T . . . P, Q, OR SO PACKAGE
(TOP VIEW)



description

The 'FCT841T bus-interface latches are designed to eliminate additional packages required to buffer existing latches and provide additional data width for wider address/data paths or buses carrying parity. The 'FCT841T devices are buffered 10-bit-wide versions of the FCT373 function.

The 'FCT841T devices' high-performance interface is designed for high-capacitance-load drive capability, while providing low-capacitance bus loading at both inputs and outputs. Outputs are designed for low-capacitance bus loading in the high-impedance state.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

PIN DESCRIPTION

NAME	I/O	DESCRIPTION
D	I	Latch data inputs
LE	I	Latch-enable input. The latches are transparent when LE is high. Input data is latched on the high-to-low transition.
Y	O	3-state latch outputs
\overline{OE}	I	Output-enable control. When \overline{OE} is low, the outputs are enabled. When \overline{OE} is high, the outputs are in the high-impedance (off) state.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2001, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

CY54FCT841T, CY74FCT841T 10-BIT LATCHES WITH 3-STATE OUTPUTS

SCCS035A – SEPTEMBER 1994 – REVISED OCTOBER 2001

ORDERING INFORMATION

T _A	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QSOP – Q	Tape and reel	5.5	CY74FCT841CTQCT	FCT841C
	SOIC – SO	Tube	5.5	CY74FCT841CTSOC	FCT841C
		Tape and reel	5.5	CY74FCT841CTSOCT	
	DIP – P	Tube	6.5	CY74FCT841BTPC	CY74FCT841BTPC
	SOIC – SO	Tube	9	CY74FCT841ATSOC	FCT841A
Tape and reel		9	CY74FCT841ATSOCT		
-55°C to 125°C	CDIP – D	Tube	10	CY54FCT841ATDMB	

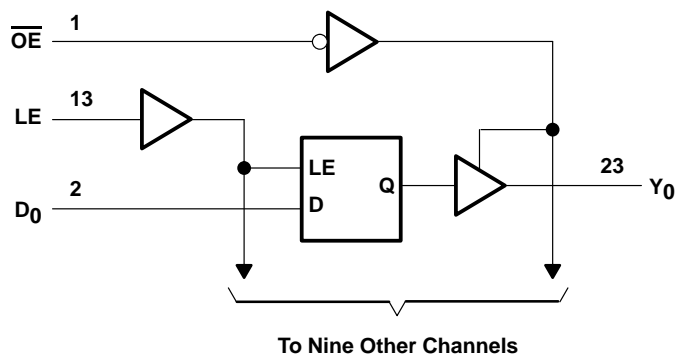
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS			INTERNAL OUTPUTS		FUNCTION
\overline{OE}	LE	D	O	Y	
H	X	X	X	Z	Z
H	H	L	L	Z	
H	H	H	H	Z	
H	L	X	NC	Z	Latched (Z)
L	H	L	L	L	Transparent
L	H	H	H	H	
L	L	X	NC	NC	Latched

H = High logic level, L = Low logic level, X = Don't care, NC = No change, Z = High-impedance state

logic diagram (positive logic)



CY54FCT841T, CY74FCT841T
10-BIT LATCHES
WITH 3-STATE OUTPUTS

SCCS035A – SEPTEMBER 1994 – REVISED OCTOBER 2001

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		CY54FCT841T			CY74FCT841T			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = 4.5 V,	I _{IN} = -18 mA	-0.7	-1.2				V	
	V _{CC} = 4.75 V,	I _{IN} = -18 mA				-0.7	-1.2		
V _{OH}	V _{CC} = 4.5 V,	I _{OH} = -12 mA	2.4	3.3				V	
	V _{CC} = 4.75 V	I _{OH} = -32 mA			2				
		I _{OH} = -15 mA			2.4	3.3			
V _{OL}	V _{CC} = 4.5 V,	I _{OL} = 32 mA	0.3	0.55				V	
	V _{CC} = 4.75 V,	I _{OL} = 64 mA				0.3	0.55		
V _{hys}	All inputs		0.2			0.2		V	
I _I	V _{CC} = 5.5 V,	V _{IN} = V _{CC}			5			μA	
	V _{CC} = 5.25 V,	V _{IN} = V _{CC}					5		
I _{IH}	V _{CC} = 5.5 V,	V _{IN} = 2.7 V			±1			μA	
	V _{CC} = 5.25 V,	V _{IN} = 2.7 V					±1		
I _{IL}	V _{CC} = 5.5 V,	V _{IN} = 0.5 V			±1			μA	
	V _{CC} = 5.25 V,	V _{IN} = 0.5 V					±1		
I _{OZH}	V _{CC} = 5.5 V,	V _{OUT} = 2.7 V			10			μA	
	V _{CC} = 5.25 V,	V _{OUT} = 2.7 V					10		
I _{OZL}	V _{CC} = 5.5 V,	V _{OUT} = 0.5 V			-10			μA	
	V _{CC} = 5.25 V,	V _{OUT} = 0.5 V					-10		
I _{OS} ‡	V _{CC} = 5.5 V,	V _{OUT} = 0 V	-60	-120	-225			mA	
	V _{CC} = 5.25 V,	V _{OUT} = 0 V				-60	-120		-225
I _{off}	V _{CC} = 0 V,	V _{OUT} = 4.5 V			±1		±1	μA	
I _{CC}	V _{CC} = 5.5 V,	V _{IN} ≤ 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V	0.1	0.2				mA	
	V _{CC} = 5.25 V,	V _{IN} ≤ 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V				0.1	0.2		
ΔI _{CC}	V _{CC} = 5.5 V, V _{IN} = 3.4 V§, f ₁ = 0, Outputs open		0.5	2				mA	
	V _{CC} = 5.25 V, V _{IN} = 3.4 V§, f ₁ = 0, Outputs open					0.5	2		
I _{CCD} ¶	V _{CC} = 5.5 V, One input switching at 50% duty cycle, Outputs open, OE = GND, LE = V _{CC} , V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V		0.06	0.12				mA/ MHz	
	V _{CC} = 5.25 V, One input switching at 50% duty cycle, Outputs open, OE = GND, LE = V _{CC} , V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V					0.06	0.12		

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND

¶ This parameter is derived for use in total power-supply calculations.



CY54FCT841T, CY74FCT841T
10-BIT LATCHES
WITH 3-STATE OUTPUTS

SCCS035A – SEPTEMBER 1994 – REVISED OCTOBER 2001

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS		CY54FCT841T		CY74FCT841T		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
I _C #	V _{CC} = 5.5 V, Outputs open, OE = GND, LE = V _{CC}	One bit switching at f ₁ = 10 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V	0.7	1.4		mA	
			V _{IN} = 3.4 V or GND	1	2.4			
		10 bits switching at f ₁ = 2.5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V	1	3.2			
			V _{IN} = 3.4 V or GND	4.1	13.2			
	V _{CC} = 5.25 V, Outputs open, OE = GND, LE = V _{CC}	One bit switching at f ₁ = 10 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V			0.7		1.4
			V _{IN} = 3.4 V or GND			1		2.4
	10 bits switching at f ₁ = 2.5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V			1	3.2		
		V _{IN} = 3.4 V or GND			4.1	13.2		
C _i				5	10	5	10	pF
C _o				9	12	9	12	pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

I_C = I_{CC} + ΔI_{CC} × D_H × N_T + I_{CCD} (f₀/2 + f₁ × N₁)

Where:

I_C = Total supply current

I_{CC} = Power-supply current with CMOS input levels

ΔI_{CC} = Power-supply current for a TTL high input (V_{IN} = 3.4 V)

D_H = Duty cycle for TTL inputs high

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)

f₀ = Clock frequency for registered devices, otherwise zero

f₁ = Input signal frequency

N₁ = Number of inputs changing at f₁

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I_{CC} formula.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		CY54FCT841AT		CY74FCT841AT		CY74FCT841BT		CY74FCT841CT		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, LE high	5		4		4		4		ns
t _{su}	Setup time, data before LE↑	2.5		2.5		2.5		2.5		ns
t _h	Hold time, data after LE↑	3		2.5		2.5		2.5		ns



CY54FCT841T, CY74FCT841T
10-BIT LATCHES
WITH 3-STATE OUTPUTS

SCCS035A – SEPTEMBER 1994 – REVISED OCTOBER 2001

switching characteristics over operating free-air temperature range (see Figure 1)

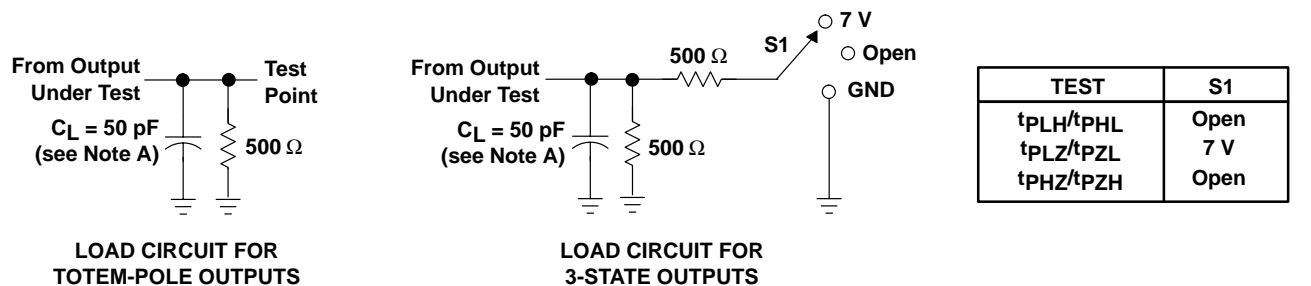
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST LOAD	CY54FCT841AT		CY74FCT841AT		UNIT
				MIN	MAX	MIN	MAX	
t _{PLH}	D	Y	C _L = 50 pF, R _L = 500 Ω	1.5	10	1.5	9	ns
t _{PHL}				1.5	10	1.5	9	
t _{PLH}	D	Y	C _L = 300 pF, R _L = 500 Ω	1.5	15	1.5	13	ns
t _{PHL}				1.5	15	1.5	13	
t _{PLH}	LE	Y	C _L = 50 pF, R _L = 500 Ω	1.5	13	1.5	12	ns
t _{PHL}				1.5	13	1.5	12	
t _{PLH}	LE	Y	C _L = 300 pF, R _L = 500 Ω	1.5	20	1.5	16	ns
t _{PHL}				1.5	20	1.5	16	
t _{PZH}	\overline{OE}	Y	C _L = 50 pF, R _L = 500 Ω	1.5	13	1.5	11.5	ns
t _{PZL}				1.5	13	1.5	11.5	
t _{PZH}	\overline{OE}	Y	C _L = 300 pF, R _L = 500 Ω	1.5	25	1.5	23	ns
t _{PZL}				1.5	25	1.5	23	
t _{PHZ}	\overline{OE}	Y	C _L = 5 pF, R _L = 500 Ω	1.5	9	1.5	7	ns
t _{PLZ}				1.5	9	1.5	7	
t _{PHZ}	\overline{OE}	Y	C _L = 50 pF, R _L = 500 Ω	1.5	10	1.5	8	ns
t _{PLZ}				1.5	10	1.5	8	

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST LOAD	CY74FCT841BT		CY74FCT841CT		UNIT
				MIN	MAX	MIN	MAX	
t _{PLH}	D	Y	C _L = 50 pF, R _L = 500 Ω	1.5	6.5	1.5	5.5	ns
t _{PHL}				1.5	6.5	1.5	5.5	
t _{PLH}	D	Y	C _L = 50 pF, R _L = 500 Ω	1.5	13	1.5	13	ns
t _{PHL}				1.5	13	1.5	13	
t _{PLH}	LE	Y	C _L = 50 pF, R _L = 500 Ω	1.5	8	1.5	6.4	ns
t _{PHL}				1.5	8	1.5	6.4	
t _{PLH}	LE	Y	C _L = 300 pF, R _L = 500 Ω	1.5	15.5	1.5	15	ns
t _{PHL}				1.5	15.5	1.5	15	
t _{PZH}	\overline{OE}	Y	C _L = 50 pF, R _L = 500 Ω	1.5	8	1.5	6.5	ns
t _{PZL}				1.5	8	1.5	6.5	
t _{PZH}	\overline{OE}	Y	C _L = 300 pF, R _L = 500 Ω	1.5	14	1.5	12	ns
t _{PZL}				1.5	14	1.5	12	
t _{PHZ}	\overline{OE}	Y	C _L = 5 pF, R _L = 500 Ω	1.5	6	1.5	5.7	ns
t _{PLZ}				1.5	6	1.5	5.7	
t _{PHZ}	\overline{OE}	Y	C _L = 50 pF, R _L = 500 Ω	1.5	7	1.5	6	ns
t _{PLZ}				1.5	7	1.5	6	

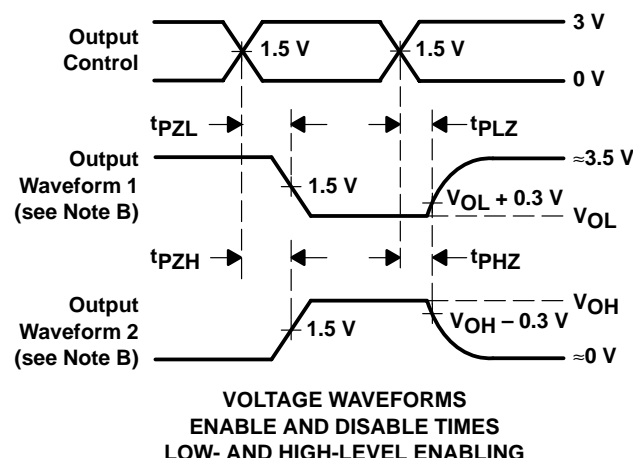
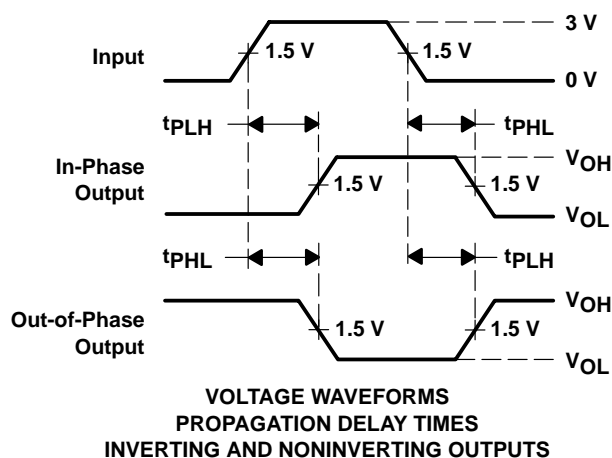
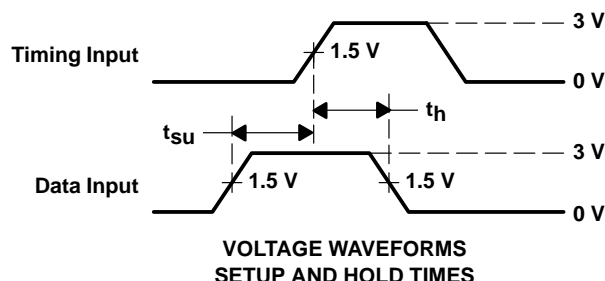
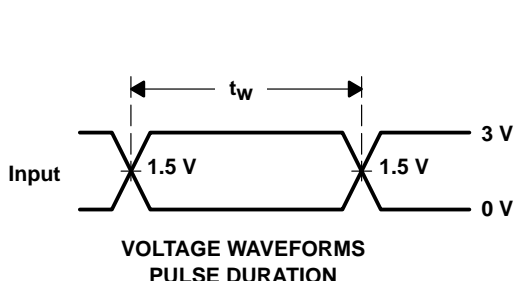


PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE OUTPUTS



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CY54FCT841ATDMB	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CY54FCT841ATDM B
CY74FCT841ATSOC	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT841A
CY74FCT841ATSOC.B	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT841A
CY74FCT841ATSOCT	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT841A
CY74FCT841ATSOCT.B	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT841A
CY74FCT841CTQCT	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT841C
CY74FCT841CTQCT.B	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT841C
CY74FCT841CTSOC	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT841C
CY74FCT841CTSOC.B	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT841C
CY74FCT841CTSOCT	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT841C
CY74FCT841CTSOCT.B	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT841C

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

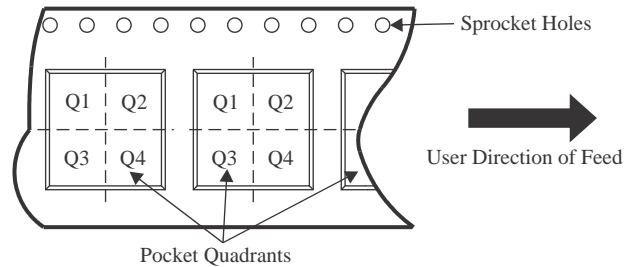
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

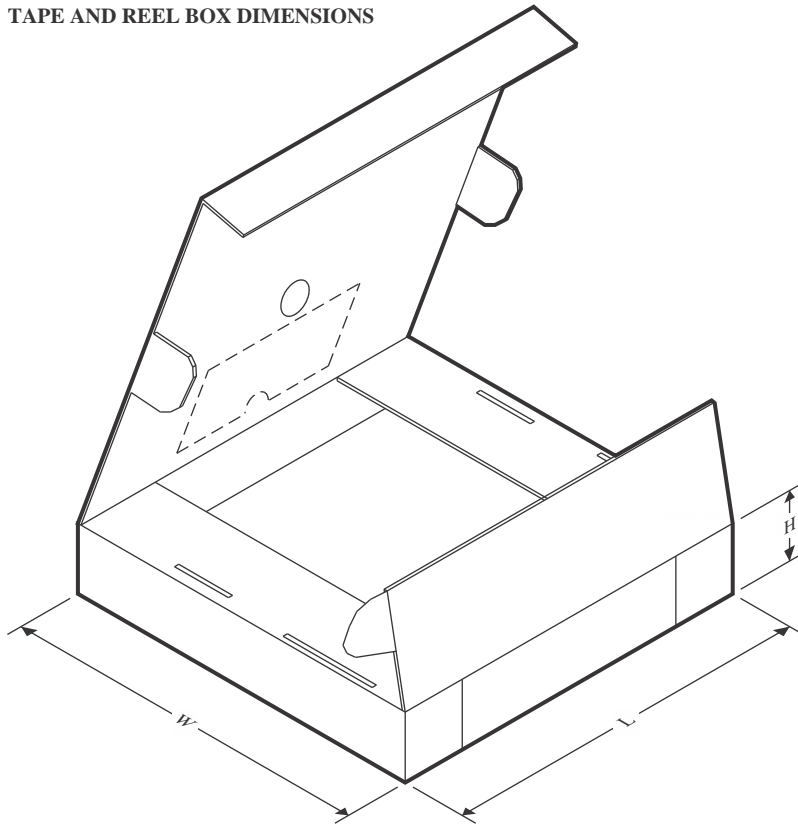
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT841ATSOCT	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CY74FCT841CTQCT	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT841CTSOCT	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT841ATSOCT	SOIC	DW	24	2000	350.0	350.0	43.0
CY74FCT841CTQCT	SSOP	DBQ	24	2500	353.0	353.0	32.0
CY74FCT841CTSOCT	SOIC	DW	24	2000	350.0	350.0	43.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CY74FCT841ATSOC	DW	SOIC	24	25	506.98	12.7	4826	6.6
CY74FCT841ATSOC.B	DW	SOIC	24	25	506.98	12.7	4826	6.6
CY74FCT841CTSOC	DW	SOIC	24	25	506.98	12.7	4826	6.6
CY74FCT841CTSOC.B	DW	SOIC	24	25	506.98	12.7	4826	6.6

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025