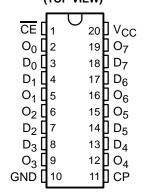
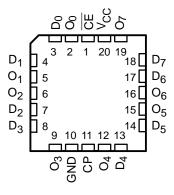
- Function, Pinout, and Drive Compatible With FCT and F Logic
- Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- Matched Rise and Fall Times
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Fully Compatible With TTL Input and Output Logic Levels
- Clock Enable for Address and Data Synchronization Application
- Eight Edge-Triggered D-Type Flip-Flops
- CY54FCT377T
 - 32-mA Output Sink Current
 - 12-mA Output Source Current
- CY74FCT377T
 - 64-mA Output Sink Current
 - 32-mA Output Source Current

SN74FCT377T . . . Q OR SO PACKAGE (TOP VIEW)



SN54FCT377T . . . L PACKAGE (TOP VIEW)



description

The 'FCT377T devices have eight triggered D-type flip-flops with individual data (D) inputs. The common buffered clock (CP) inputs load all flip-flops simultaneously when the clock-enable ($\overline{\text{CE}}$) input is low. The register is fully edge triggered. The state of each D input at one setup time before the low-to-high clock transition is transferred to the corresponding flip-flop output (O). $\overline{\text{CE}}$ must be stable only one setup time prior to the low-to-high clock transition for predictable operation.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



ORDERING INFORMATION

TA	PAC	KAGE [†]	SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	QSOP – Q	Tape and reel	5.2	CY74FCT377CTQCT	FCT377C
	SOIC - SO	Tube	5.2	CY74FCT377CTSOC	FCT377C
	3010 = 30	Tape and reel	5.2	CY74FCT377CTSOCT	1013/70
–40°C to 85°C	QSOP – Q	Tape and reel	7.2	CY74FCT377ATQCT	FCT377A
	SOIC - SO	Tube	7.2	CY74FCT377ATSOC	FCT377A
	3010 - 30	Tape and reel	7.2	CY74FCT377ATSOCT	FCISTIA
	QSOP – Q	Tape and reel	13	CY74FCT377TQCT	FCT377
–55°C to 125°C	LCC – L	Tube	5.5	CY54FCT377CTLMB	
-55 C to 125°C	LCC - L	Tube	8.3	CY54FCT377ATLMB	

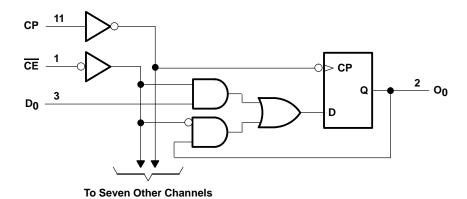
[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

	INPUTS		OUTPUT	OPERATING
СР	CE	D	0	MODE
1	I	h	Н	Load 1
1	1	1	L	Load 0
↑ X	h H	X	No change	Hold

 $H=High\,logic\,level,\,h=High\,logic\,level\,one$ setup time prior to the low-to-high clock transition, $L=Low\,logic\,level,\,l=Low\,logic\,level$ one setup time prior to the low-to-high clock transition, $X=Don't\,care,\,\uparrow=Low-to-high\,clock\,transition$

logic diagram



TEXAS INSTRUMENTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range to ground potential	\dots -0.5 V to 7 V
DC input voltage range	\dots -0.5 V to 7 V
DC output voltage range	\dots -0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, θ _{JA} (see Note 1): Q package	
SO package	58°C/W
Ambient temperature range with power applied, T _A	–65°C to 135°C
Storage temperature range, T _{stq}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 2)

		CY!	54FCT37	7T	CY7	74FCT37	7T	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
ІОН	High-level output current			-12			-32	mA
loL	Low-level output current			32			64	mA
TA	Operating free-air temperature	-55		125	-40		85	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.



NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER		TEGT COMPLETE	NIO	CY	54FCT37	7T	CY	74FCT37	7T	
PARAMETER		TEST CONDITIO	JN5	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
V	$V_{CC} = 4.5 \text{ V},$	$I_{IN} = -18 \text{ mA}$			-0.7	-1.2				٧
VIK	$V_{CC} = 4.75 \text{ V},$	$I_{1N} = -18 \text{ mA}$						-0.7	-1.2	V
	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -12 \text{ mA}$		2.4	3.3					
Voн	V _{CC} = 4.75 V	I _{OH} = -32 mA					2			V
	VCC = 4.75 V	I _{OH} = -15 mA					2.4	3.3		
Val	$V_{CC} = 4.5 \text{ V},$	$I_{OL} = 32 \text{ mA}$			0.3	0.55				V
VOL	$V_{CC} = 4.75 \text{ V},$	$I_{OL} = 64 \text{ mA}$						0.3	0.55	V
V_{hys}	All inputs				0.2			0.2		V
	$V_{CC} = 5.5 \text{ V},$	$V_{IN} = V_{CC}$				5				μΑ
ΙΙ	$V_{CC} = 5.25 \text{ V},$	$V_{IN} = V_{CC}$							5	μΑ
1	$V_{CC} = 5.5 \text{ V},$	$V_{1N} = 2.7 \text{ V}$				±1				μΑ
lіН	$V_{CC} = 5.25 \text{ V},$	$V_{IN} = 2.7 \text{ V}$							±1	μΑ
1	$V_{CC} = 5.5 \text{ V},$	$V_{IN} = 0.5 V$				±1				μΑ
IIL	$V_{CC} = 5.25 \text{ V},$	$V_{IN} = 0.5 V$							±1	μΑ
. +	$V_{CC} = 5.5 \text{ V},$	V _{OUT} = 0 V		-60	-120	-225				mA
los‡	$V_{CC} = 5.25 \text{ V},$	V _{OUT} = 0 V					-60	-120	-225	IIIA
l _{off}	$V_{CC} = 0 V$,	V _{OUT} = 4.5 V				±1			±1	μΑ
loo	$V_{CC} = 5.5 \text{ V},$	$V_{IN} \leq 0.2 V$	$V_{IN} \ge V_{CC} - 0.2 \text{ V}$		0.1	0.2				mA
Icc			$V_{IN} \ge V_{CC} - 0.2 \text{ V}$					0.1	0.2	IIIA
Aloc	$V_{CC} = 5.5 \text{ V}, V_{II}$	$_{V} = 3.4 \text{ V}, f_{1} = 0,$	Outputs open		0.5	2				mA
∆ICC	V _{CC} = 5.25 V, V	$IN = 3.4 \text{ V}$, $f_1 = 0$, Outputs open			·		0.5	2	IIIA

[†] Typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.



^{*} Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, IoS tests should be performed last.

[§] Per TTL-driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

DADAMETED		TEST CONDITIO	CY	54FCT37	7T	CY	74FCT37	7T		
PARAMETER		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT		
ICCD [¶]		itputs open, g at 50% duty cycle IN ≥ V _{CC} – 0.2 V	, CE = GND,		0.06	0.12				mA/
ICCD"		Outputs open, g at 50% duty cycle IN \geq VCC $=0.2$ V	, $\overline{CE} = GND,$					0.06	0.12	MHz
		One bit switching at f ₁ = 5 MHz at	$V_{IN} \le 0.2 \text{ V or}$ $V_{IN} \ge V_{CC} - 0.2 \text{ V}$		0.7	1.4				
	$V_{CC} = 5.5 \text{ V},$ Outputs open, $f_0 = 10 \text{ MHz},$ $CE = GND$	50% duty cycle	V _{IN} = 3.4 V or GND		1.2	3.4				
		Eight bits switching at f ₁ = 2.5 MHz at	$V_{IN} \le 0.2 \text{ V or}$ $V_{IN} \ge V_{CC} - 0.2 \text{ V}$		1.6	3.2				
IC#		50% duty cycle	V _{IN} = 3.4 V or GND		3.9	12.2				A
IC"		One bit switching at	$V_{IN} \le 0.2 \text{ V or}$ $V_{IN} \ge V_{CC} - 0.2 \text{ V}$					0.7	1.4	mA
	V _{CC} = 5.25 V, Outputs open,	f ₁ = 5 MHz at 50% duty cycle	V _{IN} = 3.4 V or GND					1.2	3.4	
	f ₀ = 10 MHz, CE = GND	Eight bits switching at	$V_{IN} \le 0.2 \text{ V or}$ $V_{IN} \ge V_{CC} - 0.2 \text{ V}$					1.6	3.2	
		f ₁ = 2.5 MHz at 50% duty cycle	V _{IN} = 3.4 V or GND					3.9	12.2	
Ci					5	10		5	10	pF
Co					9	12		9	12	pF

[†] Typical values are at V_{CC} = 5 V, T_A = 25°C.

Where:

I_C = Total supply current

ICC = Power-supply current with CMOS input levels

 ΔI_{CC} = Power-supply current for a TTL high input (V_{IN} = 3.4 V)

D_H = Duty cycle for TTL inputs high N_T = Number of TTL inputs at D_H

ICCD = Dynamic current caused by an input transition pair (HLH or LHL)

f₀ = Clock frequency for registered devices, otherwise zero

f₁ = Input signal frequency

 N_1 = Number of inputs changing at f_1

All currents are in milliamperes and all frequencies are in megahertz.

 \parallel Values for these conditions are examples of the ICC formula.



This parameter is derived for use in total power-supply calculations.

 $^{^{\#}}$ IC = ICC + \triangle ICC \times DH \times NT + ICCD (f₀/2 + f₁ \times N₁)

CY54FCT377T, CY74FCT377T 8-BIT REGISTERS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			CY54FC1 CY54FC1	-	CY74FCT CY74FCT CY74FCT	377AT	UNIT
			MIN	MAX	MIN	MAX	
t _W	Pulse duration, CP high or low [†]		7		6		ns
	Setup time, high or low	Data before CP↑	2		2		no
t _{su}	Setup time, high or low	CE before CP↑	3.5		3.5		ns
Ţ.,	Hold time, high or low	Data after CP↑	1.5		1.5		no
th	Hold time, high or low	CE after CP↑	1.5		1.5		ns

[†] With one data channel switching, $t_{W(L)} = t_{W(H)} = 4$ ns and $t_{\Gamma} = t_f = 1$ ns.

switching characteristics over operating free-air temperature range (see Figure 1)

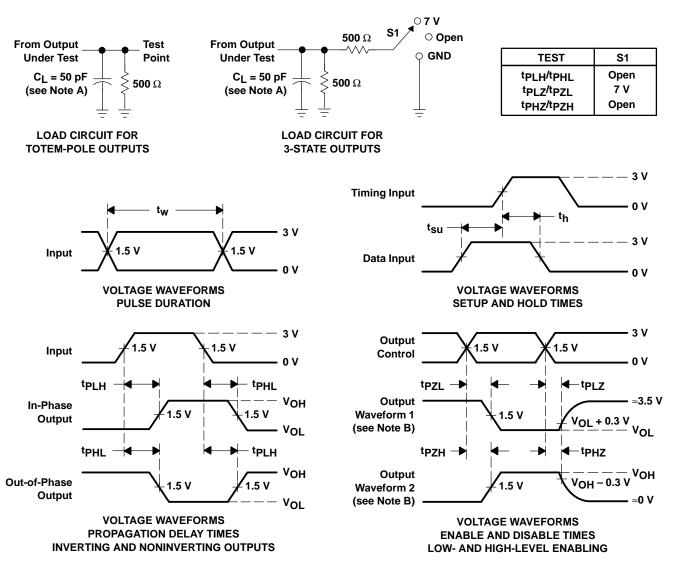
PARAMETER	FROM	то	CY54FC1	377AT	CY54FC1	UNIT	
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	ONIT
^t PLH	СР	0	2	8.3	2	5.5	no
^t PHL	CF	O	2	8.3	2	5.5	ns

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER FROM	FROM	то	CY74FC	T377T	CY74FC	Г377AT	CY74FC1	T377CT	UNIT	
	PARAMETER	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX] ""
I	^t PLH	СР	0	2	13	2	7.2	2	5.2	
Γ	^t PHL	CF	U	2	13	2	7.2	2	5.2	ns



PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-9221902M2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9221902M2A
5962-9221903M2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9221903M2A CY54FCT 377CTLMB
CY54FCT377CTLMB	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9221903M2A CY54FCT 377CTLMB
CY74FCT377ATQCT	Active	Production	SSOP (DBQ) 20	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT377A
CY74FCT377ATQCT.B	Active	Production	SSOP (DBQ) 20	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT377A
CY74FCT377ATQCTG4	Active	Production	SSOP (DBQ) 20	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT377A
CY74FCT377ATQCTG4.B	Active	Production	SSOP (DBQ) 20	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT377A
CY74FCT377ATSOC	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT377A
CY74FCT377ATSOC.B	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT377A

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT377ATQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT377ATQCTG4	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

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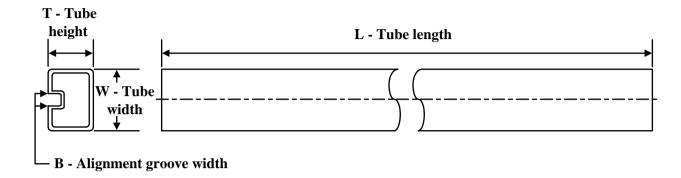
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT377ATQCT	SSOP	DBQ	20	2500	353.0	353.0	32.0
CY74FCT377ATQCTG4	SSOP	DBQ	20	2500	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9221902M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9221903M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
CY54FCT377CTLMB	FK	LCCC	20	55	506.98	12.06	2030	NA
CY74FCT377ATSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT377ATSOC.B	DW	SOIC	20	25	507	12.83	5080	6.6

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