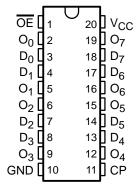
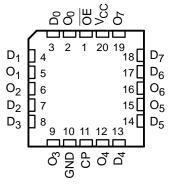
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- Function, Pinout, and Drive Compatible With FCT and F Logic
- Reduced V<sub>OH</sub> (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- Edge-Triggered D-Type Inputs
- 250-MHz Typical Switching Rate
- CY54FCT374T
  - 32-mA Output Sink Current
  - 12-mA Output Source Current
- CY74FCT374T
  - 64-mA Output Sink Current
  - 32-mA Output Source Current
- 3-State Outputs

#### CY54FCT374T . . . D PACKAGE CY74FCT374T . . . P, Q, OR SO PACKAGE (TOP VIEW)



#### CY54FCT374T . . . L PACKAGE (TOP VIEW)



#### description

The 'FCT374T devices are high-speed, low-power, octal D-type flip-flops, featuring separate D-type inputs for each flip-flop. These devices have 3-state outputs for bus-oriented applications. A buffered clock (CP) and output-enable  $(\overline{OE})$  inputs are common to all flip-flops. The eight flip-flops in the 'FCT374T store the state of their individual D inputs that meet the setup-time and hold-time requirements on the low-to-high CP transition. When  $\overline{OE}$  is low, the contents of the eight flip-flops are available at the outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state. The state of  $\overline{OE}$  does not affect the state of the flip-flops.

These devices are fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



#### **ORDERING INFORMATION**

TA	PACI	KAGE†	SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE Marking
	QSOP – Q	Tape and reel	5.2	CY74FCT374CTQCT	FCT374C
	SOIC - SO	Tube	5.2	CY74FCT374CTSOC	FCT374C
	3010 - 30	Tape and reel	5.2	CY74FCT374CTSOCT	FC1374C
	DIP – P	Tube	6.5	CY74FCT374ATPC	CY74FCT374ATPC
4000 to 0500	QSOP – Q	Tape and reel	6.5	CY74FCT374ATQCT	FCT374A
–40°C to 85°C	SOIC - SO	Tube	6.5	CY74FCT374ATSOC	FCT374A
	3010 - 30	Tape and reel	6.5	CY74FCT374ATSOCT	FC1374A
	QSOP – Q	Tape and reel	10	CY74FCT374TQCT	FCT374
	SOIC - SO	Tube	10	CY74FCT374TSOC	FCT374
	3010 - 30	Tape and reel	10	CY74FCT374TSOCT	FC1374
	CDIP – D	Tube	6.2	CY54FCT374CTDMB	
	LCC – L	Tube	6.2	CY54FCT374CTLMB	
_55°C to 125°C	CDIP – D	Tube	7.2	CY54FCT374ATDMB	
-55 0 10 125 0	LCC – L	Tube	7.2	CY54FCT374ATLMB	
	CDIP – D	Tube	11	CY54FCT374TDMB	
	LCC – L	Tube	11	CY54FCT374TLMB	

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

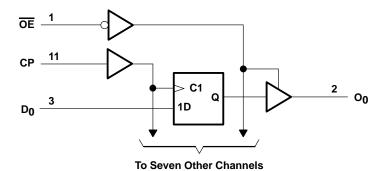
## **FUNCTION TABLE**

	INPUTS		OUTPUT
D	СР	OE	0
Н	1	L	Н
L	$\uparrow$	L	L
Х	Χ	Н	Z

H = High logic level, L = Low logic level,

X = Don't care, Z = High-impedance state, ↑ = Low-to-high clock transition

# logic diagram (positive logic)





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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range to ground potential –0	.5 V to 7 V
DC input voltage range	.5 V to 7 V
DC output voltage range	.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 1): P package	69°C/W
Q package	68°C/W
SO package	58°C/W
Ambient temperature range with power applied, T <sub>A</sub> 65°	C to 135°C
Storage temperature range, T <sub>stq</sub> –65°	C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions (see Note 2)

		CY!	54FCT37	'4T	CY	74FCT37	'4T	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
VIH	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
ІОН	High-level output current			-12			-32	mA
loL	Low-level output current			32			64	mA
TA	Operating free-air temperature	-55		125	-40		85	°C

NOTE 2: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation.



NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

# CY54FCT374T, CY74FCT374T 8-BIT REGISTERS WITH 3-STATE OUTPUTS

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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER		TEGT CONDITIO	210	CY	54FCT37	4T	CY	74FCT37	4T	
PARAMETER		TEST CONDITIO	ONS .	MIN	TYP <sup>†</sup>	MAX	MIN	TYP <sup>†</sup>	MAX	UNIT
Vers	V <sub>CC</sub> = 4.5 V,	$I_{IN} = -18 \text{ mA}$			-0.7	-1.2				V
VIK	$V_{CC} = 4.75 \text{ V},$	$I_{IN} = -18 \text{ mA}$						-0.7	-1.2	V
	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -12 \text{ mA}$		2.4	3.3					
Voн	V <sub>CC</sub> = 4.75 V	$I_{OH} = -32 \text{ mA}$					2			V
	VCC = 4.75 V	$I_{OH} = -15 \text{ mA}$					2.4	3.3		
Vol	$V_{CC} = 4.5 \text{ V},$	$I_{OL}$ = 32 mA			0.3	0.55				٧
VOL	$V_{CC} = 4.75 \text{ V},$	$I_{OL} = 64 \text{ mA}$						0.3	0.55	V
$V_{hys}$	All inputs				0.2			0.2		V
1.	$V_{CC} = 5.5 \text{ V},$	$V_{IN} = V_{CC}$				5				μΑ
lį	$V_{CC} = 5.25 \text{ V},$	$V_{IN} = V_{CC}$							5	μΑ
l., .	$V_{CC} = 5.5 \text{ V},$	$V_{1N} = 2.7 \text{ V}$				±1				μΑ
IН	$V_{CC} = 5.25 \text{ V},$	$V_{1N} = 2.7 \text{ V}$							±1	μΑ
1	$V_{CC} = 5.5 \text{ V},$	$V_{IN} = 0.5 V$				±1				μΑ
IIL	$V_{CC} = 5.25 \text{ V},$	$V_{IN} = 0.5 V$							±1	μΑ
l <sub>off</sub>	$V_{CC} = 0 V$ ,	V <sub>OUT</sub> = 4.5 V				±1			±1	μΑ
I <sub>OS</sub> ‡	$V_{CC} = 5.5 \text{ V},$	V <sub>OUT</sub> = 0 V		-60	-120	-225				mA
ios+	$V_{CC} = 5.25 \text{ V},$	V <sub>OUT</sub> = 0 V					-60	-120	-225	IIIA
lozu	$V_{CC} = 5.5 \text{ V},$	$V_{IN} = 2.7 \text{ V}$				10				μΑ
IOZH	$V_{CC} = 5.25 \text{ V},$	$V_{IN} = 2.7 \text{ V}$							10	μΑ
lo-	$V_{CC} = 5.5 \text{ V},$	$V_{IN} = 0.5 V$				-10				μΑ
IOZL	$V_{CC} = 5.25 \text{ V},$	$V_{IN} = 0.5 V$							-10	μΑ
laa	$V_{CC} = 5.5 \text{ V},$	$V_{IN} \leq 0.2 V$	$V_{IN} \ge V_{CC} - 0.2 \text{ V}$		0.1	0.2				A
lcc	V <sub>CC</sub> = 5.25 V,	V <sub>IN</sub> ≤ 0.2 V,	$V_{IN} \ge V_{CC} - 0.2 \text{ V}$					0.1	0.2	mA
Aloc	V <sub>CC</sub> = 5.5 V, V <sub>I</sub>	$N = 3.4 \text{ V}$ , $f_1 = 0$ ,	Outputs open		0.5	2				mΛ
ΔlCC	V <sub>CC</sub> = 5.25 V, V	<sub>IN</sub> = 3.4 V§, f <sub>1</sub> = 0	, Outputs open					0.5	2	mA

<sup>&</sup>lt;sup>†</sup> Typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.



Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, IOS tests should be performed last.

<sup>§</sup> Per TTL-driven input (V<sub>IN</sub> = 3.4 V); all other inputs at V<sub>CC</sub> or GND

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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

DADAMETER	TEST CONDITIONS							74FCT37	4T	UNIT
PARAMETER		1E21 CONDITIO	MIN	TYP <sup>†</sup>	MAX	MIN	TYP <sup>†</sup>	MAX	UNII	
ICCD¶		tputs open, g at 50% duty cycle $N \ge V_{CC} - 0.2 V$		0.06	0.12				mA/	
ICCD.		utputs open, g at 50% duty cycle $N \ge V_{CC} - 0.2 V$					0.06	0.12	MHz	
		One bit switching at f <sub>1</sub> = 5 MHz	$V_{IN} \le 0.2 \text{ V or}$ $V_{IN} \ge V_{CC} - 0.2 \text{ V}$		0.7	1.4				
	$V_{CC} = 5.5 \text{ V},$ $f_0 = 10 \text{ MHz},$	at 50% duty cycle	V <sub>IN</sub> = 3.4 V or GND		1.2	3.4				
	Outputs open, OE = GND	Eight bits switching at f <sub>1</sub> = 2.5 MHz	$V_{IN} \le 0.2 \text{ V or}$ $V_{IN} \ge V_{CC} - 0.2 \text{ V}$		1.6	3.2				
l <sub>C</sub>		at 50% duty cycle	V <sub>IN</sub> = 3.4 V or GND		3.9	12.2				mA
10		One bit switching at f <sub>1</sub> = 5 MHz	$V_{IN} \le 0.2 \text{ V or}$ $V_{IN} \ge V_{CC} - 0.2 \text{ V}$					0.7	1.4	IIIA
	$V_{CC} = 5.25 \text{ V},$ $f_0 = 10 \text{ MHz},$	at 50% duty cycle	V <sub>IN</sub> = 3.4 V or GND					1.2	3.4	
	Outputs open, OE = GND	Eight bits switching at f <sub>1</sub> = 2.5 MHz	$V_{IN} \le 0.2 \text{ V or}$ $V_{IN} \ge V_{CC} - 0.2 \text{ V}$					1.6	3.2	
		at 50% duty cycle	V <sub>IN</sub> = 3.4 V or GND					3.9	12.2	
Ci				5	10		5	10	pF	
Co					9	12		9	12	pF

<sup>†</sup> Typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

Where:

I<sub>C</sub> = Total supply current

ICC = Power-supply current with CMOS input levels

 $\Delta I_{CC}$  = Power-supply current for a TTL high input ( $V_{IN} = 3.4 \text{ V}$ )

D<sub>H</sub> = Duty cycle for TTL inputs high N<sub>T</sub> = Number of TTL inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic current caused by an input transition pair (HLH or LHL)

f<sub>0</sub> = Clock frequency for registered devices, otherwise zero

f<sub>1</sub> = Input signal frequency

 $N_1$  = Number of inputs changing at  $f_1$ 

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I<sub>CC</sub> formula.



<sup>¶</sup> This parameter is derived for use in total power-supply calculations.

 $<sup>^{\#}</sup>$ IC = ICC +  $\Delta$ ICC  $\times$  DH  $\times$  NT + ICCD (f<sub>0</sub>/2 + f<sub>1</sub>  $\times$  N<sub>1</sub>)

# CY54FCT374T, CY74FCT374T 8-BIT REGISTERS WITH 3-STATE OUTPUTS

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# timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		CY54FC	T374T	CY54FCT	374AT	CY54FCT	374CT	UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
t <sub>W</sub>	Pulse duration, CP high or low	7		6		6		ns
t <sub>su</sub>	Setup time, data before CP↑	2		2		2		ns
th	Hold time, data after CP↑	1.5		1.5		1.5		ns

# timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		CY74FC	T374T	CY74FCT	374AT	CY74FCT	374CT	UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
t <sub>W</sub>	Pulse duration, CP high or low	7		5		5		ns
t <sub>su</sub>	Setup time, data before CP↑	2		2		2		ns
th	Hold time, data after CP↑	1.5		1.5		1.5		ns

## switching characteristics over operating free-air temperature range (see Figure 1)

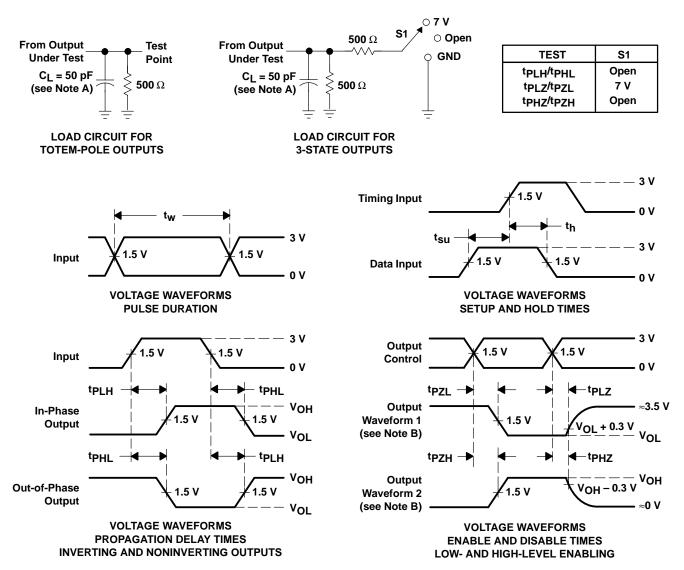
PARAMETER	FROM	то	CY54FC	T374T	CY54FC	Г374АТ	CY54FC1	374CT	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
t <sub>PLH</sub>	СР	0	2	11	2	7.2	2	6.2	no
t <sub>PHL</sub>	CF	O	2	11	2	7.2	2	6.2	ns
<sup>t</sup> PZH	ŌĒ	0	1.5	14	1.5	7.5	1.5	6.2	no
t <sub>PZL</sub>	OE	U	1.5	14	1.5	7.5	1.5	6.2	ns
<sup>t</sup> PHZ	ŌĒ	0	1.5	8	1.5	6.5	1.5	5.7	no
tPLZ	OE	U	1.5	8	1.5	6.5	1.5	5.7	ns

## switching characteristics over operating free-air temperature range (see Figure 1)

DADAMETED	FROM	то	CY74FC	T374T	CY74FC	Г374АТ	CY74FCT	374CT	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	UNII
<sup>t</sup> PLH	СР	0	2	10	2	6.5	2	5.2	20
<sup>t</sup> PHL	CF	U	2	10	2	6.5	2	5.2	ns
<sup>t</sup> PZH	ŌĒ	0	1.5	12.5	1.5	6.5	1.5	5.5	20
<sup>t</sup> PZL	OE		1.5	12.5	1.5	6.5	1.5	5.5	ns
<sup>t</sup> PHZ	ŌĒ	0	1.5	8	1.5	5.5	1.5	5	20
<sup>t</sup> PLZ	] OE	l	1.5	8	1.5	5.5	1.5	5	ns



#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>I</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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## **PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-9221802M2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9221802M2A CY54FCT 374TLMB
5962-9221802MRA	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9221802MR A CY54FCT374TDMB
5962-9221804M2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9221804M2A CY54FCT 374ATLMB
5962-9221804MRA	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9221804MR A CY54FCT374ATDM B
5962-9221806M2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9221806M2A CY54FCT 374CTLMB
CY54FCT374ATDMB	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9221804MR A CY54FCT374ATDM B
CY54FCT374ATLMB	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-	5962- 9221804M2A CY54FCT 374ATLMB
CY54FCT374CTLMB	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9221806M2A CY54FCT 374CTLMB
CY54FCT374TDMB	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9221802MR A CY54FCT374TDMB





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Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
CY54FCT374TLMB	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9221802M2A CY54FCT 374TLMB
CY74FCT374ATPC	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	CY74FCT374ATPC
CY74FCT374ATPC.B	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	CY74FCT374ATPC
CY74FCT374ATQCT	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT374A
CY74FCT374ATQCT.B	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT374A
CY74FCT374ATSOC	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT374A
CY74FCT374ATSOC.B	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT374A
CY74FCT374ATSOCT	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT374A
CY74FCT374ATSOCT.B	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT374A
CY74FCT374CTSOC	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT374C
CY74FCT374CTSOC.B	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT374C
CY74FCT374TQCT	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT374
CY74FCT374TQCT.B	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT374
CY74FCT374TSOC	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT374
CY74FCT374TSOC.B	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT374

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.



# **PACKAGE OPTION ADDENDUM**

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(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# **PACKAGE MATERIALS INFORMATION**

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## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

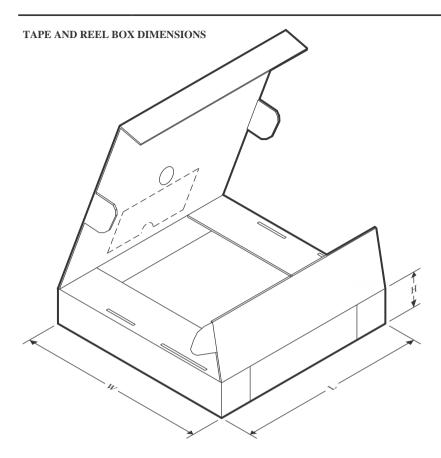
#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT374ATQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT374ATSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CY74FCT374TQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

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### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT374ATQCT	SSOP	DBQ	20	2500	353.0	353.0	32.0
CY74FCT374ATSOCT	SOIC	DW	20	2000	356.0	356.0	45.0
CY74FCT374TQCT	SSOP	DBQ	20	2500	353.0	353.0	32.0

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## **TUBE**



\*All dimensions are nominal

						0		
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9221802M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9221804M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9221806M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
CY54FCT374ATLMB	FK	LCCC	20	55	506.98	12.06	2030	NA
CY54FCT374CTLMB	FK	LCCC	20	55	506.98	12.06	2030	NA
CY54FCT374TLMB	FK	LCCC	20	55	506.98	12.06	2030	NA
CY74FCT374ATPC	N	PDIP	20	20	506	13.97	11230	4.32
CY74FCT374ATPC.B	N	PDIP	20	20	506	13.97	11230	4.32
CY74FCT374ATSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT374ATSOC.B	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT374CTSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT374CTSOC.B	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT374TSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT374TSOC.B	DW	SOIC	20	25	507	12.83	5080	6.6

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