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Dual N-Channel NexFET™ Power MOSFET

Check for Samples: CSD86311W1723

FEATURES

- **Dual N-Ch MOSFETs**
- **Common Source Configuration**
- Small Footprint 1.7 mm × 2.3 mm
- Ultra Low Q_q and Q_{qd}
- Pb Free
- **RoHS Compliant**
- **Halogen Free**

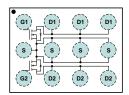
APPLICATIONS

- **Battery Management**
- **Battery Protection**
- **DC-DC Converters**

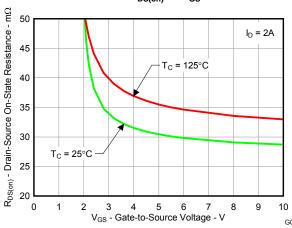
DESCRIPTION

The device has been designed to deliver the lowest on resistance and gate charge in the smallest outline possible with thermal characteristics in an ultra low profile. Low on resistance and gate charge coupled with the small footprint and low profile make the device ideal for battery operated space constrained application in load management as well as DC-DC converter applications

Top View



R_{DS(on)} vs V_{GS}



PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	25	V	
Q_g	Gate Charge Total (4.5V) 3.1			nC
Q_{gd}	Gate Charge Gate to Drain 0.33			nC
		V _{GS} = 2.5V	37	mΩ
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 4.5V 31		mΩ
		V _{GS} = 8V	29	mΩ
V _{GS(th)}	Threshold Voltage 1			V

ORDERING INFORMATION

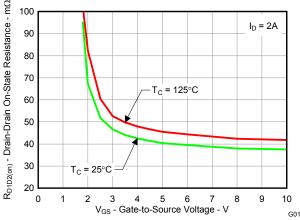
Device	Package	Media	Qty	Ship
CSD86311W1723	1.7-mm × 2.3-mm Wafer Level Package	7-inch reel	3000	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

T _A = 2	5°C unless otherwise stated	VALUE	UNIT
V_{DS}	Drain to Source Voltage	25	٧
V_{GS}	Gate to Source Voltage	+10 / -8	V
	Continuous Drain Current (1) (2)(3)	4.5	
I _D	Pulsed Drain Current (1) (2)(3)	4.5	Α
	Continuous Gate Clamp Current (4)		
I _G	Pulsed Gate Clamp Current (4)	6	Α
P_D	Power Dissipation (1)	1.5	W
T _J , T _{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C

- (1) May be limited by Max source current
- (2) Based on Min Cu footprint
- (3) Per MOSFET
- (4) Total for device







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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$

	PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT
Static Cl	haracteristics			-	
BV _{DSS}	Drain to Source Voltage	$V_{GS} = 0V, I_D = 250\mu A$	25		V
I _{DSS}	Drain to Source Leakage Current	V _{GS} = 0V, V _{DS} = 20V		1	μΑ
I _{GSS}	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = +10 / -8V$		±100	nA
V _{GS(th)}	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	0.85 1	1.4	٧
		V _{GS} = 2.5V, I _{DS} = 2A	37	51	mΩ
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 4.5V, I _{DS} = 2A	31	42	mΩ
		V _{GS} = 8V, I _{DS} = 2A	29	39	mΩ
		$V_{GS} = 2.5V, I_D = 2A$	52	75	mΩ
R _{DD(on)}	Drain to Drain On Resistance	V _{GS} = 4.5V, I _{DS} = 2A	41	55	mΩ
		V _{GS} = 8V, I _{DS} = 2A	38	50	mΩ
g _{fs} Transconductance		V _{DS} = 10V, I _D = 2A	6.4		S
Dynamic	Characteristics	,		•	
C _{ISS}	Input Capacitance	V _{GS} = 0V,	450	585	pF
Coss	Output Capacitance	$V_{DS} = 12.5V$,	250	325	pF
C _{RSS}	Reverse Transfer Capacitance	f = 1MHz	10	13	pF
R _G	Seried Gate Resistance		1.4	2.8	Ω
Qg	Gate Charge Total (4.5V)		3.1	4	nC
Q _{gd}	Gate Charge Gate to Drain	V _{DS} = 12.5V,	0.33		nC
Q _{gs}	Gate Charge Gate to Source	$I_D = 2A$	0.85		nC
Q _{g(th)}	Gate Charge at Vth		0.48		nC
Q _{OSS}	Output Charge	$V_{DS} = 12.2V, V_{GS} = 0V$	4.5		nC
t _{d(on)}	Turn On Delay Time		5.4		ns
t _r	Rise Time	V _{DS} = 12.5V, V _{GS} = 4.5V,	4.3		ns
t _{d(off)}	Turn Off Delay Time	$I_D = 2A, R_G = 2\Omega$	13.2		ns
t _f	Fall Time		2.9		ns
Diode CI	haracteristics				
V _{SD}	Diode Forward Voltage	I _S = 2A, V _{GS} = 0V	0.78	1	V
Q _{rr}	Reverse Recovery Charge	V _{dd} = 12.2V, I _F = 2A,	4.2		nC
t _{rr}	Reverse Recovery Time	di/dt = 300A/μs	13.4		ns

THERMAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

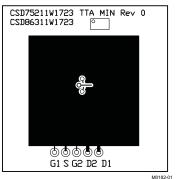
	PARAMETER	MIN	TYP	MAX	UNIT
Rθ	Thermal Resistance Junction to Ambient (Minimum Cu area) (1) (2)			165	°C/W
R _θ	Thermal Resistance Junction to Ambient (1 in ² Cu area) (2) (3)			68	°C/W

- (1) Device mounted on FR4 material with minimum Cu mounting area.
- (2) Measured with both devices biased in a parallel condition.
- (3) Device mounted on FR4 material with 1 in² of 2oz. Cu.

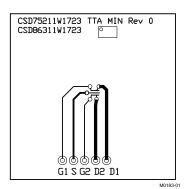
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Max $R_{\theta JA} = 68^{\circ}\text{C/W}$ when mounted on 1inch² of 2 oz. Cu.



Max $R_{\theta JA} = 165^{\circ}\text{C/W}$ when mounted on minimum pad area of 2 oz. Cu.

TYPICAL MOSFET CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

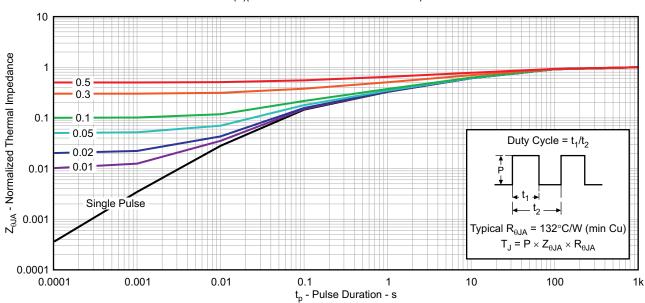


Figure 1. Transient Thermal Impedance

G012

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TYPICAL MOSFET CHARACTERISTICS (continued)

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$

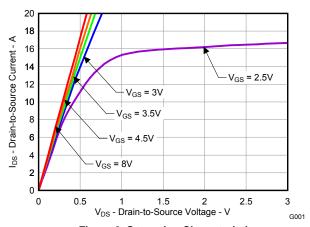
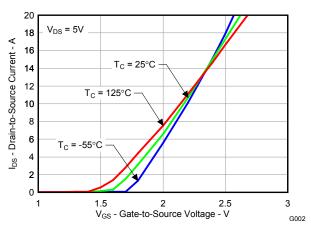


Figure 2. Saturation Characteristics



ISTRUMENTS

Figure 3. Transfer Characteristics

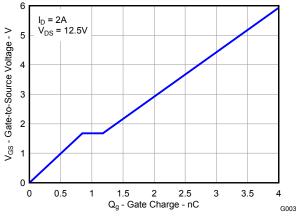


Figure 4. Gate Charge

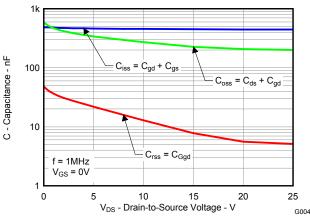


Figure 5. Capacitance

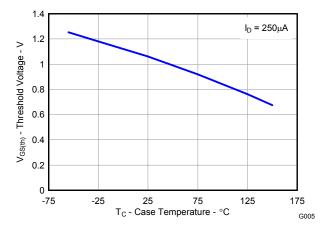


Figure 6. Threshold Voltage vs. Temperature

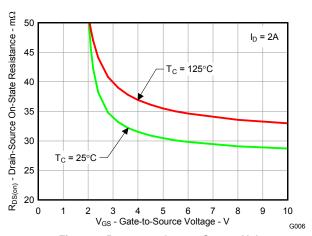


Figure 7. $R_{DS(on)}$ vs. Gate-to-Source Voltage



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TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

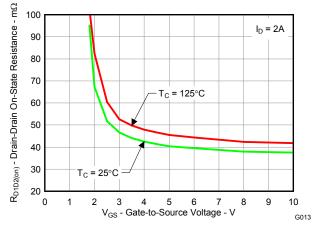


Figure 8. R_{D1D2(on)} vs. Gate-to-Source Voltage

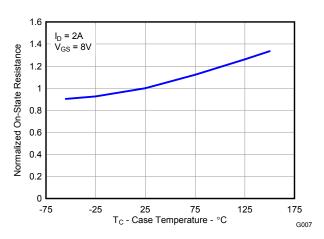


Figure 9. On Resistance vs. Temperature

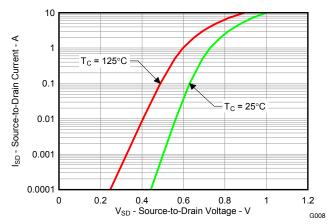


Figure 10. Typical Diode Forward Voltage

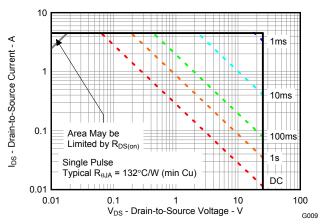


Figure 11. Maximum Safe Operating Area

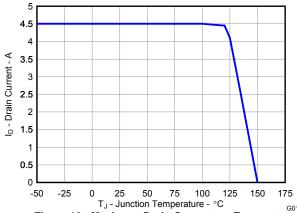
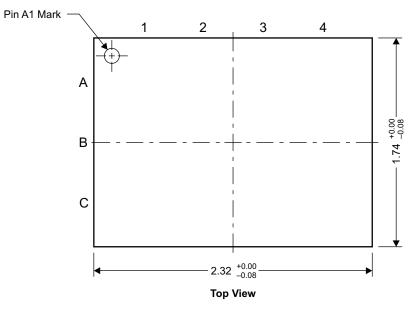


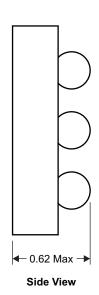
Figure 12. Maximum Drain Current vs. Temperature

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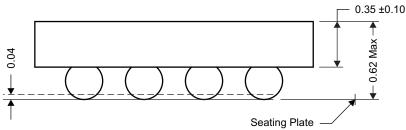
MECHANICAL DATA

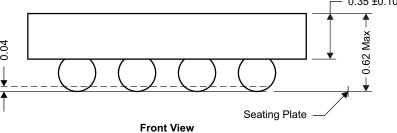
CSD86311W1723 Package Dimensions

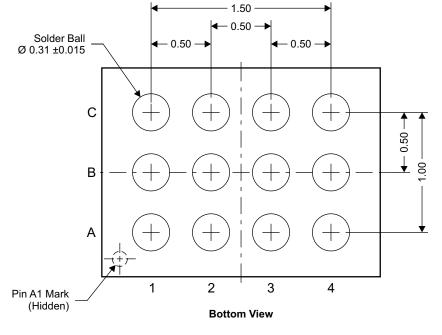




INSTRUMENTS







Pinout					
Position	Designation				
A2, A3, A4	Drain 1				
C2, C3, C4	Drain 2				
A1	Gate 1				
C1	Gate 2				
B1, B2, B3, B4	Source				

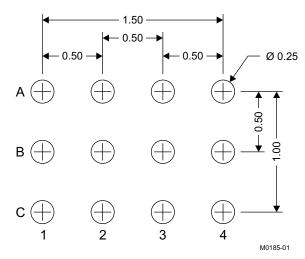
M0184-01

NOTE: All dimensions are in mm (unless otherwise specified)



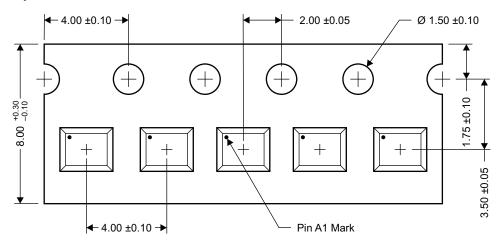
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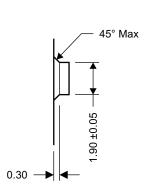
Land Pattern Recommendation



NOTE: All dimensions are in mm (unless otherwise specified)

Tape and Reel Information







M0186-01

NOTE: All dimensions are in mm (unless otherwise specified)

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
CSD86311W1723	Active	Production	DSBGA (YZG) 12	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 150	86311
CSD86311W1723.B	Active	Production	DSBGA (YZG) 12	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 150	86311

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD86311W1723	DSBGA	YZG	12	3000	180.0	8.4	2.38	1.8	0.69	4.0	8.0	Q2

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Ì	Device	Device Package Type		Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
ı	CSD86311W1723	DSBGA	YZG	12	3000	182.0	182.0	20.0	

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