



CSD85302L 20 V Dual N-Channel NexFET™ Power MOSFET

1 Features

- Common Drain Configuration
- Low On-Resistance
- Small Footprint of 1.35 mm × 1.35 mm
- Pb Free and Halogen Free
- RoHS Compliant
- ESD HBM Protection >2.5 kV

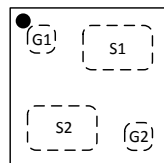
2 Applications

- USB Type-C/PD
- Battery Management
- Battery Protection

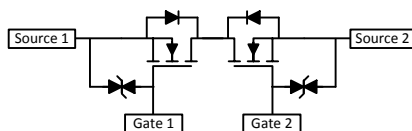
3 Description

This 20 V, 18.7 mΩ, 1.35 mm × 1.35 mm LGA Dual NexFET™ power MOSFET is designed to minimize resistance in the smallest footprint. Its small footprint and common drain configuration make the device ideal for battery-powered applications in small handheld devices.

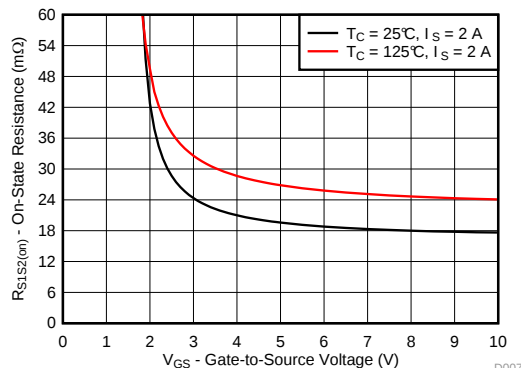
Top View



Configuration

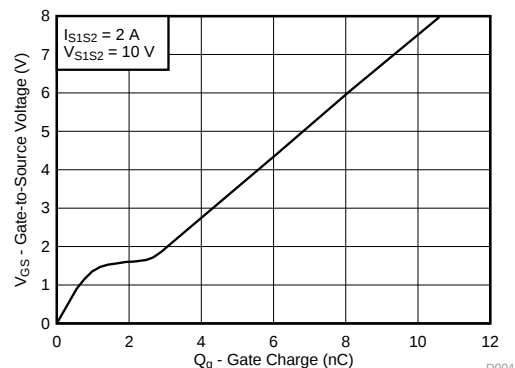


$R_{DS(on)}$ vs V_{GS}



D007

Gate Charge



D004

Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE	UNIT
V_{S1S2}	Source-to-Source Voltage	20	V
Q_g	Gate Charge Total (4.5 V)	6	nC
Q_{gd}	Gate Charge Gate-to-Drain	1.4	nC
$R_{S1S2(on)}$	Source-to-Source On-Resistance	$V_{GS} = 2.5\text{ V}$	29 mΩ
		$V_{GS} = 4.5\text{ V}$	20 mΩ
		$V_{GS} = 6.5\text{ V}$	18.7 mΩ
$V_{GS(th)}$	Threshold Voltage	0.9	V

Ordering Information⁽¹⁾

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD85302L	3000	7-Inch Reel	1.35 × 1.35 mm Land Grid Array (LGA) Package	Tape and Reel
CSD85302LT	250			

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{S1S2}	Source-to-Source Voltage	20	V
V_{GS}	Gate-to-Source Voltage	±10	V
I_S	Continuous Source Current ⁽¹⁾	7	A
I_{SM}	Pulsed Source Current ⁽²⁾	37	A
P_D	Power Dissipation ⁽¹⁾	1.7	W
$V_{(ESD)}$	Human Body Model (HBM)	2.5	kV
T_J , T_{stg}	Operating Junction and Storage Temperature Range	–55 to 150	°C

(1) Typical $R_{\theta JA} = 75^\circ\text{C/W}$ when mounted on a 1 inch², 2 oz. Cu pad on a 0.06 inch thick FR4 PCB.

(2) Max $R_{\theta JA} = 90^\circ\text{C/W}$, pulse duration ≤100 μs, duty cycle ≤1%



Table of Contents

1 Features	1	6.1 Community Resources.....	7
2 Applications	1	6.2 Trademarks	7
3 Description	1	6.3 Electrostatic Discharge Caution	7
4 Revision History	2	6.4 Glossary	7
5 Specifications	3	7 Mechanical, Packaging, and Orderable Information	8
5.1 Electrical Characteristics.....	3	7.1 Package Dimensions	8
5.2 Thermal Information	3	7.2 Recommended PCB Pattern.....	9
5.3 Typical MOSFET Characteristics.....	4	7.3 Recommended Stencil Pattern	9
6 Device and Documentation Support	7	7.4 Q3A Tape and Reel Information	10

4 Revision History

DATE	REVISION	NOTES
November 2015	*	Initial release.

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{S1S2}	Source-to-source voltage	V _{GS} = 0 V, I _S = 250 μA	20			V
I _{S1S2}	Source-to-source leakage current	V _{GS} = 0 V, V _{S1S2} = 16 V			1	μA
I _{GSS}	Gate-to-source leakage current	V _{S1S2} = 0 V, V _{GS} = 6 V			0.5	μA
		V _{S1S2} = 0 V, V _{GS} = 10V			4	μA
V _{GS(th)}	Gate-to-source threshold voltage	V _{S1S2} = V _{GS} , I _S = 250 μA	0.68	0.9	1.3	V
R _{S1S2(on)}	Source-to-source on-resistance	V _{GS} = 2.5 V, I _S = 2 A	20	29	36	mΩ
		V _{GS} = 4.5 V, I _S = 2 A	14	20	24	mΩ
		V _{GS} = 6.5 V, I _S = 2 A	13	18.7	22.5	mΩ
g _{fs}	Transconductance	V _{S1S2} = 2 V, I _S = 2 A		19		S
DYNAMIC CHARACTERISTICS⁽¹⁾						
C _{iss}	Input capacitance	V _{GS} = 0 V, V _{S1S2} = 10 V, f = 1 MHz		718	933	pF
C _{oss}	Output capacitance			92	120	pF
C _{rss}	Reverse transfer capacitance			61	79	pF
Q _g	Gate charge total (4.5 V)	V _{S1S2} = 10 V, I _S = 2 A		6.0	7.8	nC
Q _{gd}	Gate charge gate-to-drain			1.4		nC
Q _{gs}	Gate charge gate-to-source			1.2		nC
Q _{g(th)}	Gate charge at V _{th}			0.6		nC
Q _{oss}	Output charge	V _{S1S2} = 10 V, V _{GS} = 0 V		2.3		nC
t _{d(on)}	Turn-on delay time	V _{S1S2} = 10 V, V _{GS} = 4.5 V, I _{S1S2} = 2 A, R _G = 0 Ω		37		ns
t _r	Rise time			54		ns
t _{d(off)}	Turn-off delay time			173		ns
t _f	Fall time			99		ns

(1) Charge and timing values specified are per single FET.

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

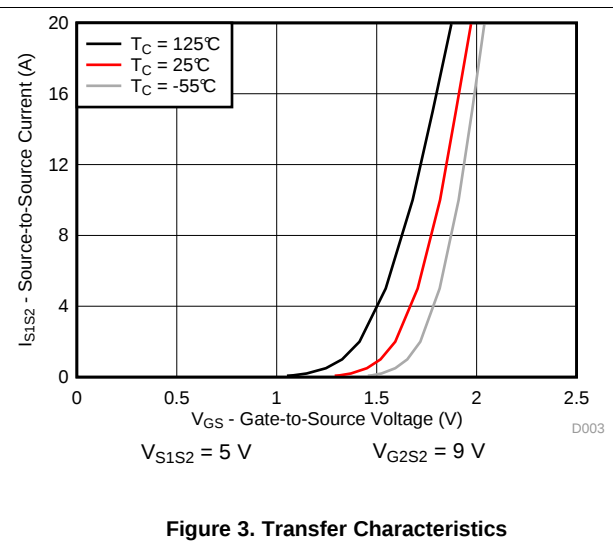
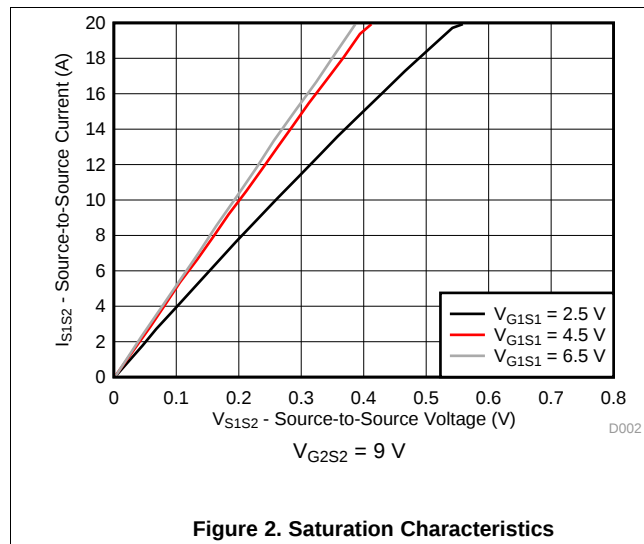
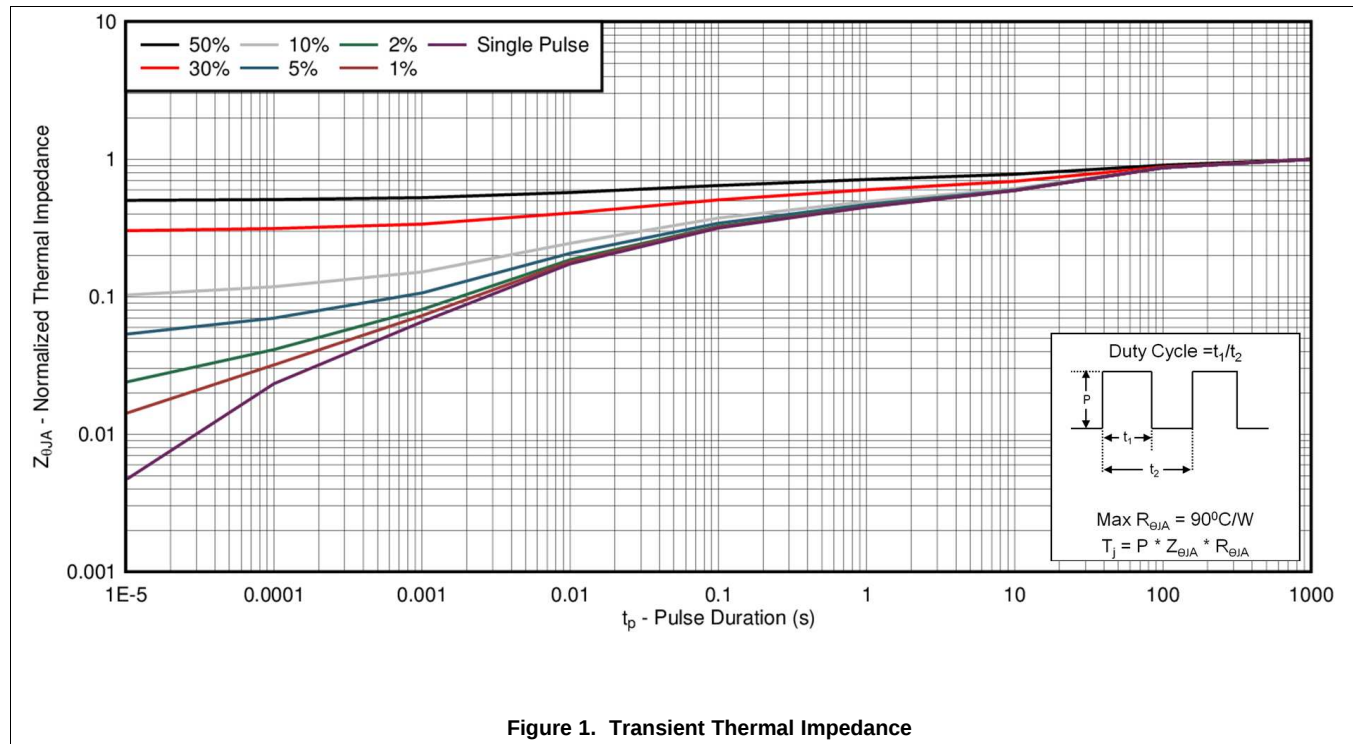
THERMAL METRIC		MIN	TYP	MAX	UNIT
R _{θJA}	Junction-to-ambient thermal resistance ⁽¹⁾		75		°C/W
	Junction-to-ambient thermal resistance ⁽²⁾		175		°C/W

(1) Device mounted on FR4 material with 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu.

(2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)



Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

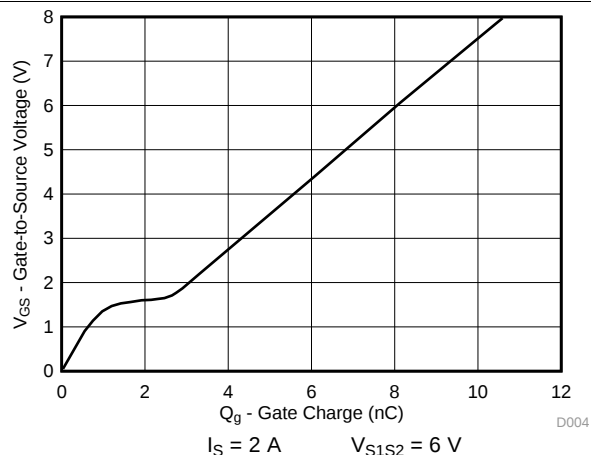


Figure 4. Gate Charge

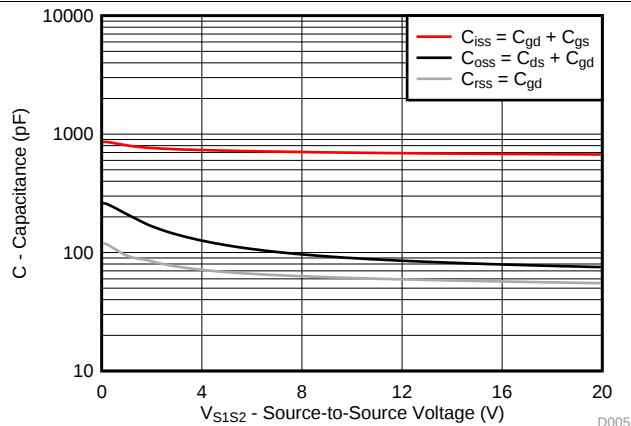


Figure 5. Capacitance

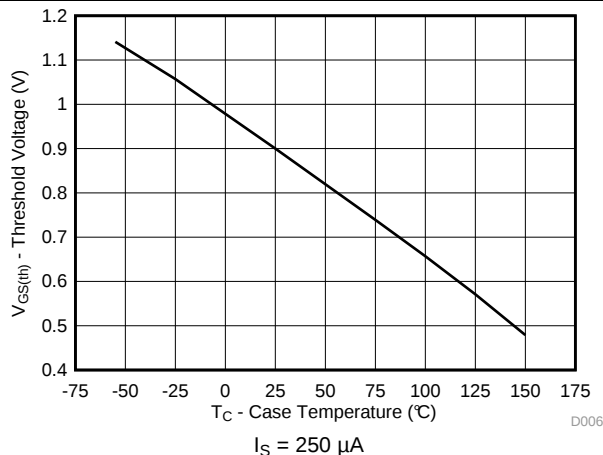


Figure 6. Threshold Voltage vs Temperature

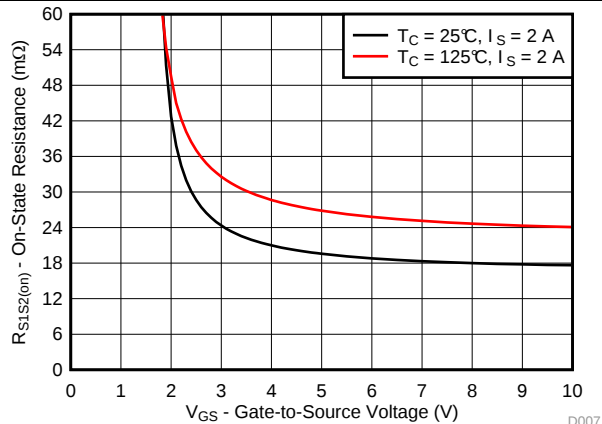


Figure 7. On-State Source-to-Source Resistance vs Gate-to-Source Voltage

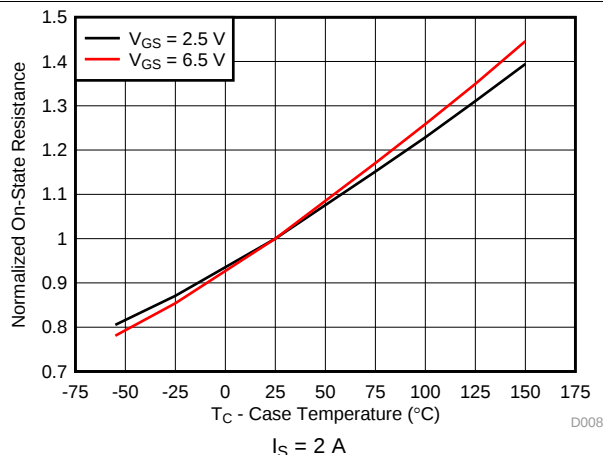


Figure 8. Normalized On-State Resistance vs Temperature

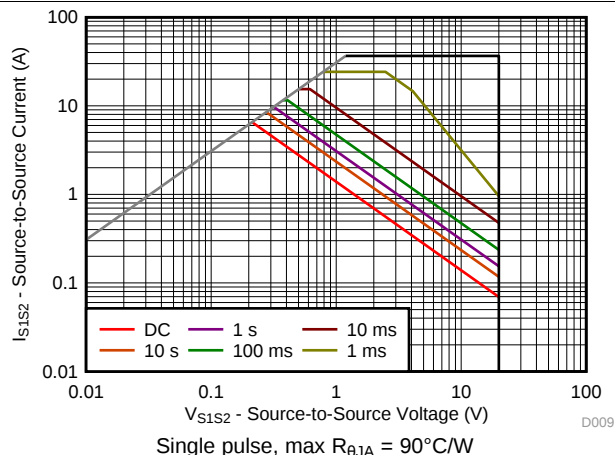


Figure 9. Maximum Safe Operating Area

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

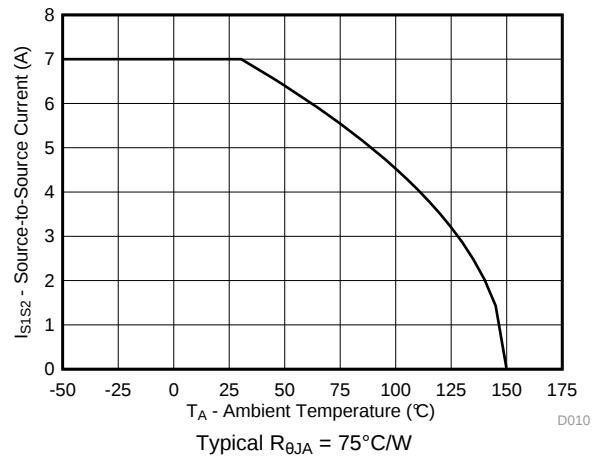


Figure 10. Maximum Source Current vs Temperature

6 Device and Documentation Support

6.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.2 Trademarks

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.4 Glossary

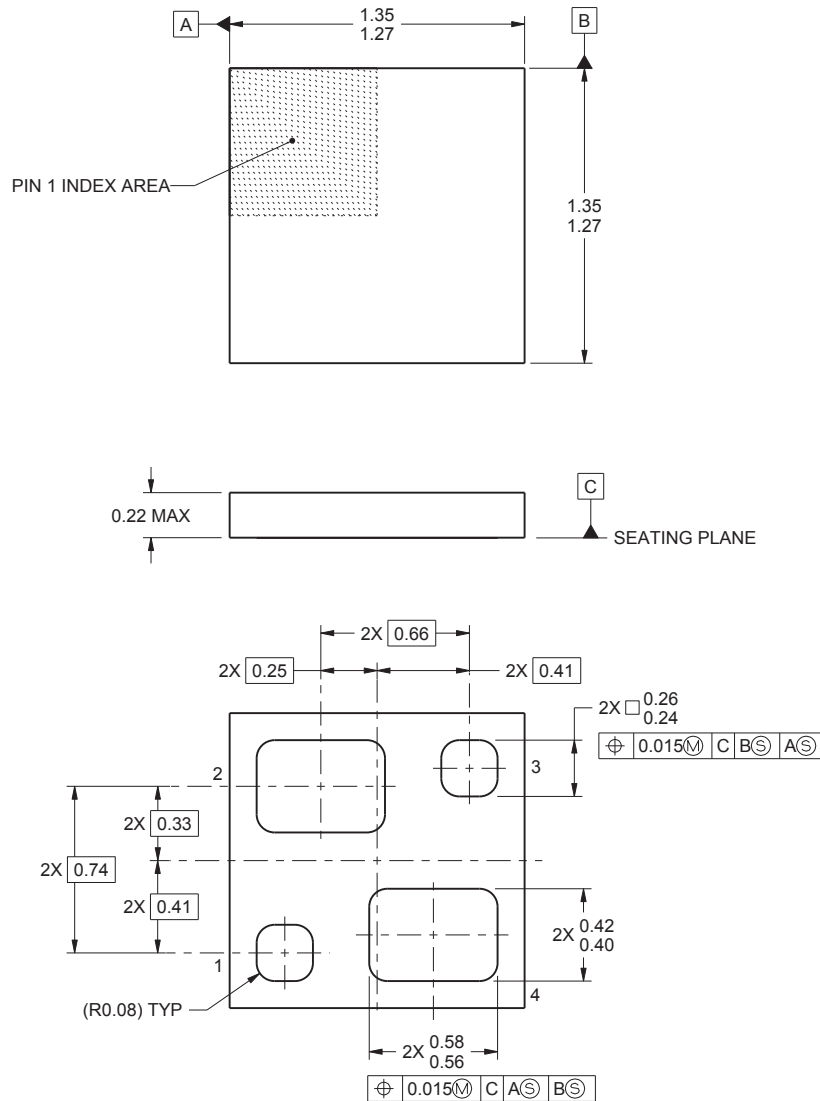
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Package Dimensions

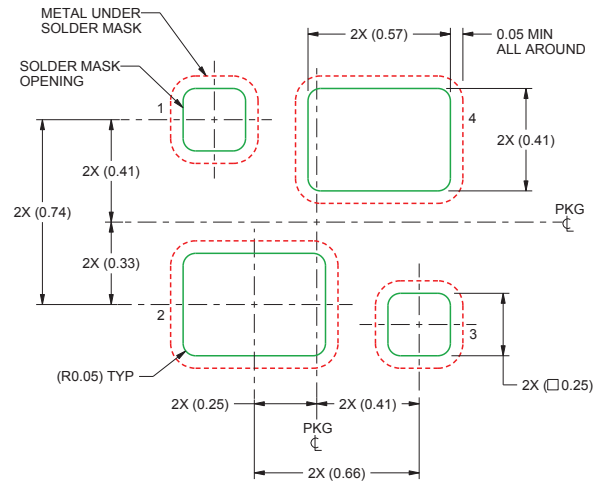


Pin Configuration

PIN NUMBER	NAME
1	G1
2	S2
3	G2
4	S1

- All linear dimensions are in millimeters.

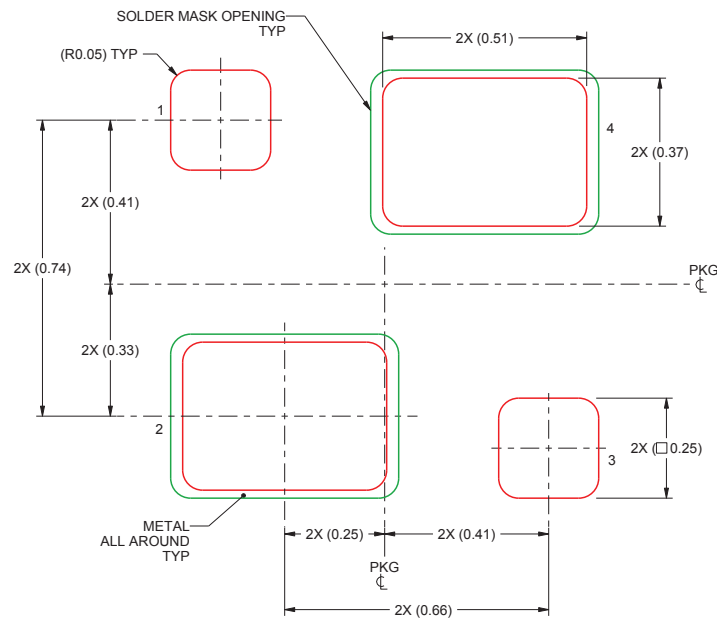
7.2 Recommended PCB Pattern



Land Pattern Example

Solder Mask Defined
Scale: 50X

7.3 Recommended Stencil Pattern

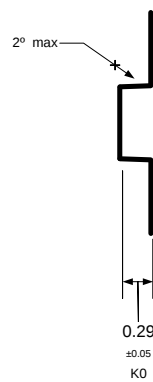
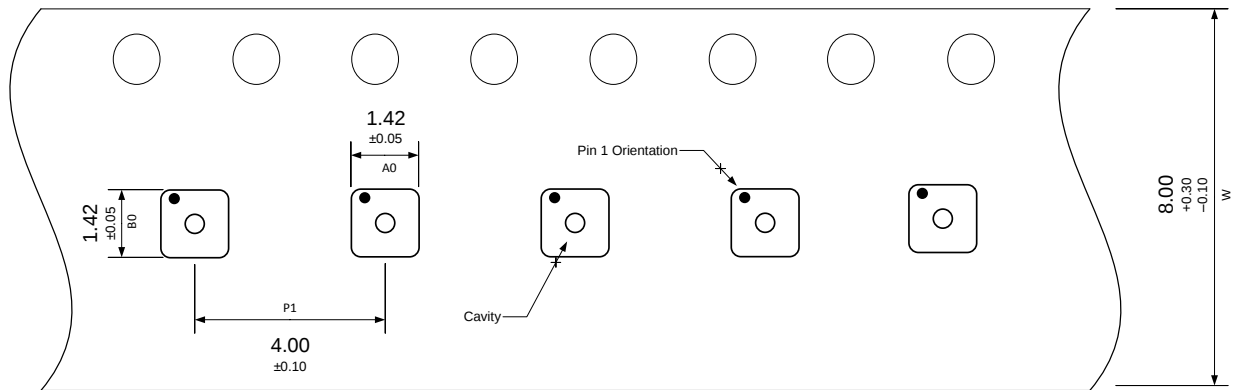


Solder Paste Example

Based on 0.1 mm thick stencil
Pads 2 and 4: 81% printed on solder coverage by area
Scale: 80X

1. All linear dimensions are in millimeters.
2. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

7.4 Q3A Tape and Reel Information



All Measurements in
Millimeters (mm)

- Notes:
1. 10-sprocket hole-pitch cumulative tolerance ± 0.2
 2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
 3. Material: black static-dissipative polystyrene
 4. MSL1 260°C (IR and convection) PbF-reflow compatible

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD85302L	Active	Production	PICOSTAR (YME) 4	3000 LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	85302
CSD85302L.B	Active	Production	PICOSTAR (YME) 4	3000 LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	85302
CSD85302LT	Active	Production	PICOSTAR (YME) 4	250 SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	85302
CSD85302LT.B	Active	Production	PICOSTAR (YME) 4	250 SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	85302

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated