CSD19532KTT 100V N-Channel NexFET™ Power MOSFET

1 Features

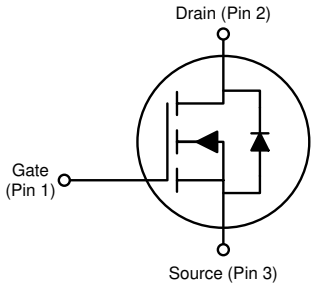
- Ultra-low Q_g and Q_{gd}
- Low thermal resistance
- Avalanche rated
- Pb-free terminal plating
- RoHS compliant
- Halogen free
- D^2PAK plastic package

2 Applications

- Secondary side synchronous rectifier
- Hot swap
- Motor control

3 Description

This 100V, 4.6mΩ, D^2PAK (TO-263) NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



Pin Out

Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	100		V
Q_g	Gate Charge Total (10V)	44		nC
Q_{gd}	Gate Charge Gate to Drain	5.6		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 6V	5.3	mΩ
		V_{GS} = 10V	4.6	mΩ
$V_{GS(th)}$	Threshold Voltage	2.6		V

Ordering Information (1)

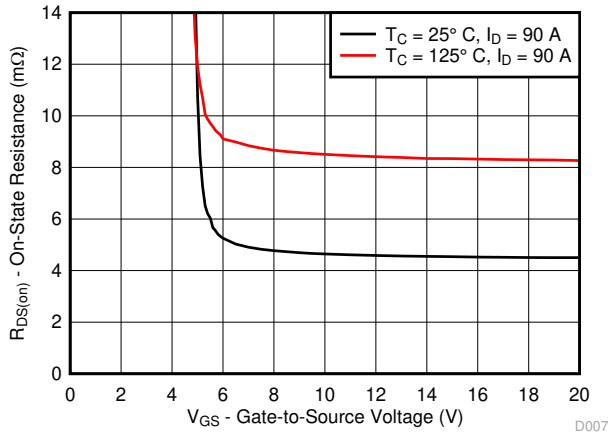
DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD19532KTT	500	13-Inch Reel	D^2PAK Plastic Package	Tape & Reel
CSD19532KTTT	50			

(1) For all available packages, see the orderable addendum at the end of the data sheet.

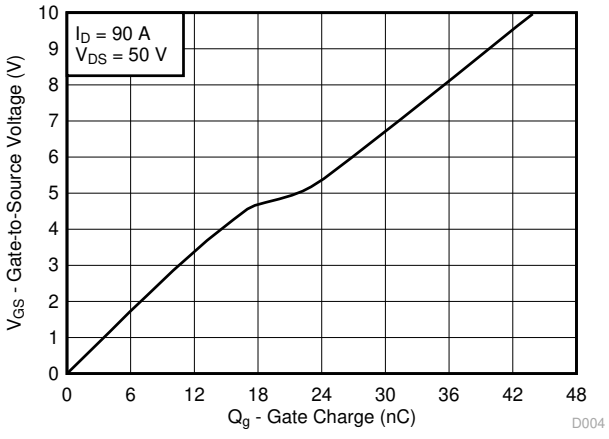
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	100	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package limited)	200	A
	Continuous Drain Current (Silicon limited), T_C = 25°C	136	
	Continuous Drain Current (Silicon limited), T_C = 100°C	98	
I_{DM}	Pulsed Drain Current (1)	400	A
P_D	Power Dissipation	250	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	–55 to 175	°C
E_{AS}	Avalanche Energy, single pulse I_D = 72A, L = 0.1mH, R_G = 25Ω	259	mJ

(1) Max $R_{\theta JC}$ = 0.6°C/W, Pulse duration ≤ 100µs, Duty cycle ≤ 1%



$R_{DS(on)}$ vs V_{GS}



Gate Charge

Table of Contents

4 Specifications

4.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0V, I_D = 250µA	100			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0V, V_{DS} = 80V			1	µA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0V, V_{GS} = 20V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	2.2	2.6	3.2	V
$R_{DS(on)}$	Drain-to-source on resistance	V_{GS} = 6V, I_D = 90A		5.3	6.6	mΩ
		V_{GS} = 10V, I_D = 90A		4.6	5.6	mΩ
g_{fs}	Transconductance	V_{DS} = 10V, I_D = 90A		113		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0V, V_{DS} = 50V, f = 1MHz		3890	5060	pF
C_{oss}	Output capacitance			674	876	pF
C_{rss}	Reverse transfer capacitance			14	18	pF
R_G	Series gate resistance			1.3	2.6	Ω
Q_g	Gate charge total (10 V)	V_{DS} = 50V, I_D = 90A		44	57	nC
Q_{gd}	Gate charge gate to drain			5.6		nC
Q_{gs}	Gate charge gate to source			17		nC
$Q_{g(th)}$	Gate charge at V_{th}			9.6		nC
Q_{oss}	Output charge	V_{DS} = 50V, V_{GS} = 0V		124		nC
$t_{d(on)}$	Turn on delay time	V_{DS} = 50V, V_{GS} = 10V, I_{DS} = 90A, R_G = 0Ω		9		ns
t_r	Rise time			3		ns
$t_{d(off)}$	Turn off delay time			14		ns
t_f	Fall time			2		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 90A, V_{GS} = 0V		0.9	1.0	V
Q_{rr}	Reverse recovery charge	V_{DS}= 50V, I_F = 90A, di/dt = 300A/µs		326		nC
t_{rr}	Reverse recovery time			74		ns

4.2 Thermal Information

(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance			0.6	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance			62	°C/W

4.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

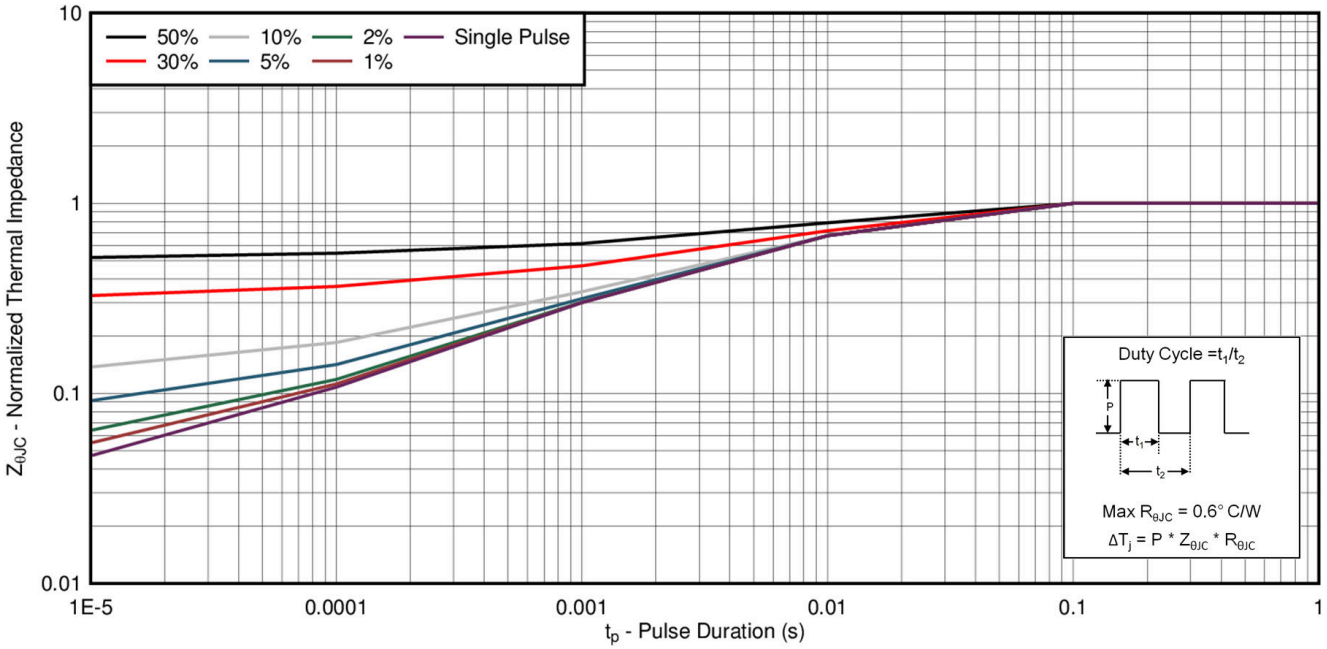


Figure 4-1. Transient Thermal Impedance

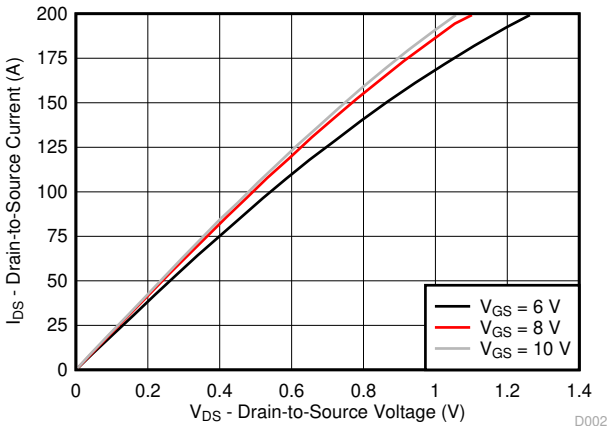
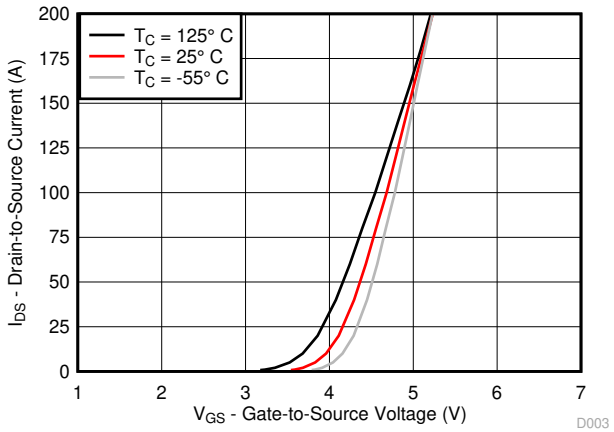
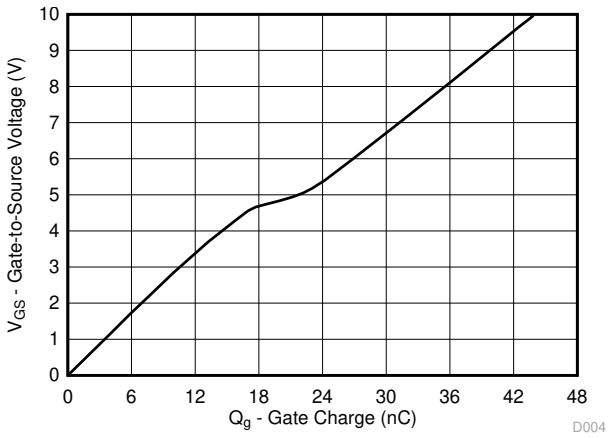


Figure 4-2. Saturation Characteristics



VDS = 5V

Figure 4-3. Transfer Characteristics



V_{DS} = 50V I_D = 90A

Figure 4-4. Gate Charge

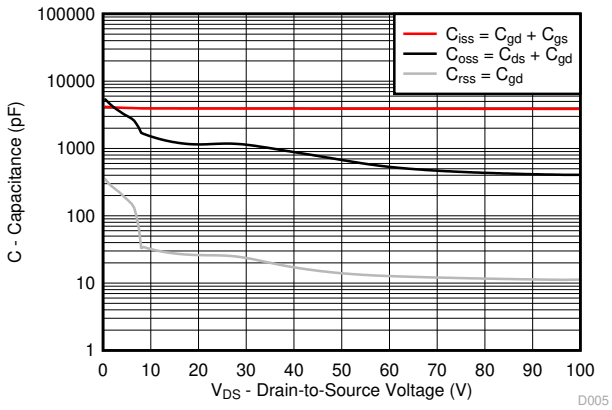
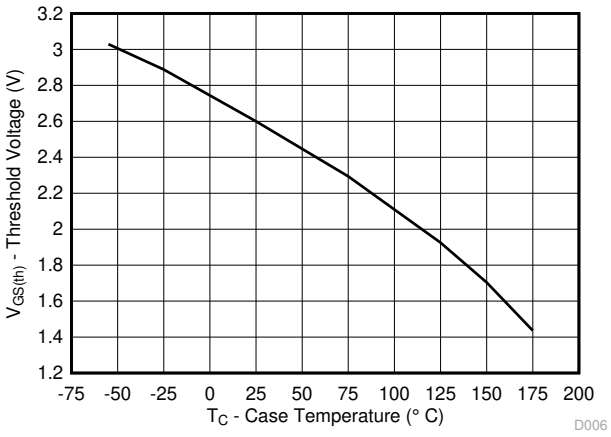


Figure 4-5. Capacitance



I_D = 250µA

Figure 4-6. Threshold Voltage vs Temperature

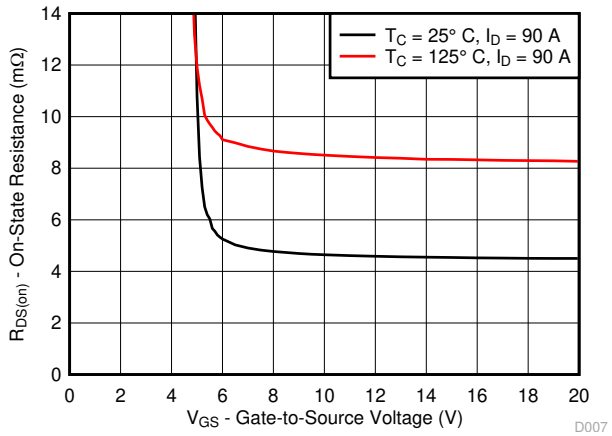
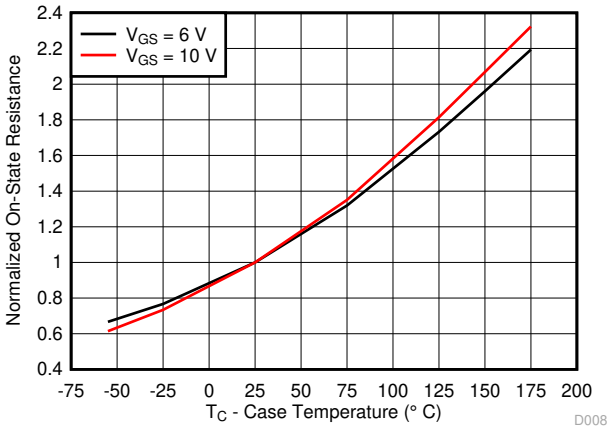


Figure 4-7. On-State Resistance vs Gate-to-Source Voltage



I_D = 90A

Figure 4-8. Normalized On-State Resistance vs Temperature

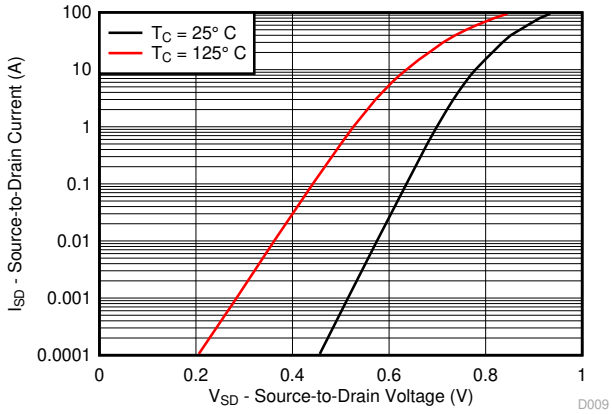
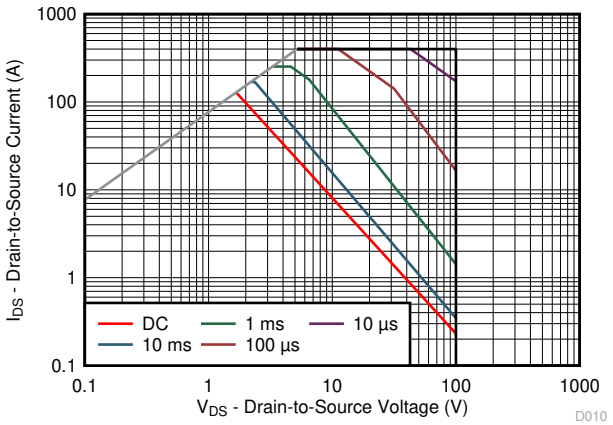


Figure 4-9. Typical Diode Forward Voltage



Single Pulse, Max $R_{\theta JC}$ = 0.6°C/W

Figure 4-10. Maximum Safe Operating Area

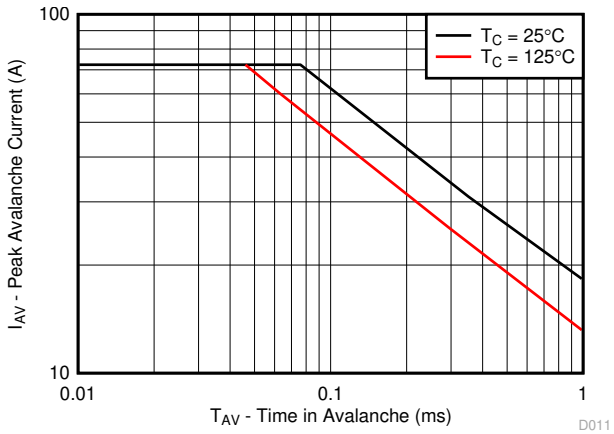


Figure 4-11. Single Pulse Unclamped Inductive Switching

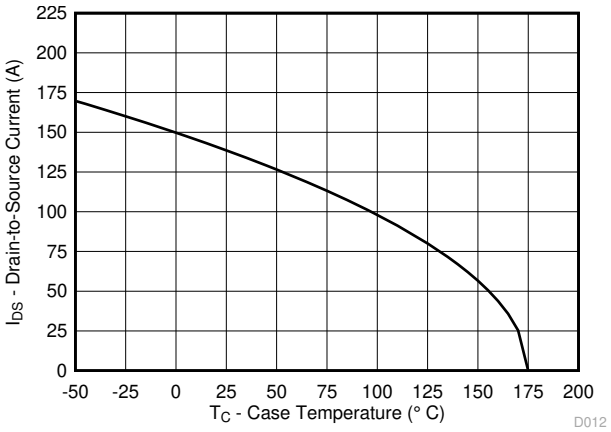


Figure 4-12. Maximum Drain Current vs Temperature

5 Device and Documentation Support

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5.2 Documentation Support

5.2.1 Related Documentation

5.3 Receiving Notification of Documentation Updates

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

6 Revision History

Changes from Revision * (October 2015) to Revision A (June 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD19532KTT	Active	Production	DDPAK/ TO-263 (KTT) | 2	500 | LARGE T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 175	CSD19532KTT
CSD19532KTT.B	Active	Production	DDPAK/ TO-263 (KTT) | 2	500 | LARGE T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 175	CSD19532KTT
CSD19532KTTT	Active	Production	DDPAK/ TO-263 (KTT) | 2	50 | SMALL T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 175	CSD19532KTT
CSD19532KTTT.B	Active	Production	DDPAK/ TO-263 (KTT) | 2	50 | SMALL T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 175	CSD19532KTT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

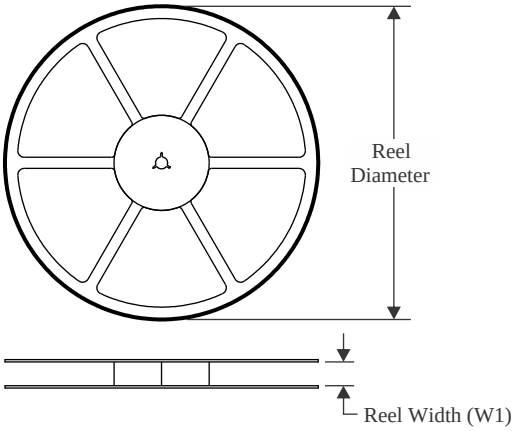
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

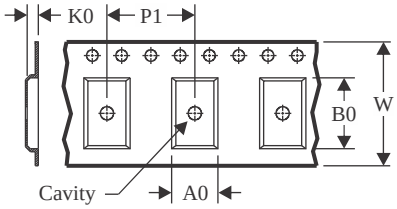
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

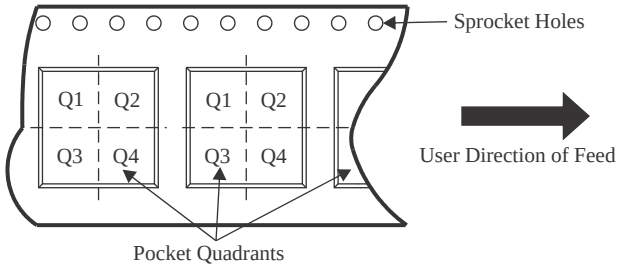


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

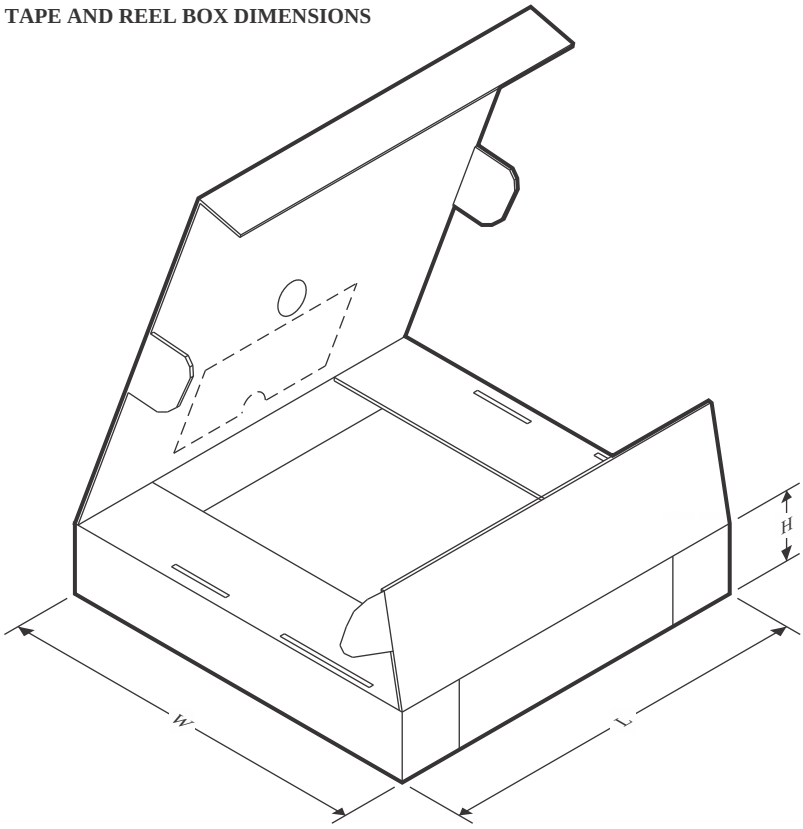
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD19532KTT	DDPAK/ TO-263	KTT	2	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
CSD19532KTTT	DDPAK/ TO-263	KTT	2	50	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2

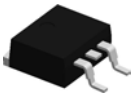
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD19532KTT	DDPAK/TO-263	KTT	2	500	340.0	340.0	38.0
CSD19532KTTT	DDPAK/TO-263	KTT	2	50	340.0	340.0	38.0

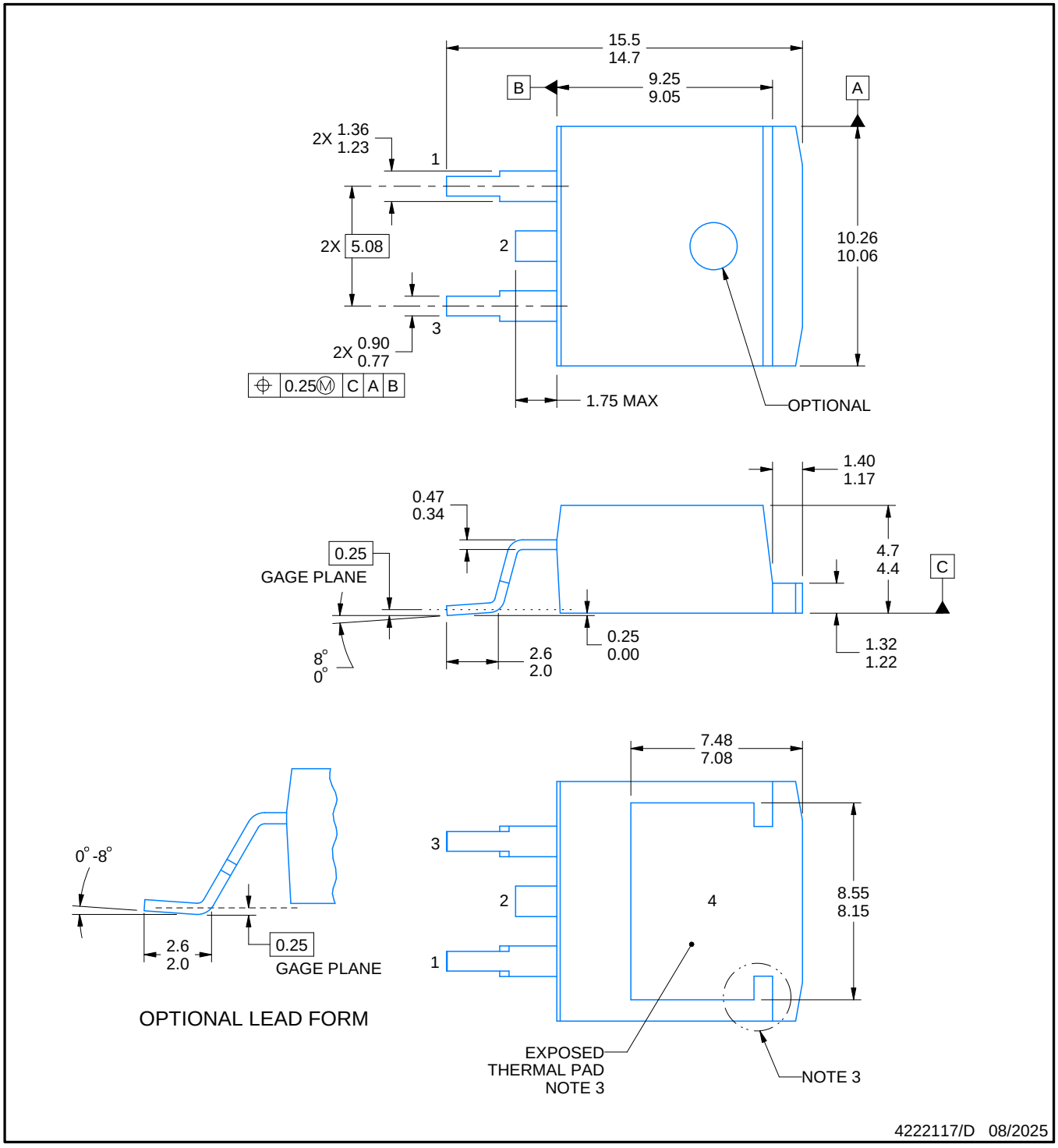
KTT0002A



PACKAGE OUTLINE

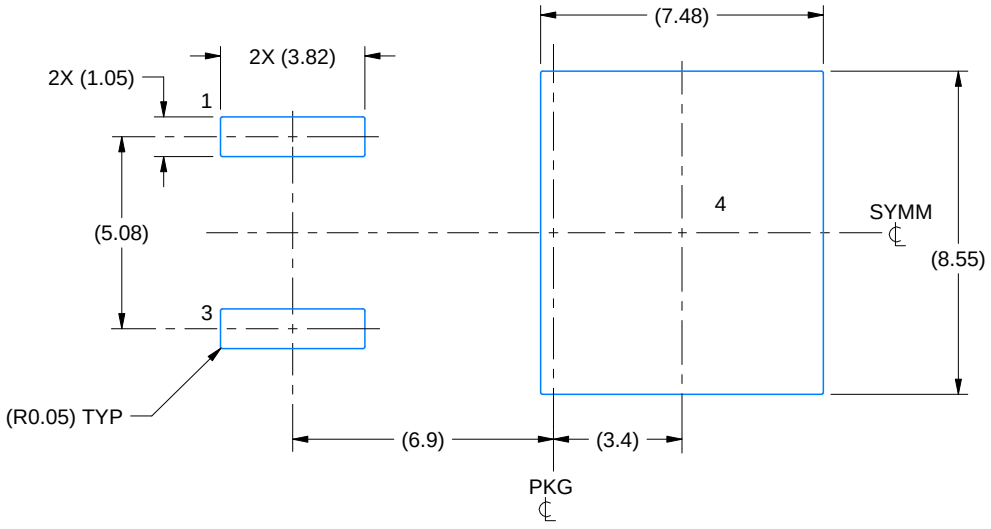
TO-263 - 4.7 mm max height

TRANSISTOR OUTLINE

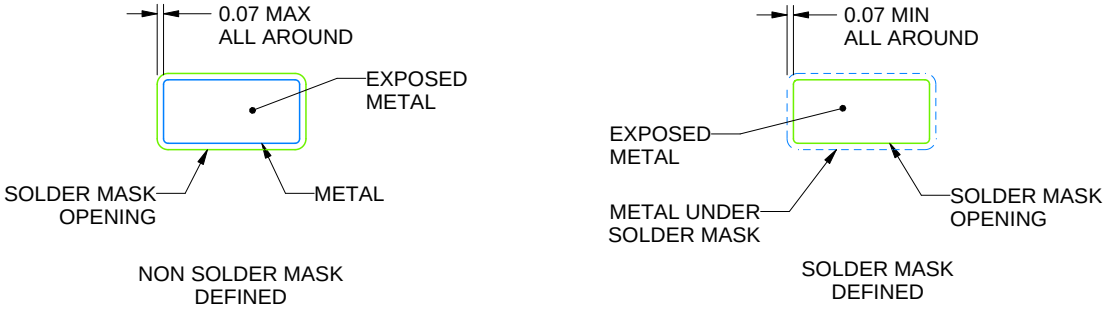


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Features may not exist and shape may vary per different assembly sites. Pin 2 and Pin 4 connected.
4. Reference JEDEC registration TO-263.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:5X



SOLDER MASK DETAILS

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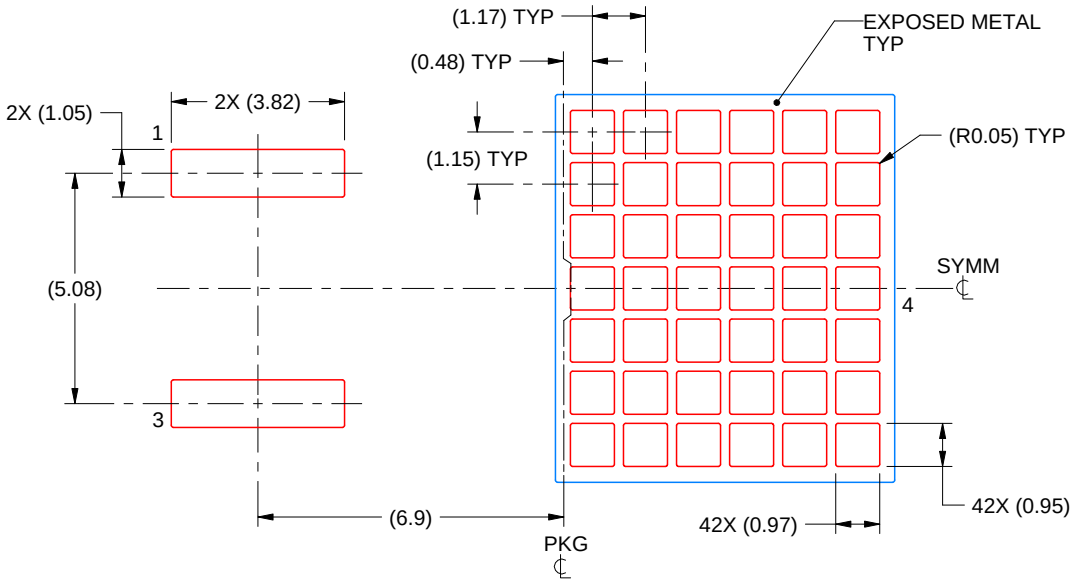
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
60.5% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025