

CSD18542KTT 60V N-Channel NexFET™ Power MOSFET

1 Features

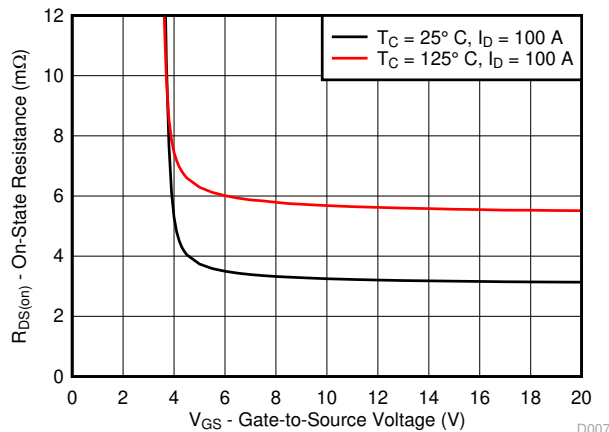
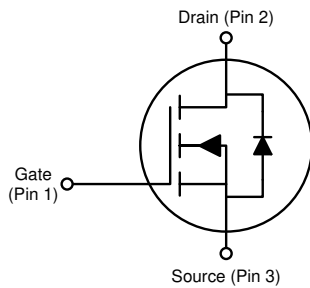
- Ultra-low Q_g and Q_{gd}
- Low-thermal resistance
- Avalanche rated
- Logic level
- Lead-free terminal plating
- RoHS compliant
- Halogen free
- D²PAK plastic package

2 Applications

- DC-DC ,conversion
- Secondary side synchronous rectifier
- Motor control

3 Description

This 60V, 3.3mΩ, D²PAK (TO-263) NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



$R_{DS(on)}$ vs V_{GS}

D007

Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	60	V
Q_g	Gate Charge Total (10V)	44	nC
Q_{gd}	Gate Charge Gate-to-Drain	6.9	nC
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 4.5\text{V}$	4.0
		$V_{GS} = 10\text{V}$	3.3
$V_{GS(th)}$	Threshold Voltage	1.8	V

Device Information⁽¹⁾

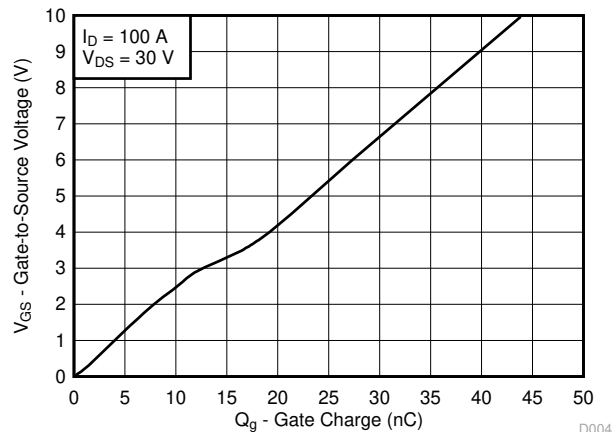
DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD18542KTT	500	13-Inch Reel	D ² PAK Plastic Package	Tape and Reel
CSD18542KTTT	50			

- (1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current (Package Limited)	200	A
	Continuous Drain Current (Silicon Limited), $T_C = 25^\circ\text{C}$	170	
	Continuous Drain Current (Silicon Limited), $T_C = 100^\circ\text{C}$	120	
I_{DM}	Pulsed Drain Current ⁽¹⁾	400	A
P_D	Power Dissipation	250	W
T_J, T_{stg}	Operating Junction, Storage Temperature	-55 to 175	$^\circ\text{C}$
E_{AS}	Avalanche Energy, Single Pulse $I_D = 75\text{A}, L = 0.1\text{mH}, R_G = 25\Omega$	281	mJ

- (1) Max $R_{\theta JC} = 0.6^\circ\text{C/W}$, pulse duration $\leq 100\mu\text{s}$, duty cycle $\leq 1\%$.



Gate Charge

D004



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4 Specifications

4.1 Electrical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
STATIC CHARACTERISTICS							
BV _{DSS}	Drain-to-source voltage	V _{GS} = 0V, I _D = 250μA	60			V	
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0V, V _{DS} = 48V	1			μA	
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0V, V _{GS} = 20V	100			nA	
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _D = 250μA	1.5	1.8	2.2	V	
R _{DS(on)}	Drain-to-source on resistance	V _{GS} = 4.5V, I _D = 100A	4.0			mΩ	
		V _{GS} = 10V, I _D = 100A	3.3				
g _{fs}	Transconductance	V _{DS} = 6V, I _D = 100A	198			S	
DYNAMIC CHARACTERISTICS							
C _{iss}	Input capacitance	V _{GS} = 0V, V _{DS} = 30V, f = 1MHz	3900			5070	pF
C _{oss}	Output capacitance		570			740	pF
C _{rss}	Reverse transfer capacitance		11			14	pF
R _G	Series gate resistance		1.3			2.6	Ω
Q _g	Gate charge total (4.5V)	V _{DS} = 30V, I _D = 100A	21			27	nC
Q _g	Gate charge total (10V)		44			57	nC
Q _{gd}	Gate charge gate-to-drain		6.9				nC
Q _{gs}	Gate charge gate-to-source		10				nC
Q _{g(th)}	Gate charge at V _{th}		7.3				nC
Q _{oss}	Output charge	V _{DS} = 30V, V _{GS} = 0V	63				nC
t _{d(on)}	Turnon delay time	V _{DS} = 30V, V _{GS} = 10V, I _{DS} = 100A, R _G = 0Ω	6				ns
t _r	Rise time		5				ns
t _{d(off)}	Turnoff delay time		18				ns
t _f	Fall time		21				ns
DIODE CHARACTERISTICS							
V _{SD}	Diode forward voltage	I _{SD} = 100A, V _{GS} = 0V	0.9			1.0	V
Q _{rr}	Reverse recovery charge	V _{DS} = 30V, I _F = 100A, di/dt = 300A/μs	148				nC
t _{rr}	Reverse recovery time		53				ns

4.2 Thermal Information

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance			0.6	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance			62	$^\circ\text{C/W}$

4.3 Typical MOSFET Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

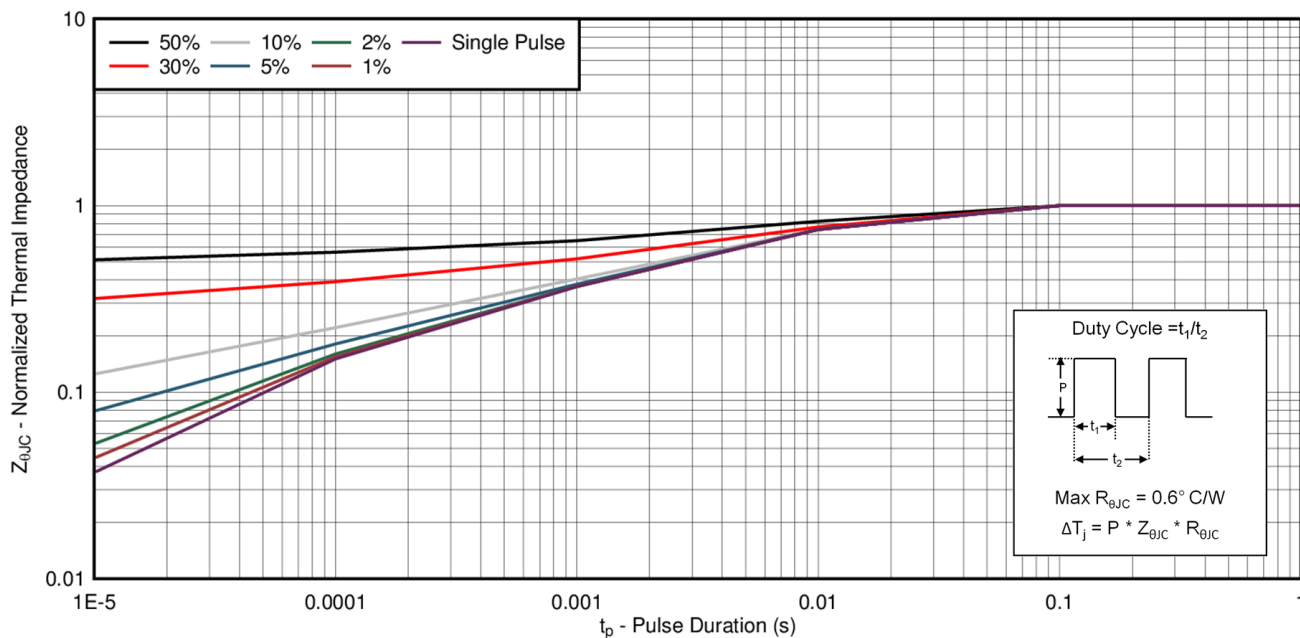


Figure 4-1. Transient Thermal Impedance

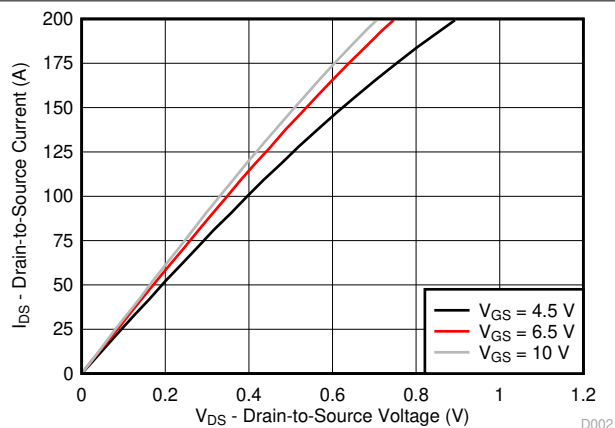


Figure 4-2. Saturation Characteristics

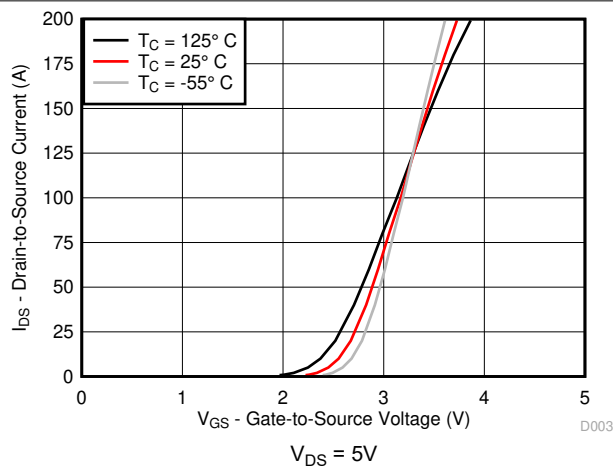


Figure 4-3. Transfer Characteristics

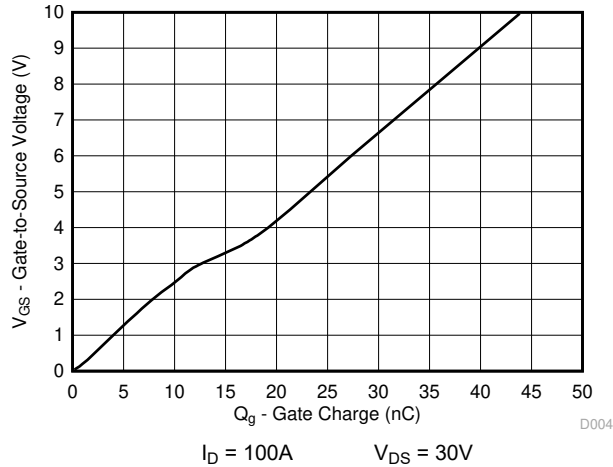


Figure 4-4. Gate Charge

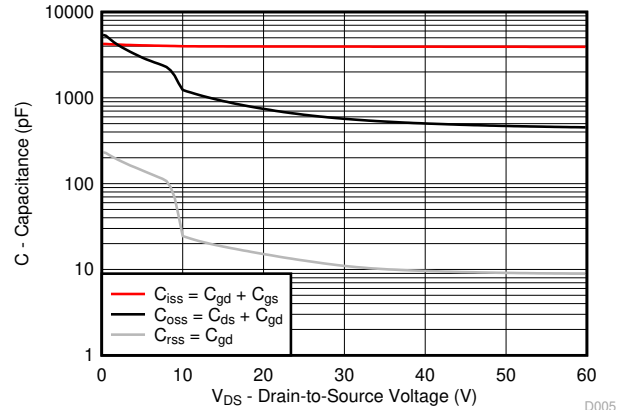


Figure 4-5. Capacitance

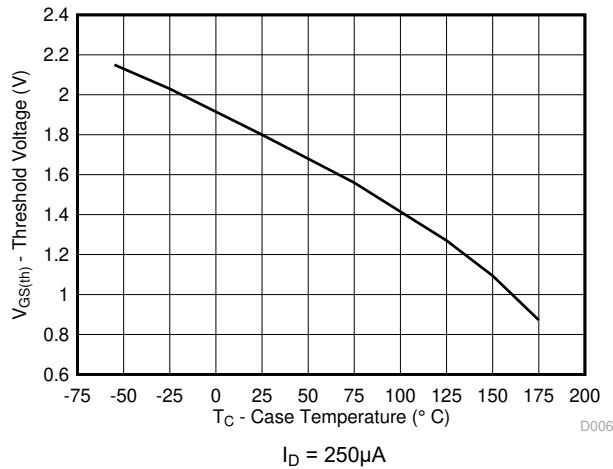


Figure 4-6. Threshold Voltage vs Temperature

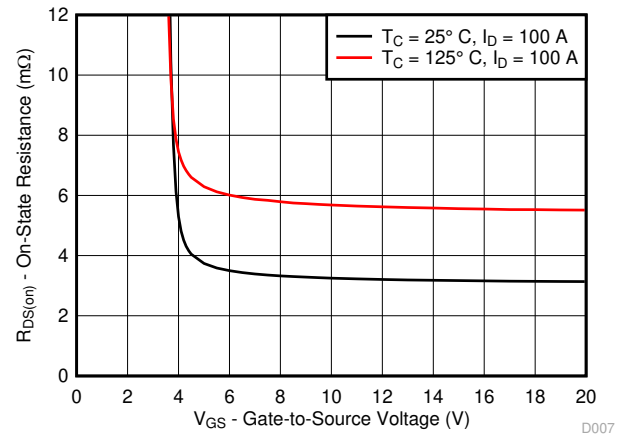


Figure 4-7. On-State Resistance vs Gate-to-Source Voltage

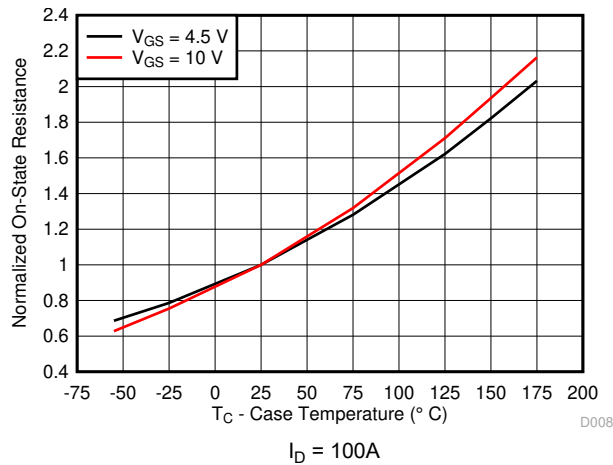


Figure 4-8. Normalized On-State Resistance vs Temperature

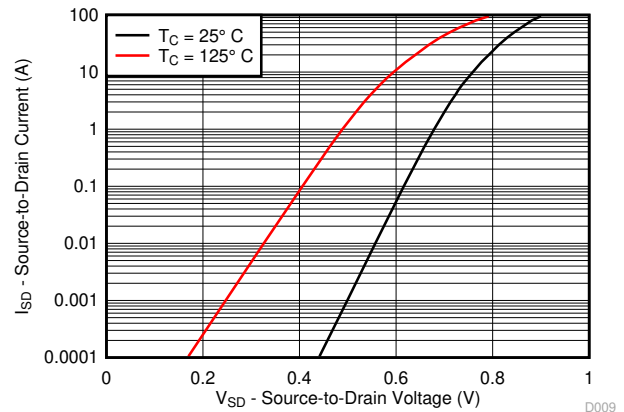


Figure 4-9. Typical Diode Forward Voltage

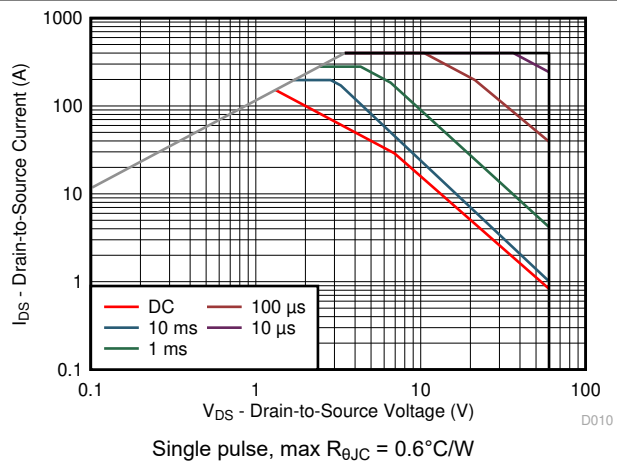


Figure 4-10. Maximum Safe Operating Area

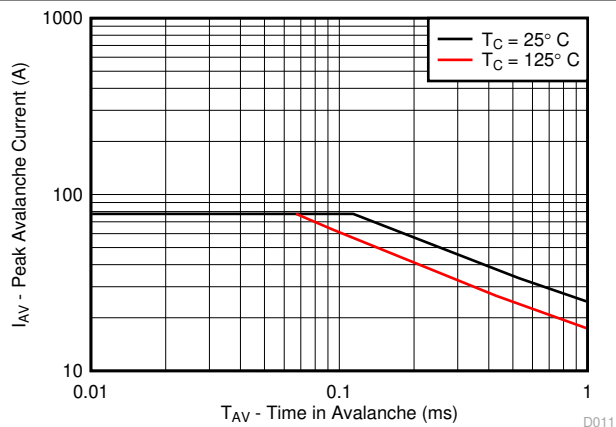


Figure 4-11. Single Pulse Unclamped Inductive Switching

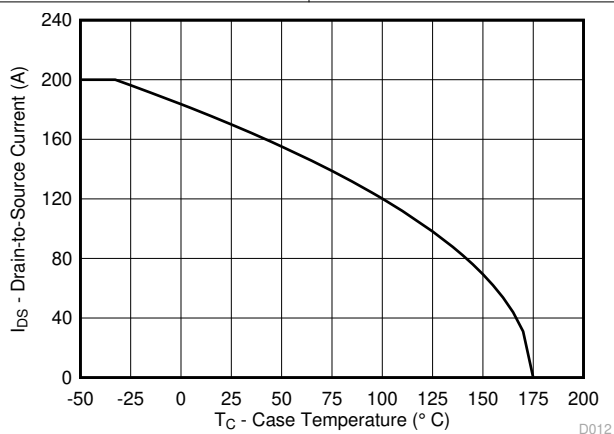


Figure 4-12. Maximum Drain Current vs Temperature

5 Device and Documentation Support

5.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5.3 Trademarks

NexFET™ is a trademark of Texas Instruments.

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5.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

6 Revision History

Changes from Revision A (March 2017) to Revision B (June 2024) Page

- Updated the numbering format for tables, figures, and cross-references throughout the document..... **1**

Changes from Revision * (March 2016) to Revision A (March 2017) Page

- Changed the values for C_{OSS} , Q_{gs} , t_r , $t_{d(off)}$, t_f , Q_{rr} , and t_{rr} in the *Electrical Characteristics* table..... **3**

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD18542KTT	Active	Production	DDPAK/ TO-263 (KTT) 2	500 LARGE T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 175	CSD18542KTT
CSD18542KTT.B	Active	Production	DDPAK/ TO-263 (KTT) 2	500 LARGE T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 175	CSD18542KTT
CSD18542KTTT	Active	Production	DDPAK/ TO-263 (KTT) 2	50 SMALL T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 175	CSD18542KTT
CSD18542KTTT.B	Active	Production	DDPAK/ TO-263 (KTT) 2	50 SMALL T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 175	CSD18542KTT

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

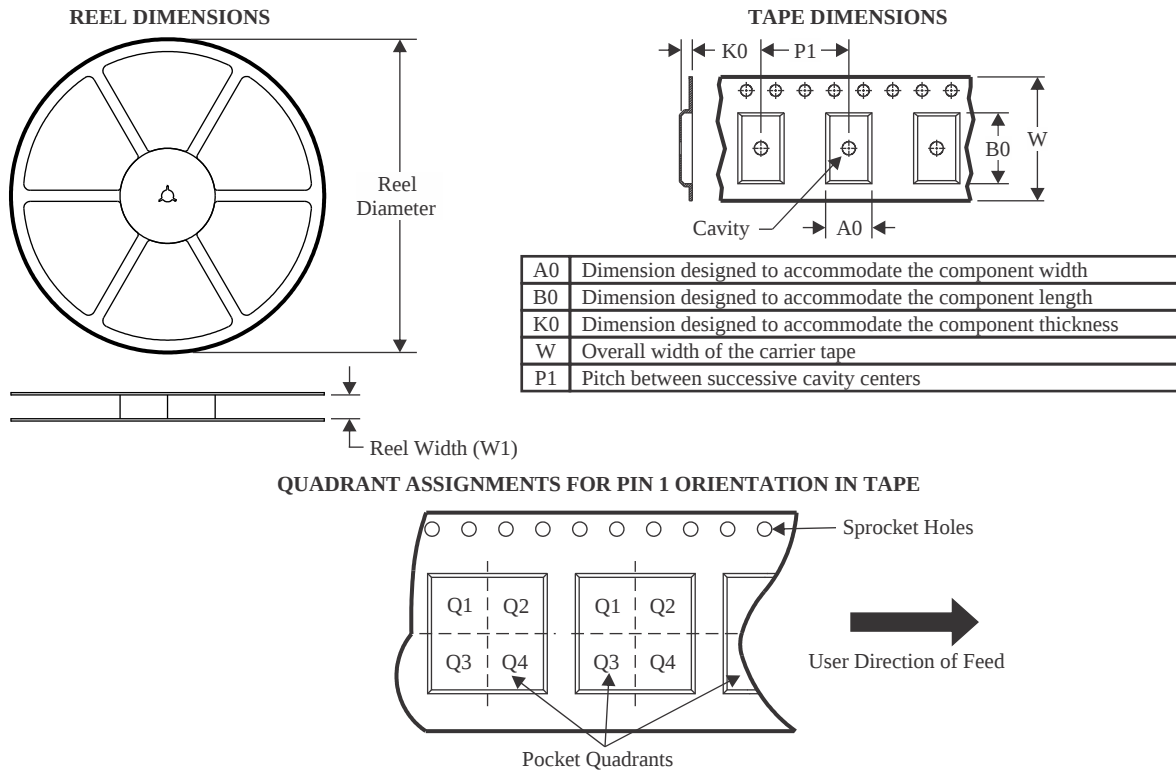
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD18542KTT	DDPAK/ TO-263	KTT	2	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
CSD18542KTTT	DDPAK/ TO-263	KTT	2	50	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2

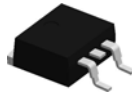
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD18542KTT	DDPAK/TO-263	KTT	2	500	340.0	340.0	38.0
CSD18542KTTT	DDPAK/TO-263	KTT	2	50	340.0	340.0	38.0

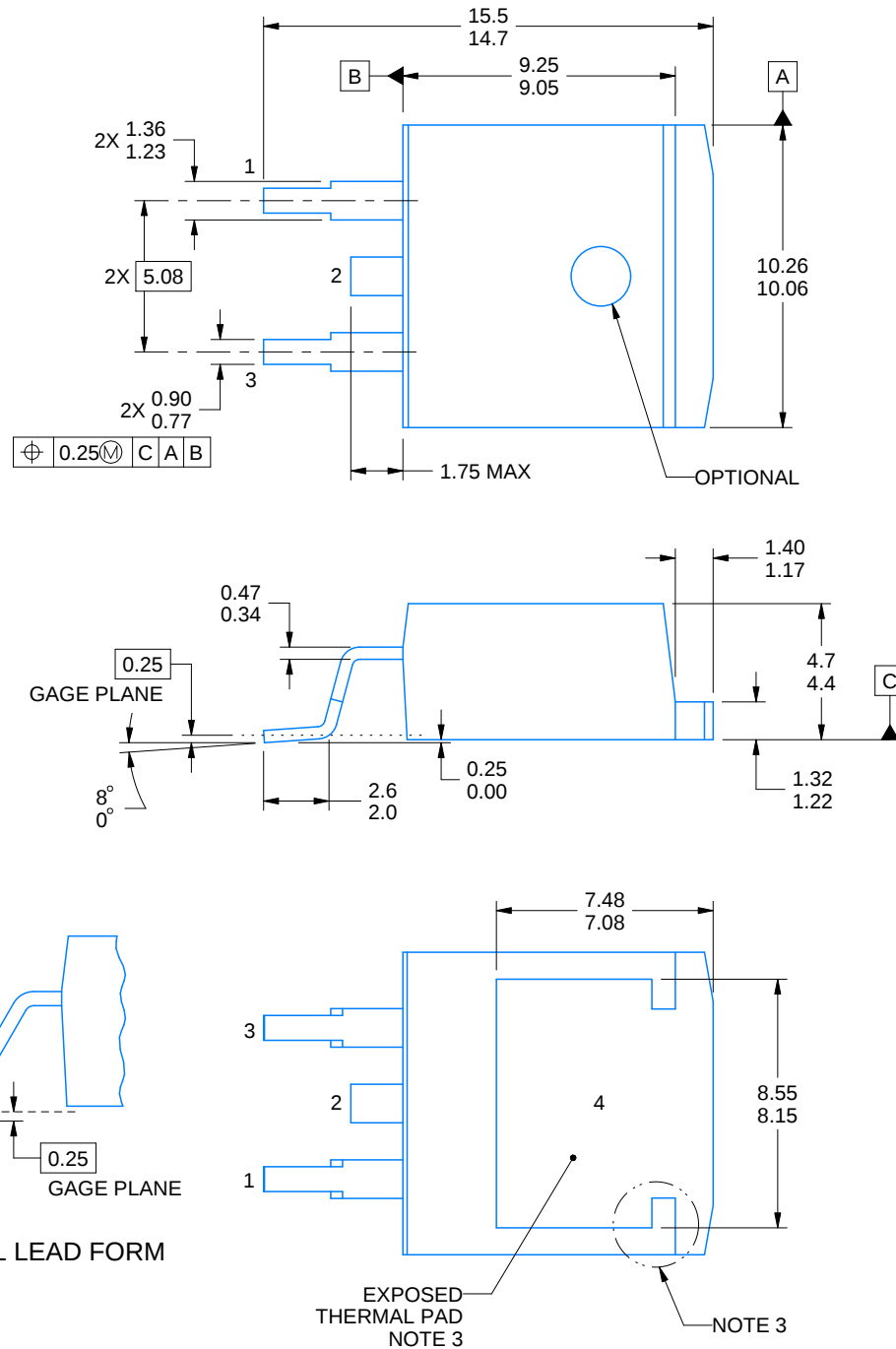
KTT0002A



PACKAGE OUTLINE

TO-263 - 4.7 mm max height

TRANSISTOR OUTLINE



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NOTES:

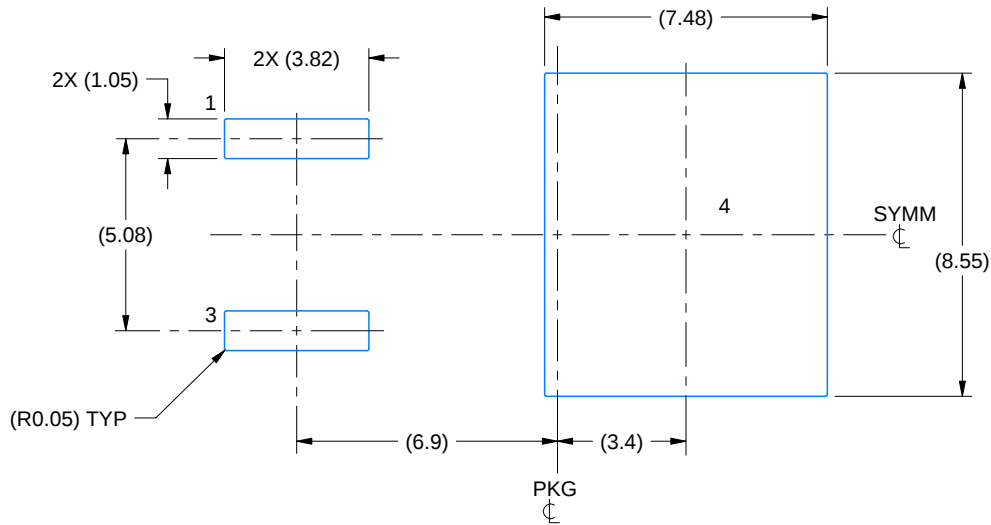
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Features may not exist and shape may vary per different assembly sites. Pin 2 and Pin 4 connected.
4. Reference JEDEC registration TO-263.

EXAMPLE BOARD LAYOUT

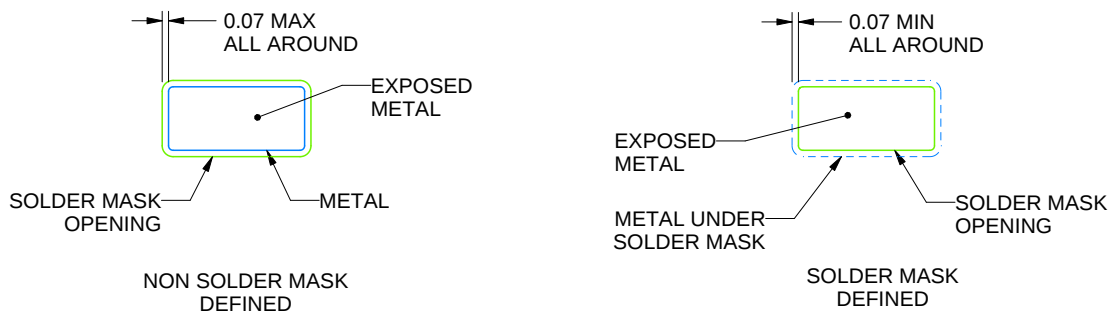
KTT0002A

TO-263 - 4.7 mm max height

TRANSISTOR OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:5X



SOLDER MASK DETAILS

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NOTES: (continued)

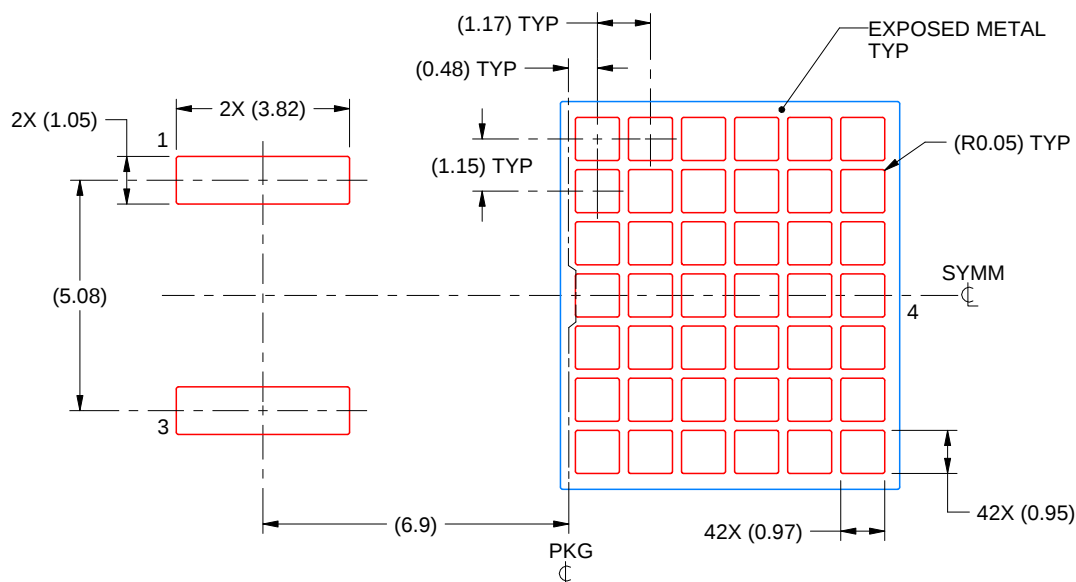
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

KTT0002A

TO-263 - 4.7 mm max height

TRANSISTOR OUTLINE



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 60.5% PRINTED SOLDER COVERAGE BY AREA
 SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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