







CSD18541F5

SLPS571B - MAY 2016 - REVISED FEBRUARY 2022

CSD18541F5 60-V N-Channel FemtoFET™ MOSFET

1 Features

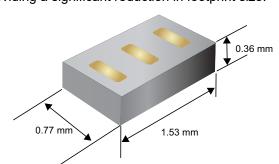
- Low on-resistance
- Ultra-low Q_g and Q_{gd}
- Ultra-small footprint
 - 1.53 mm × 0.77 mm
- Low profile
 - 0.36-mm height
- Integrated ESD protection diode
- Lead and halogen free
- RoHS compliant

2 Applications

- Optimized for industrial load switch applications
- Optimized for general purpose switching applications

3 Description

This 54-mΩ, 60-V, N-Channel FemtoFET™ MOSFET technology is designed and optimized to minimize the footprint in many space constrained industrial load switch applications. This technology is capable of replacing standard small signal MOSFETs while providing a significant reduction in footprint size.



Typical Part Dimensions

Product Summary

T _A = 25°	С	TYPICAL VA	UNIT		
V _{DS}	Drain-to-Source Voltage	60		V	
Qg	Gate Charge Total (10 V)	11		nC	
Q _{gd}	Gate Charge Gate-to-Drain	1.6	nC		
В	Drain-to-Source On-Resistance	V _{GS} = 4.5 V 57		mΩ	
R _{DS(on)}	Dialii-to-Source Off-Resistance	V _{GS} = 10 V 54		11152	
V _{GS(th)}	Threshold Voltage 1.75				

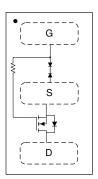
Device Information

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD18541F5	3000		Femto	Таре
CSD18541F5T	7-Inch Ree		1.53-mm × 0.77-mm SMD Lead Less	and Reel

1. For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

T _A = 25	s°C	VALUE	UNIT
V _{DS}	Drain-to-Source Voltage	60	V
V _{GS}	Gate-to-Source Voltage	±20	V
I _D	Continuous Drain Current	2.2	Α
I _{DM}	Pulsed Drain Current (1)(2)	21	Α
P _D	Power Dissipation	500	mW
T _J , T _{stg}	Operating Junction Temperature, Storage Temperature	-55 to 150	°C
E _{AS}	Avalanche Energy, Single Pulse I_D = 12.8 A, L = 0.1 mH, R_G = 25 Ω	8.2	mJ



Top View



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

С	changes from Revision A (December 2016) to Revision B (February 2022)	Page
•	Changed ultra-low profile bullet from 0.35 mm to 0.36 mm in height	1
•	Updated ultra-low profile image height from 0.35 mm to 0.36 mm	1
•	Changed ultra-low profile image height from 0.35 mm to 0.36 mm.	8
	Added FemtoFET Surface Mount Guide note	

С	hanges from Revision * (May 2016) to Revision A (August 2017)	Page
•	Added the Section 6.1 section to Section 6	7
•	Added Table 7-1 to the Section 7.1 section	8
•	Updated the Section 7.2	9
•	Updated the Section 7.3	9

5 Specifications

5.1 Electrical Characteristics

 $T_A = 25^{\circ}C$ (unless otherwise stated)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC	CHARACTERISTICS	,			-	
BV _{DSS}	Drain-to-source voltage	V _{GS} = 0 V, I _{DS} = 250 μA	60			V
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0 V, V _{DS} = 48 V			1	μΑ
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0 V, V _{GS} = 20 V			10	μΑ
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _{DS} = 250 μA	1.4	1.75	2.2	V
D	Drain-to-source on-resistance	V _{GS} = 4.5 V, I _{DS} = 1 A		57	75	mΩ
$R_{DS(on)}$	Drain-to-source on-resistance	V _{GS} = 10 V, I _{DS} = 1 A		54	65	11177
9 _{fs}	Transconductance	V _{DS} = 6 V, I _{DS} = 1 A		7.7		S
DYNAM	IC CHARACTERISTICS					
C _{iss}	Input capacitance			598	777	pF
C _{oss}	Output capacitance	$V_{GS} = 0 \text{ V, } V_{DS} = 30 \text{ V,}$ f = 1 MHz		47	61	pF
C _{rss}	Reverse transfer capacitance	J2		8.1	10.5	pF
R _G	Series gate resistance			1200	1600	Ω
Qg	Gate charge total (10 V)			11	14	nC
Q _{gd}	Gate charge gate-to-drain	V = 20 V L = 4 A		1.6		nC
Q _{gs}	Gate charge gate-to-source	V _{DS} = 30 V, I _{DS} = 1 A		1.5		nC
Q _{g(th)}	Gate charge at V _{th}			0.8		nC
Q _{oss}	Output charge	V _{DS} = 30 V, V _{GS} = 0 V		3.2		nC
t _{d(on)}	Turnon delay time			572		ns
t _r	Rise time	V _{DS} = 30 V, V _{GS} = 4.5 V,		540		ns
t _{d(off)}	Turnoff delay time	$I_{DS} = 1 \text{ A}, R_G = 0 \Omega$		1076		ns
t _f	Fall time			496		ns
DIODE (CHARACTERISTICS	,				
V _{SD}	Diode forward voltage	I _{SD} = 1 A, V _{GS} = 0 V		0.8	1	V

5.2 Thermal Information

T_A = 25°C (unless otherwise stated)

	THERMAL METRIC	MIN	TYP	MAX	UNIT
Ь	Junction-to-ambient thermal resistance ⁽¹⁾		85		°C/W
R _{0JA}	Junction-to-ambient thermal resistance ⁽²⁾		245		C/VV

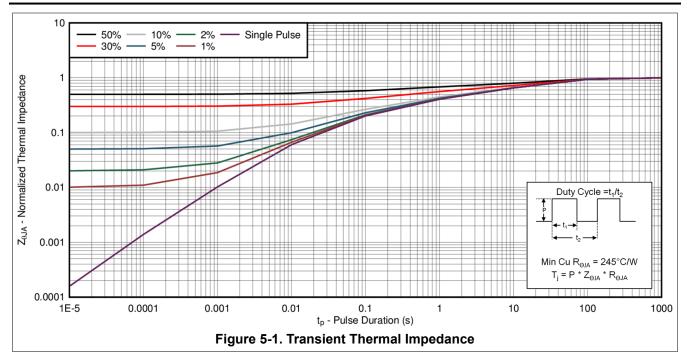
⁽¹⁾ Device mounted on FR4 material with 1-in² (6.45-cm²), 2-oz (0.071-mm) thick Cu.

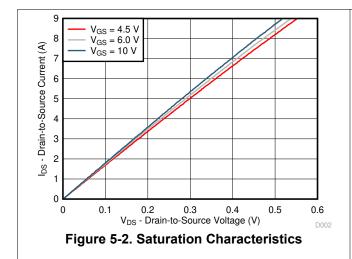
5.3 Typical MOSFET Characteristics

 $T_A = 25$ °C (unless otherwise stated)

⁽²⁾ Device mounted on FR4 material with minimum Cu mounting area.







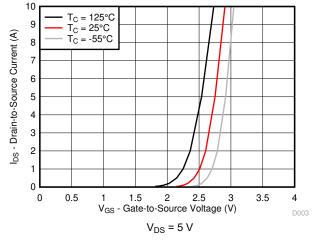
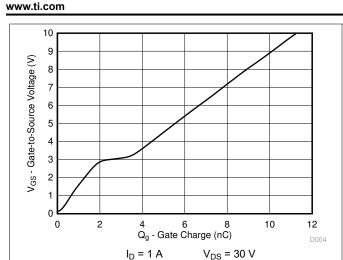


Figure 5-3. Transfer Characteristics



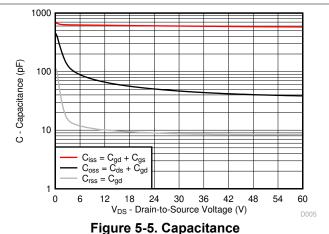
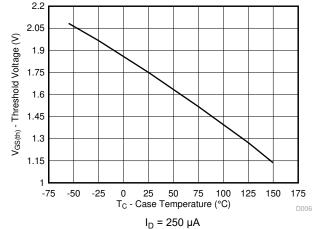


Figure 5-4. Gate Charge

Figure 5-4. Gate Charge



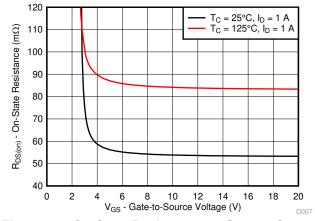
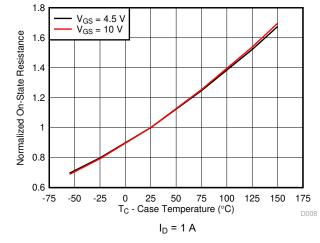


Figure 5-6. Threshold Voltage vs Temperature

Figure 5-7. On-State Resistance vs Gate-to-Source Voltage



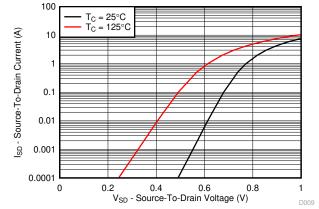
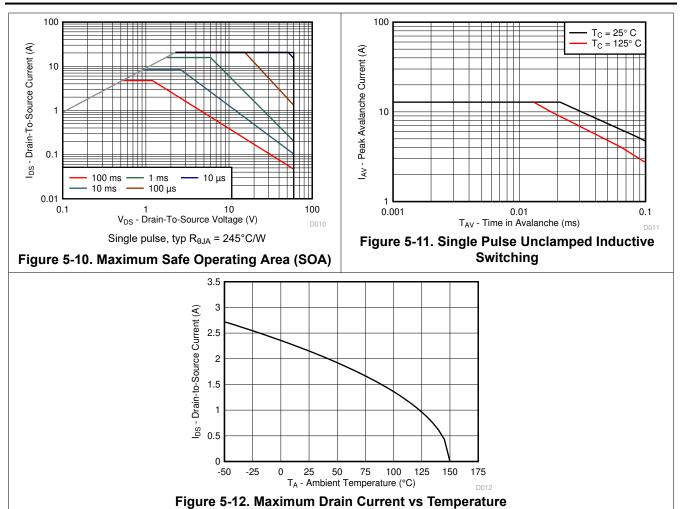


Figure 5-8. Normalized On-State Resistance vs
Temperature

Figure 5-9. Typical Diode Forward Voltage







6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Community Resources

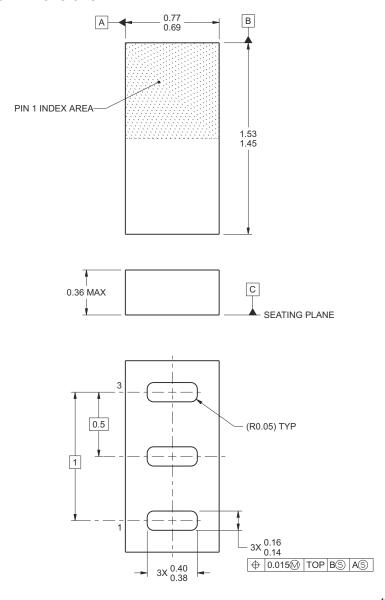
6.3 Trademarks

FemtoFET[™] is a trademark of Texas Instruments.
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7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions



4222132/A 06/2015

- A. All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
- B. This drawing is subject to change without notice.
- C. This package is a PB-free solder land design.

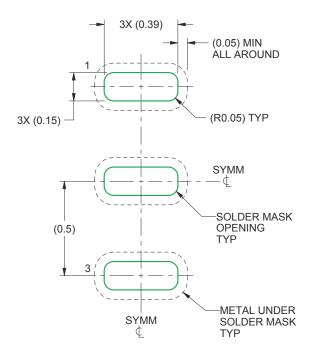
Table 7-1. Pin Configuration

POSITION	DESIGNATION
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

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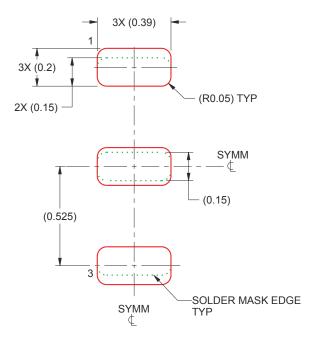


7.2 Recommended Minimum PCB Layout



- A. All dimensions are in millimeters.
- B. For more information, see FemtoFET Surface Mount Guide (SLRA003D).

7.3 Recommended Stencil Pattern



A. All dimensions are in millimeters.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
CSD18541F5	Active	Production	PICOSTAR (YJK) 3	3000 LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	1T
CSD18541F5.B	Active	Production	PICOSTAR (YJK) 3	3000 LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	1T
CSD18541F5T	Active	Production	PICOSTAR (YJK) 3	250 SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	1T
CSD18541F5T.B	Active	Production	PICOSTAR (YJK) 3	250 SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	1T

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD18541F5	PICOSTAF	YJK	3	3000	180.0	8.4	0.92	1.68	0.42	4.0	8.0	Q1
CSD18541F5T	PICOSTAF	YJK	3	250	180.0	8.4	0.92	1.68	0.42	4.0	8.0	Q1

PACKAGE MATERIALS INFORMATION

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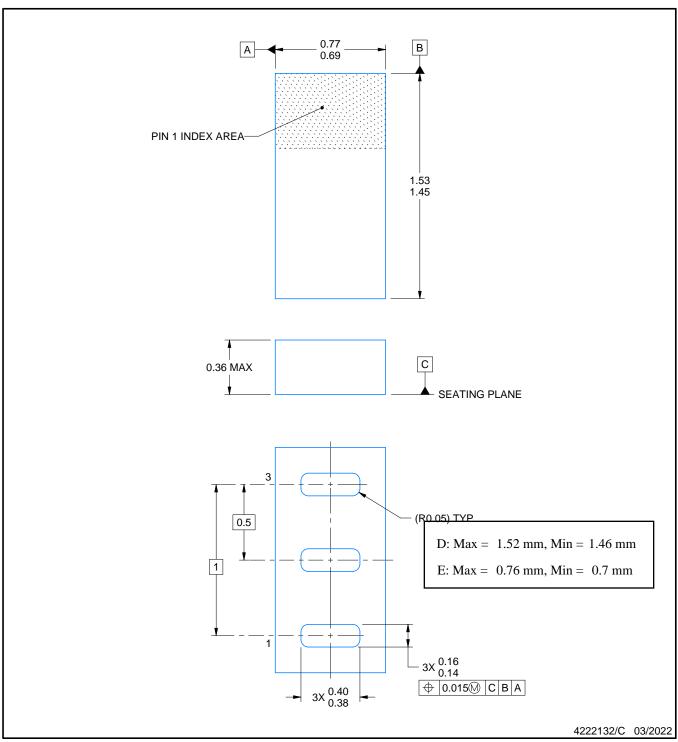


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD18541F5	PICOSTAR	YJK	3	3000	182.0	182.0	20.0
CSD18541F5T	PICOSTAR	YJK	3	250	182.0	182.0	20.0



PicoStar™



NOTES:

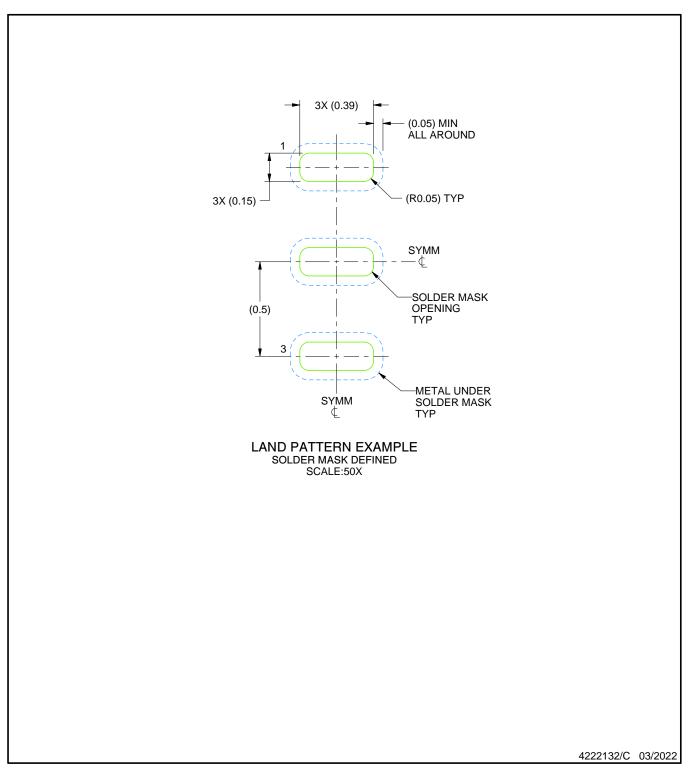
PicoStar is a trademark of Texas Instruments.

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M

 2. This drawing is subject to change without notice.
- 3. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device datasheet or contact a local TI representative.



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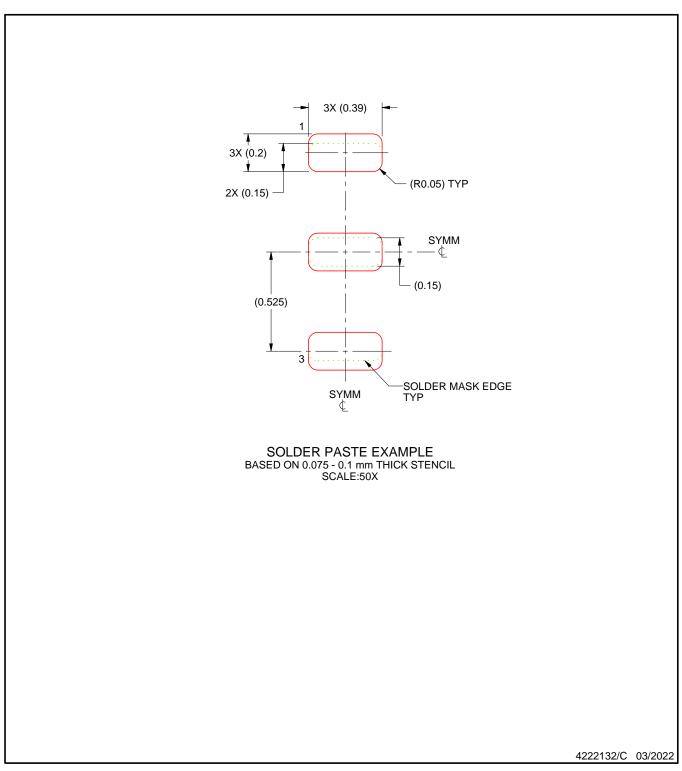


NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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