

# CSD18541F5 60-V N-Channel FemtoFET™ MOSFET

## 1 Features

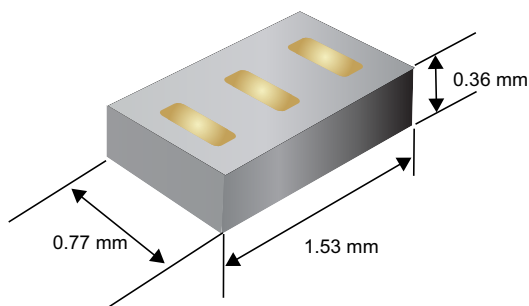
- Low on-resistance
- Ultra-low  $Q_g$  and  $Q_{gd}$
- Ultra-small footprint
  - 1.53 mm × 0.77 mm
- Low profile
  - 0.36-mm height
- Integrated ESD protection diode
- Lead and halogen free
- RoHS compliant

## 2 Applications

- Optimized for industrial load switch applications
- Optimized for general purpose switching applications

## 3 Description

This 54-mΩ, 60-V, N-Channel FemtoFET™ MOSFET technology is designed and optimized to minimize the footprint in many space constrained industrial load switch applications. This technology is capable of replacing standard small signal MOSFETs while providing a significant reduction in footprint size.



**Typical Part Dimensions**

## Product Summary

| $T_A = 25^\circ\text{C}$ |                               | TYPICAL VALUE           | UNIT |
|--------------------------|-------------------------------|-------------------------|------|
| $V_{DS}$                 | Drain-to-Source Voltage       | 60                      | V    |
| $Q_g$                    | Gate Charge Total (10 V)      | 11                      | nC   |
| $Q_{gd}$                 | Gate Charge Gate-to-Drain     | 1.6                     | nC   |
| $R_{DS(on)}$             | Drain-to-Source On-Resistance | $V_{GS} = 4.5\text{ V}$ | 57   |
|                          |                               | $V_{GS} = 10\text{ V}$  | 54   |
| $V_{GS(th)}$             | Threshold Voltage             | 1.75                    | V    |

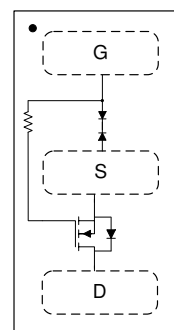
## Device Information

| DEVICE      | QTY  | MEDIA       | PACKAGE                                     | SHIP                |
|-------------|------|-------------|---------------------------------------------|---------------------|
| CSD18541F5  | 3000 | 7-Inch Reel | Femto<br>1.53-mm × 0.77-mm<br>SMD Lead Less | Tape<br>and<br>Reel |
| CSD18541F5T | 250  |             |                                             |                     |

1. For all available packages, see the orderable addendum at the end of the data sheet.

## Absolute Maximum Ratings

| $T_A = 25^\circ\text{C}$ |                                                                                              | VALUE      | UNIT |
|--------------------------|----------------------------------------------------------------------------------------------|------------|------|
| $V_{DS}$                 | Drain-to-Source Voltage                                                                      | 60         | V    |
| $V_{GS}$                 | Gate-to-Source Voltage                                                                       | ±20        | V    |
| $I_D$                    | Continuous Drain Current                                                                     | 2.2        | A    |
| $I_{DM}$                 | Pulsed Drain Current (1)(2)                                                                  | 21         | A    |
| $P_D$                    | Power Dissipation                                                                            | 500        | mW   |
| $T_J, T_{stg}$           | Operating Junction Temperature, Storage Temperature                                          | –55 to 150 | °C   |
| $E_{AS}$                 | Avalanche Energy, Single Pulse<br>$I_D = 12.8\text{ A}, L = 0.1\text{ mH}, R_G = 25\ \Omega$ | 8.2        | mJ   |



**Top View**



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision A (December 2016) to Revision B (February 2022)</b> | <b>Page</b> |
|------------------------------------------------------------------------------|-------------|
| • Changed ultra-low profile bullet from 0.35 mm to 0.36 mm in height.....    | 1           |
| • Updated ultra-low profile image height from 0.35 mm to 0.36 mm.....        | 1           |
| • Changed ultra-low profile image height from 0.35 mm to 0.36 mm.....        | 8           |
| • Added FemtoFET Surface Mount Guide note.....                               | 9           |

| <b>Changes from Revision * (May 2016) to Revision A (August 2017)</b>              | <b>Page</b> |
|------------------------------------------------------------------------------------|-------------|
| • Added the <a href="#">Section 6.1</a> section to <a href="#">Section 6</a> ..... | 7           |
| • Added <a href="#">Table 7-1</a> to the <a href="#">Section 7.1</a> section.....  | 8           |
| • Updated the <a href="#">Section 7.2</a> .....                                    | 9           |
| • Updated the <a href="#">Section 7.3</a> .....                                    | 9           |

## 5 Specifications

### 5.1 Electrical Characteristics

$T_A = 25^\circ\text{C}$  (unless otherwise stated)

| PARAMETER               |                                  | TEST CONDITIONS                                                                                 | MIN  | TYP  | MAX | UNIT |    |
|-------------------------|----------------------------------|-------------------------------------------------------------------------------------------------|------|------|-----|------|----|
| STATIC CHARACTERISTICS  |                                  |                                                                                                 |      |      |     |      |    |
| BV <sub>DSS</sub>       | Drain-to-source voltage          | V <sub>GS</sub> = 0 V, I <sub>DS</sub> = 250 μA                                                 | 60   |      |     | V    |    |
| I <sub>DSS</sub>        | Drain-to-source leakage current  | V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 48 V                                                   | 1    |      |     | μA   |    |
| I <sub>GSS</sub>        | Gate-to-source leakage current   | V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V                                                   | 10   |      |     | μA   |    |
| V <sub>GS(th)</sub>     | Gate-to-source threshold voltage | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>DS</sub> = 250 μA                                    | 1.4  | 1.75 | 2.2 | V    |    |
| R <sub>DS(on)</sub>     | Drain-to-source on-resistance    | V <sub>GS</sub> = 4.5 V, I <sub>DS</sub> = 1 A                                                  | 57   |      |     | mΩ   |    |
|                         |                                  | V <sub>GS</sub> = 10 V, I <sub>DS</sub> = 1 A                                                   | 54   |      |     |      |    |
| g <sub>fs</sub>         | Transconductance                 | V <sub>DS</sub> = 6 V, I <sub>DS</sub> = 1 A                                                    | 7.7  |      |     | S    |    |
| DYNAMIC CHARACTERISTICS |                                  |                                                                                                 |      |      |     |      |    |
| C <sub>iss</sub>        | Input capacitance                | V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 30 V,<br>f = 1 MHz                                     | 598  |      |     | 777  | pF |
| C <sub>oss</sub>        | Output capacitance               |                                                                                                 | 47   |      |     | 61   | pF |
| C <sub>rss</sub>        | Reverse transfer capacitance     |                                                                                                 | 8.1  |      |     | 10.5 | pF |
| R <sub>G</sub>          | Series gate resistance           |                                                                                                 | 1200 |      |     | 1600 | Ω  |
| Q <sub>g</sub>          | Gate charge total (10 V)         | V <sub>DS</sub> = 30 V, I <sub>DS</sub> = 1 A                                                   | 11   |      |     | 14   | nC |
| Q <sub>gd</sub>         | Gate charge gate-to-drain        |                                                                                                 | 1.6  |      |     |      | nC |
| Q <sub>gs</sub>         | Gate charge gate-to-source       |                                                                                                 | 1.5  |      |     |      | nC |
| Q <sub>g(th)</sub>      | Gate charge at V <sub>th</sub>   |                                                                                                 | 0.8  |      |     |      | nC |
| Q <sub>oss</sub>        | Output charge                    | V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V                                                   | 3.2  |      |     |      | nC |
| t <sub>d(on)</sub>      | Turnon delay time                | V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 4.5 V,<br>I <sub>DS</sub> = 1 A, R <sub>G</sub> = 0 Ω | 572  |      |     |      | ns |
| t <sub>r</sub>          | Rise time                        |                                                                                                 | 540  |      |     |      | ns |
| t <sub>d(off)</sub>     | Turnoff delay time               |                                                                                                 | 1076 |      |     |      | ns |
| t <sub>f</sub>          | Fall time                        |                                                                                                 | 496  |      |     |      | ns |
| DIODE CHARACTERISTICS   |                                  |                                                                                                 |      |      |     |      |    |
| V <sub>SD</sub>         | Diode forward voltage            | I <sub>SD</sub> = 1 A, V <sub>GS</sub> = 0 V                                                    | 0.8  |      |     | 1    | V  |

### 5.2 Thermal Information

$T_A = 25^\circ\text{C}$  (unless otherwise stated)

| THERMAL METRIC  |                                                       | MIN | TYP | MAX | UNIT               |
|-----------------|-------------------------------------------------------|-----|-----|-----|--------------------|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance <sup>(1)</sup> |     | 85  |     | $^\circ\text{C/W}$ |
|                 | Junction-to-ambient thermal resistance <sup>(2)</sup> |     | 245 |     |                    |

(1) Device mounted on FR4 material with 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm) thick Cu.

(2) Device mounted on FR4 material with minimum Cu mounting area.

### 5.3 Typical MOSFET Characteristics

$T_A = 25^\circ\text{C}$  (unless otherwise stated)

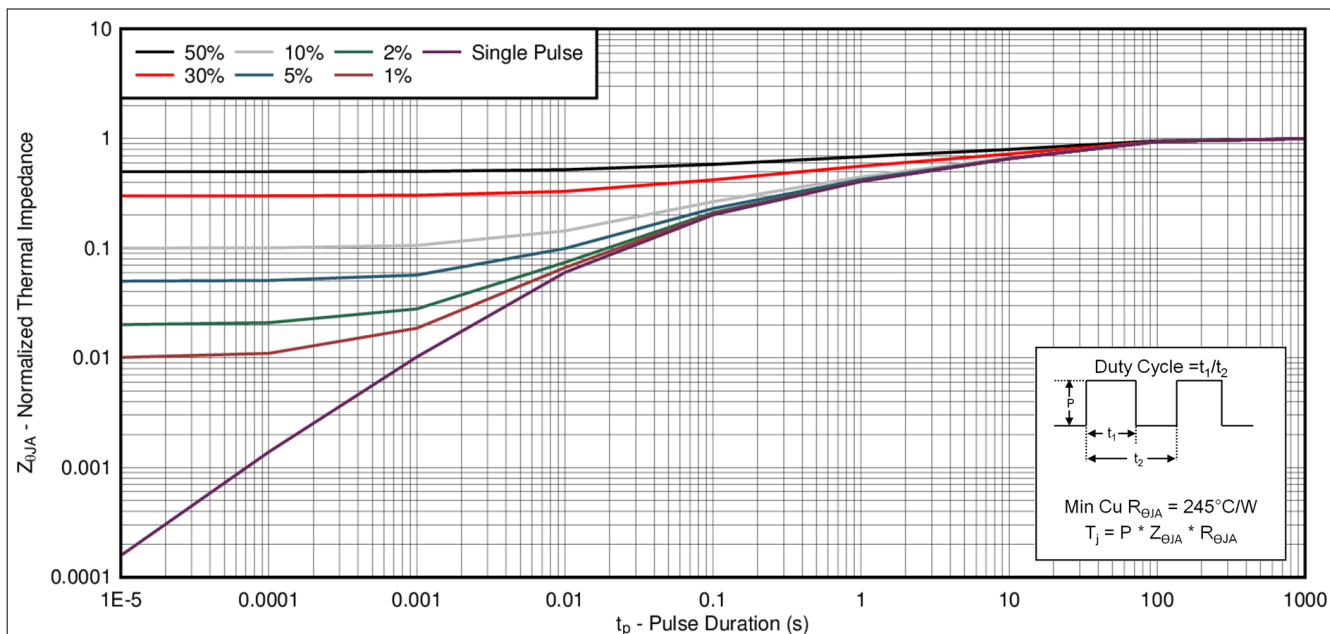


Figure 5-1. Transient Thermal Impedance

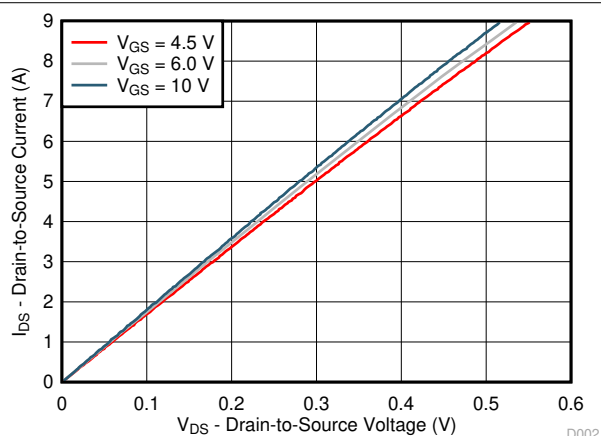


Figure 5-2. Saturation Characteristics

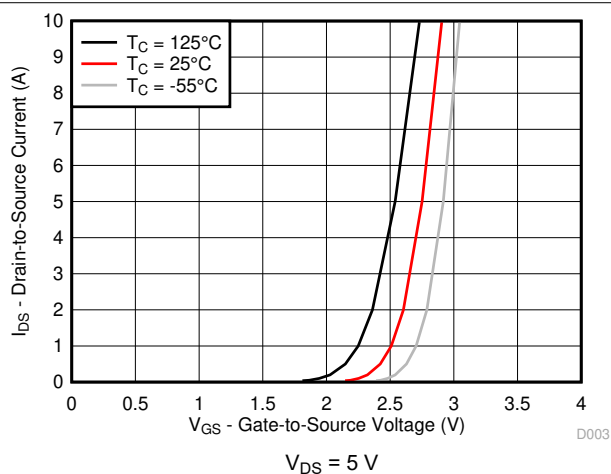
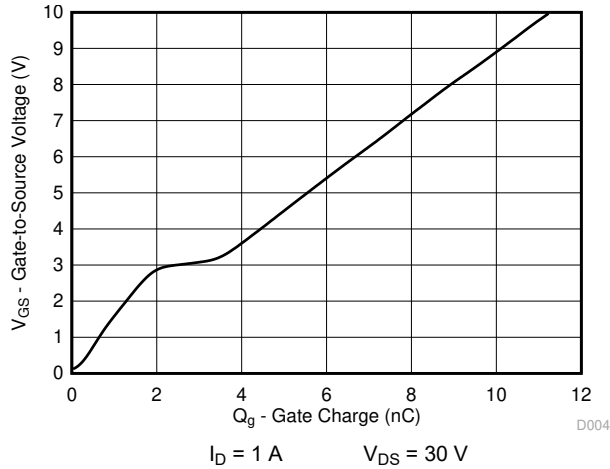
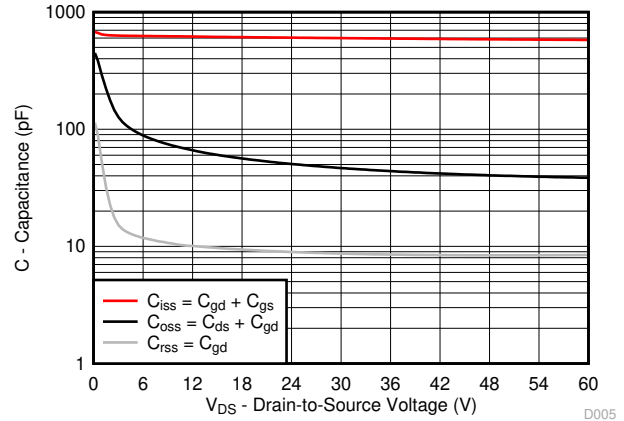


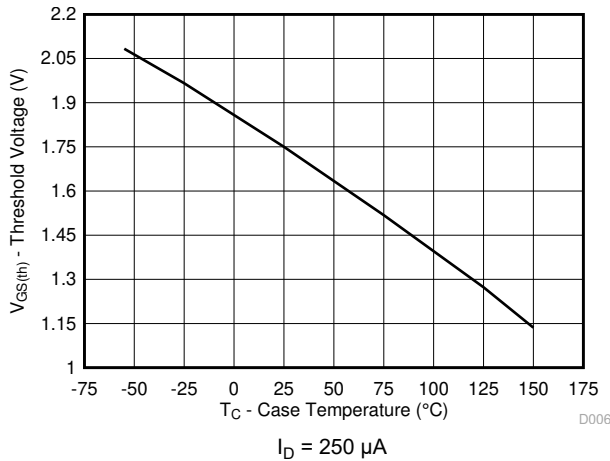
Figure 5-3. Transfer Characteristics



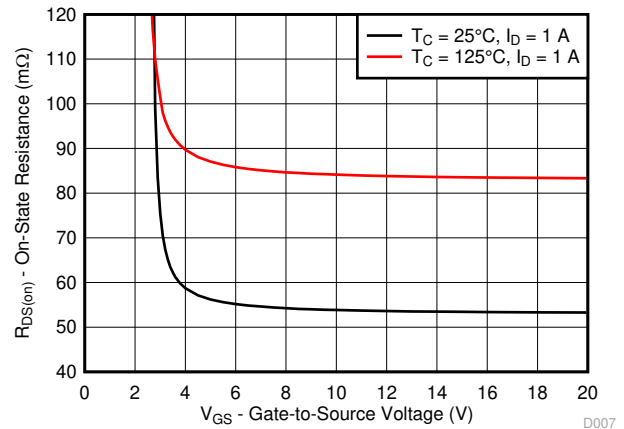
**Figure 5-4. Gate Charge**



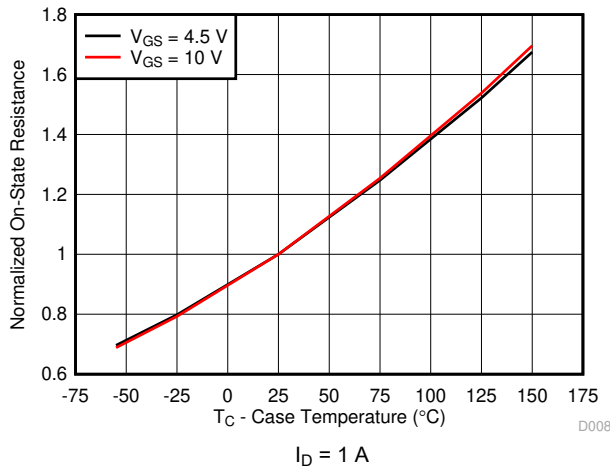
**Figure 5-5. Capacitance**



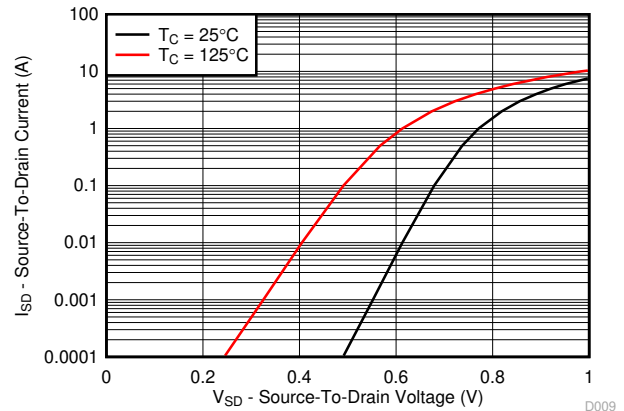
**Figure 5-6. Threshold Voltage vs Temperature**



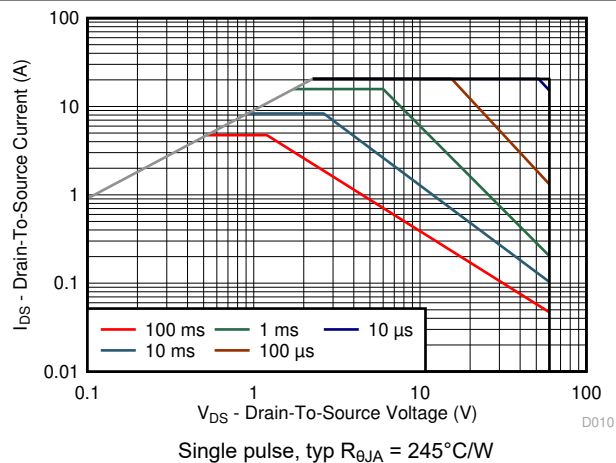
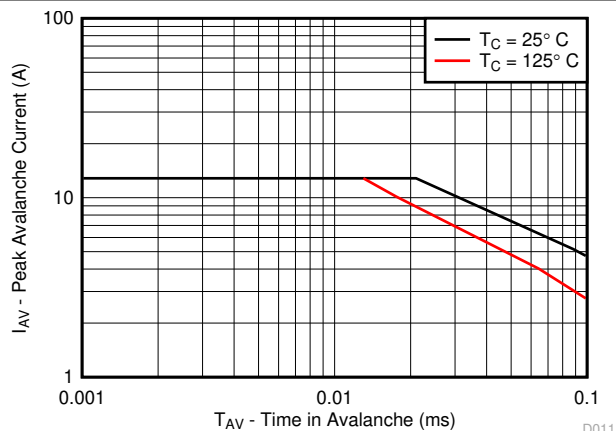
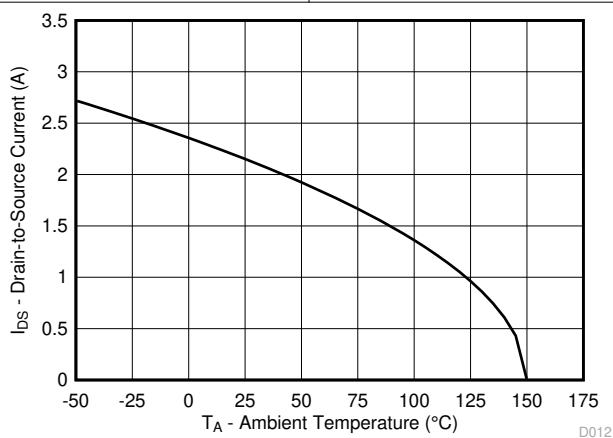
**Figure 5-7. On-State Resistance vs Gate-to-Source Voltage**



**Figure 5-8. Normalized On-State Resistance vs Temperature**



**Figure 5-9. Typical Diode Forward Voltage**

**Figure 5-10. Maximum Safe Operating Area (SOA)****Figure 5-11. Single Pulse Unclamped Inductive Switching****Figure 5-12. Maximum Drain Current vs Temperature**

## **6 Device and Documentation Support**

### **6.1 Receiving Notification of Documentation Updates**

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### **6.2 Community Resources**

### **6.3 Trademarks**

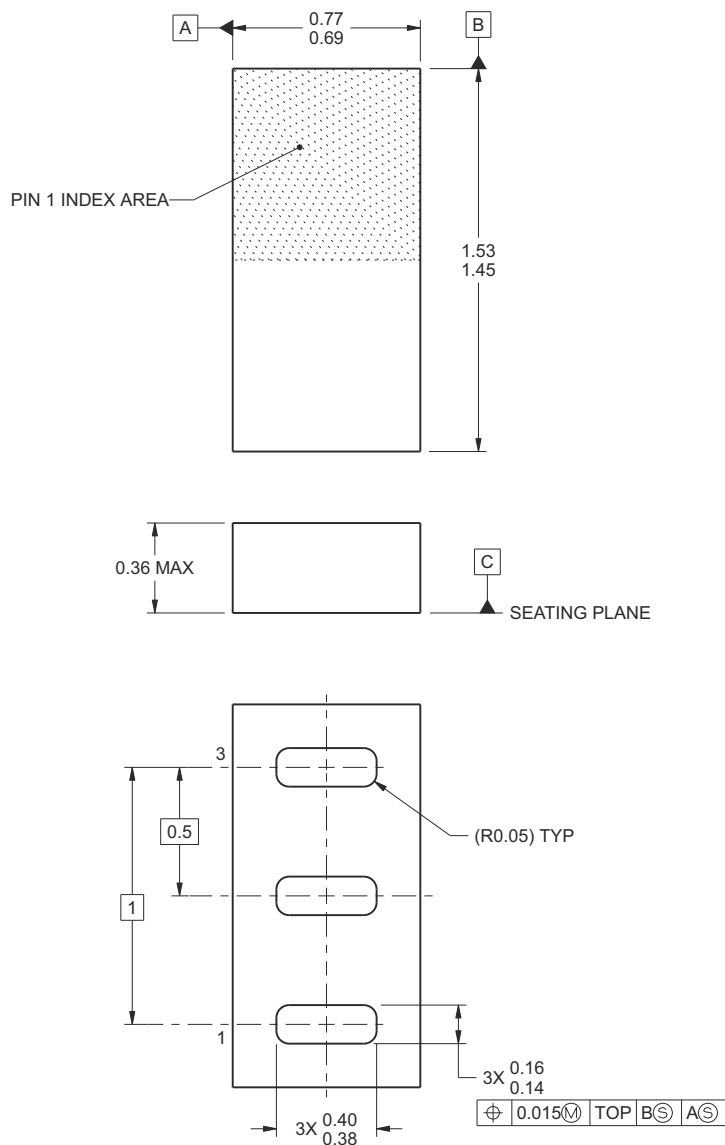
FemtoFET™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 7.1 Mechanical Dimensions



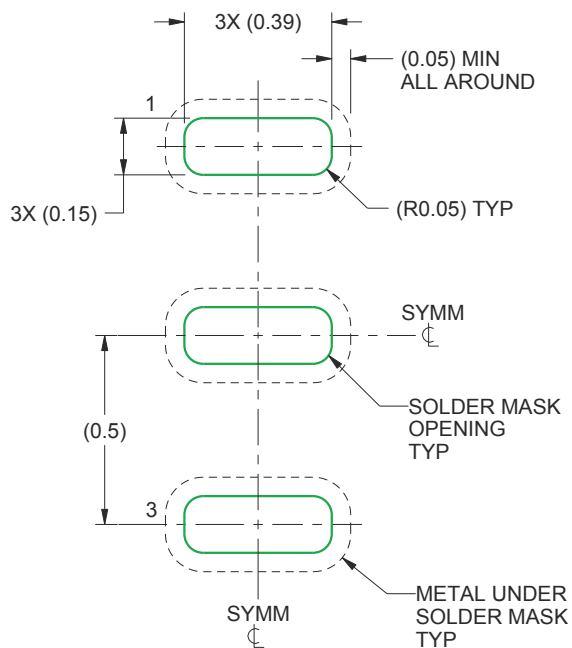
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- A. All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
- B. This drawing is subject to change without notice.
- C. This package is a PB-free solder land design.

**Table 7-1. Pin Configuration**

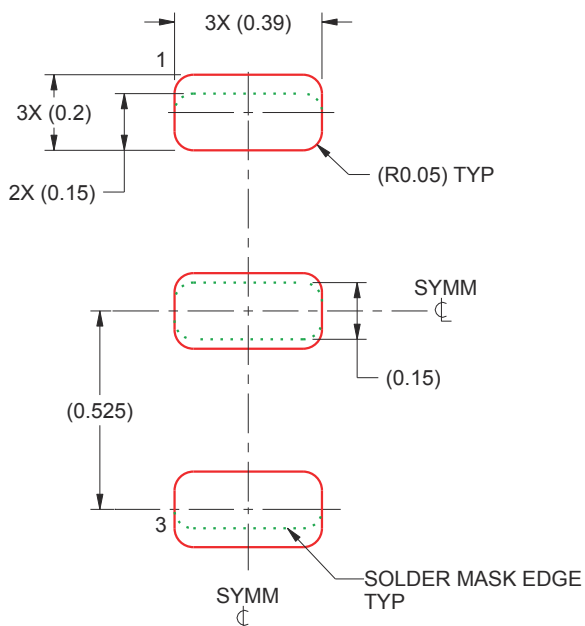
| POSITION | DESIGNATION |
|----------|-------------|
| Pin 1    | Gate        |
| Pin 2    | Source      |
| Pin 3    | Drain       |

## 7.2 Recommended Minimum PCB Layout



- A. All dimensions are in millimeters.
- B. For more information, see [FemtoFET Surface Mount Guide](#) (SLRA003D).

## 7.3 Recommended Stencil Pattern



- A. All dimensions are in millimeters.

## PACKAGING INFORMATION

| Orderable part number       | Status<br>(1) | Material type<br>(2) | Package   Pins     | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------------|---------------|----------------------|--------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">CSD18541F5</a>  | Active        | Production           | PICOSTAR (YJK)   3 | 3000   LARGE T&R      | Yes         | NIAU                                 | Level-1-260C-UNLIM                | -55 to 150   | 1T                  |
| CSD18541F5.B                | Active        | Production           | PICOSTAR (YJK)   3 | 3000   LARGE T&R      | Yes         | NIAU                                 | Level-1-260C-UNLIM                | -55 to 150   | 1T                  |
| <a href="#">CSD18541F5T</a> | Active        | Production           | PICOSTAR (YJK)   3 | 250   SMALL T&R       | Yes         | NIAU                                 | Level-1-260C-UNLIM                | -55 to 150   | 1T                  |
| CSD18541F5T.B               | Active        | Production           | PICOSTAR (YJK)   3 | 250   SMALL T&R       | Yes         | NIAU                                 | Level-1-260C-UNLIM                | -55 to 150   | 1T                  |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

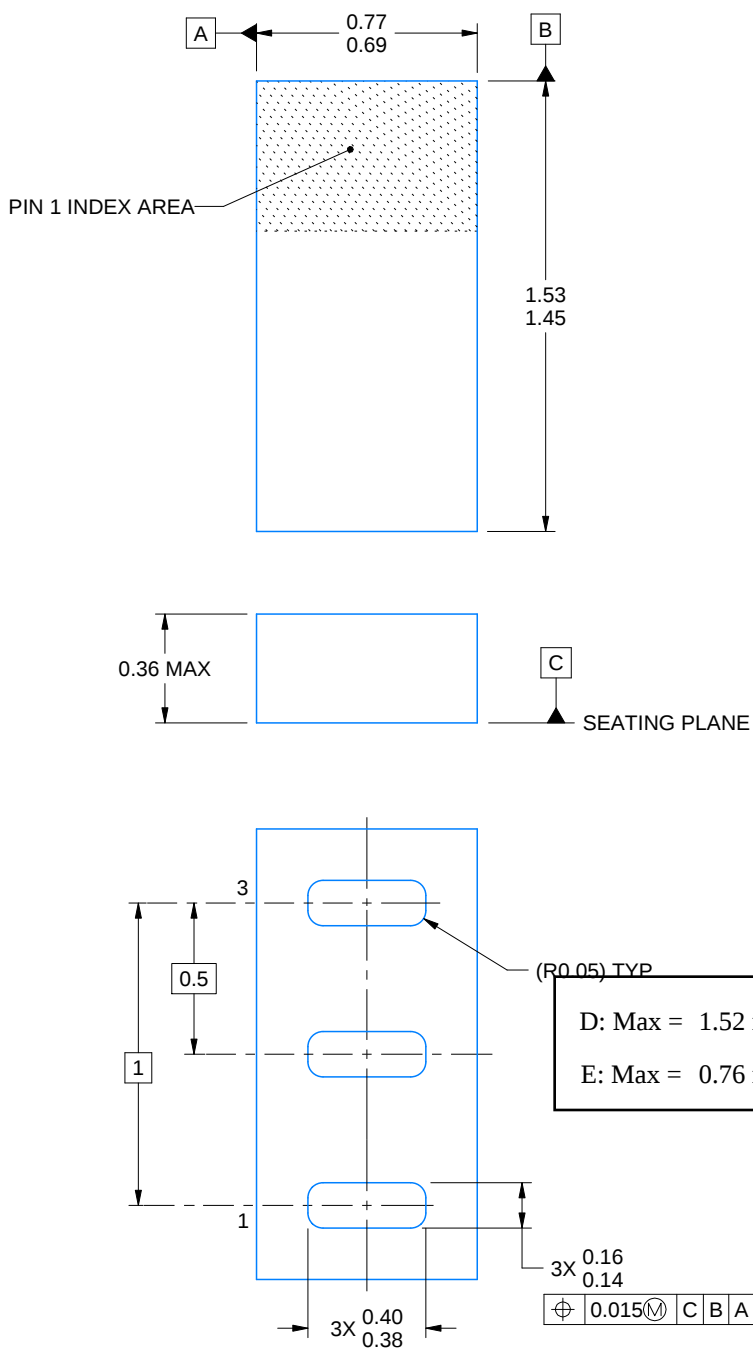
| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CSD18541F5  | PICOSTAR     | YJK             | 3    | 3000 | 180.0              | 8.4                | 0.92    | 1.68    | 0.42    | 4.0     | 8.0    | Q1            |
| CSD18541F5T | PICOSTAR     | YJK             | 3    | 250  | 180.0              | 8.4                | 0.92    | 1.68    | 0.42    | 4.0     | 8.0    | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CSD18541F5  | PICOSTAR     | YJK             | 3    | 3000 | 182.0       | 182.0      | 20.0        |
| CSD18541F5T | PICOSTAR     | YJK             | 3    | 250  | 182.0       | 182.0      | 20.0        |

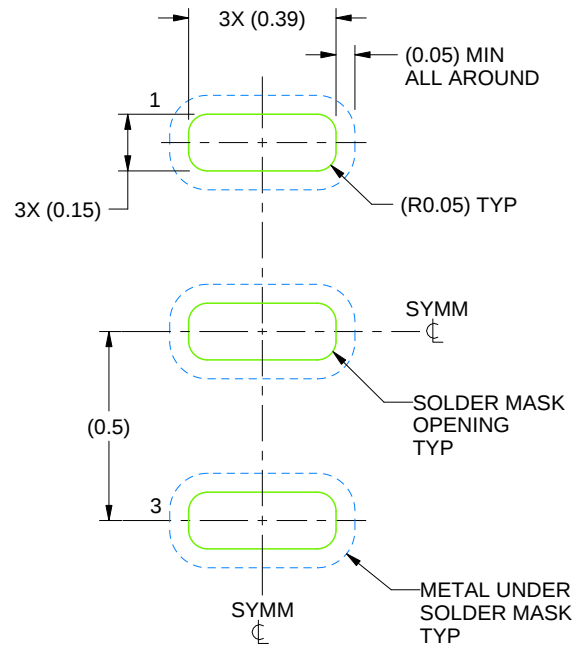


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## NOTES:

PicoStar is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.
3. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device datasheet or contact a local TI representative.

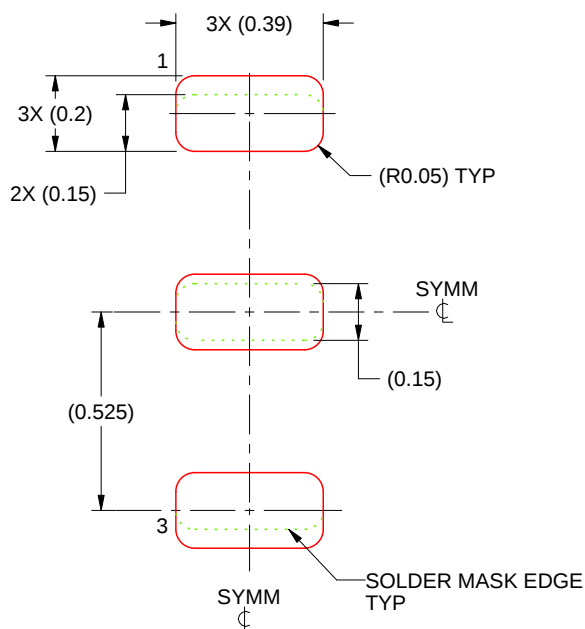


LAND PATTERN EXAMPLE  
SOLDER MASK DEFINED  
SCALE:50X

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NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).



SOLDER PASTE EXAMPLE  
BASED ON 0.075 - 0.1 mm THICK STENCIL  
SCALE:50X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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