

CSD17552Q3A 30 V N-Channel NexFET™ Power MOSFETs

1 Features

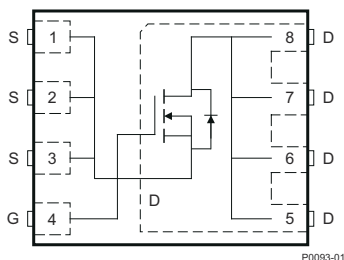
- Ultra-Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb Free
- RoHS Compliant
- Halogen Free
- SON 3.3 mm × 3.3 mm Plastic Package

2 Applications

- Point-of-Load Synchronous Buck in Networking, Telecom, and Computing Systems
- Optimized for Control FET Applications

3 Description

This 30 V, 5.5 mΩ, 3.3 mm × 3.3 mm SON NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



Top View

Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	30		V
Q_g	Gate Charge Total (4.5 V)	9.0		nC
Q_{gd}	Gate Charge Gate-to-Drain	2.3		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 4.5\text{ V}$	6.5	mΩ
		$V_{GS} = 10\text{ V}$	5.5	mΩ
$V_{GS(th)}$	Threshold Voltage	1.5		V

Ordering Information⁽¹⁾

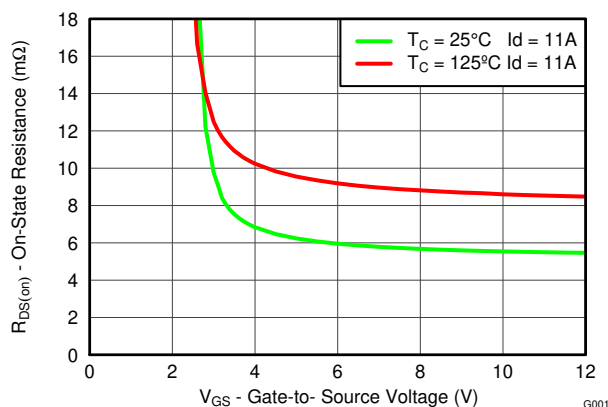
DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD17552Q3A	2500	13-Inch Reel	SON 3.3 mm × 3.3 mm Plastic Package	Tape and Reel
CSD17552Q3AT	250	7-Inch Reel		

- (1) For all available packages, see the orderable addendum at the end of the data sheet.

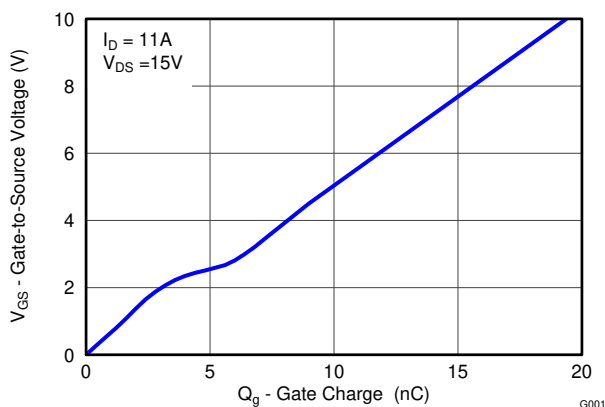
Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current, $T_C = 25^\circ\text{C}$	60	A
	Continuous Drain Current, Silicon Limited	74	A
	Continuous Drain Current, $T_A = 25^\circ\text{C}$ ⁽¹⁾	15	A
I_{DM}	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ ⁽²⁾	84	A
P_D	Power Dissipation ⁽¹⁾	2.6	W
T_J , T_{stg}	Operating Junction Temperature, Storage Temperature	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse $I_D = 30\text{ A}$, $L = 0.1\text{ mH}$, $R_G = 25\ \Omega$	45	mJ

- (1) Typical $R_{\theta JA} = 48^\circ\text{C/W}$ on a 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu pad on a 0.06 inch (1.52 mm) thick FR4 PCB.
- (2) Pulse duration ≤300 μs, duty cycle ≤2%



$R_{DS(on)}$ vs V_{GS}



Gate Charge



Table of Contents

1 Features	1	5 Device and Documentation Support	7
2 Applications	1	5.1 Support Resources.....	7
3 Description	1	5.2 Trademarks.....	7
4 Specifications	3	5.3 Electrostatic Discharge Caution.....	7
4.1 Electrical Characteristics.....	3	5.4 Glossary.....	7
4.2 Thermal Information.....	3	6 Revision History	7
4.3 Typical MOSFET Characteristics.....	4	7 Mechanical, Packaging, and Orderable Information	7

4 Specifications

4.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-source voltage	V _{GS} = 0 V, I _D = 250 μA	30			V
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0 V, V _{DS} = 24 V			1	μA
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0 V, V _{GS} = 20 V			100	nA
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	1.1	1.5	1.9	V
R _{DS(on)}	Drain-to-source on resistance	V _{GS} = 4.5 V, I _D = 11 A		6.5	8.1	mΩ
		V _{GS} = 10 V, I _D = 11 A		5.5	6.0	mΩ
g _{fs}	Transconductance	V _{DS} = 15 V, I _D = 11 A		106		S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input capacitance	V _{GS} = 0 V, V _{DS} = 15 V, f = 1 MHz		1580	2050	pF
C _{oss}	Output capacitance			385	500	pF
C _{rss}	Reverse transfer capacitance			28	36	pF
R _G	Series gate resistance			.9	1.8	Ω
Q _g	Gate charge total (4.5 V)	V _{DS} = 15 V, I _D = 11 A		9	12	nC
Q _{gd}	Gate charge gate to drain			2.3		nC
Q _{gs}	Gate charge gate to source			3.6		nC
Q _{g(th)}	Gate charge at V _{th}			1.8		nC
Q _{oss}	Output charge	V _{DS} = 15 V, V _{GS} = 0 V		11		nC
t _{d(on)}	Turn on delay time	V _{DS} = 15 V, V _{GS} = 4.5 V, I _{DS} = 11 A, R _G = 2 Ω		7.2		ns
t _r	Rise time			7.4		ns
t _{d(off)}	Turn off delay time			11.0		ns
t _f	Fall time			3.4		ns
DIODE CHARACTERISTICS						
V _{SD}	Diode forward voltage	I _{SD} = 11 A, V _{GS} = 0 V		0.8	1	V
Q _{rr}	Reverse recovery charge	V _{DS} = 13.5 V, I _F = 11 A,		17		nC
t _{rr}	Reverse recovery time	di/dt = 300 A/μs		15		ns

4.2 Thermal Information

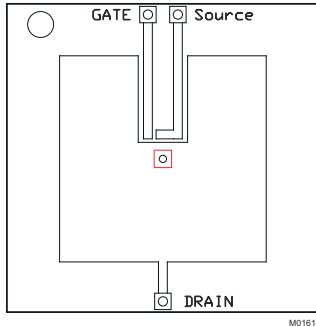
(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
R _{θJC}	Junction-to-case thermal resistance ⁽¹⁾			2.3	°C/W
R _{θJA}	Junction-to-ambient thermal resistance ^{(1) (2)}			60	°C/W

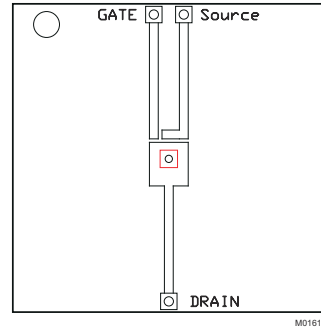
- (1) R_{θJC} is determined with the device mounted on a 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inches × 1.5 inches (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 PCB. R_{θJC} is specified by design, whereas R_{θJA} is determined by the user's board design.
- (2) Device mounted on FR4 material with 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu.

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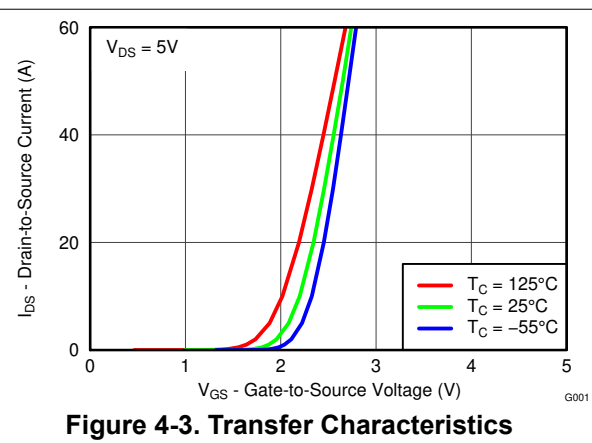
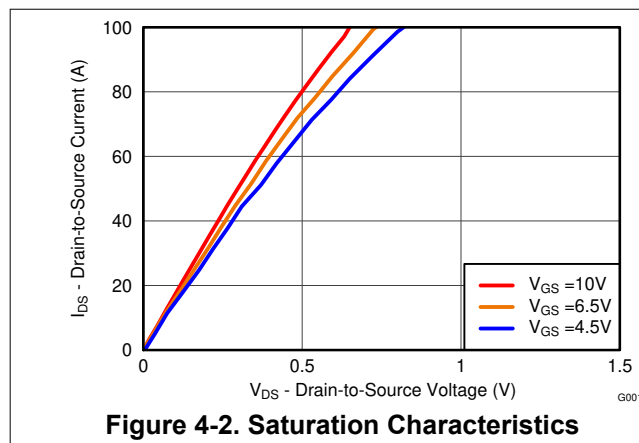
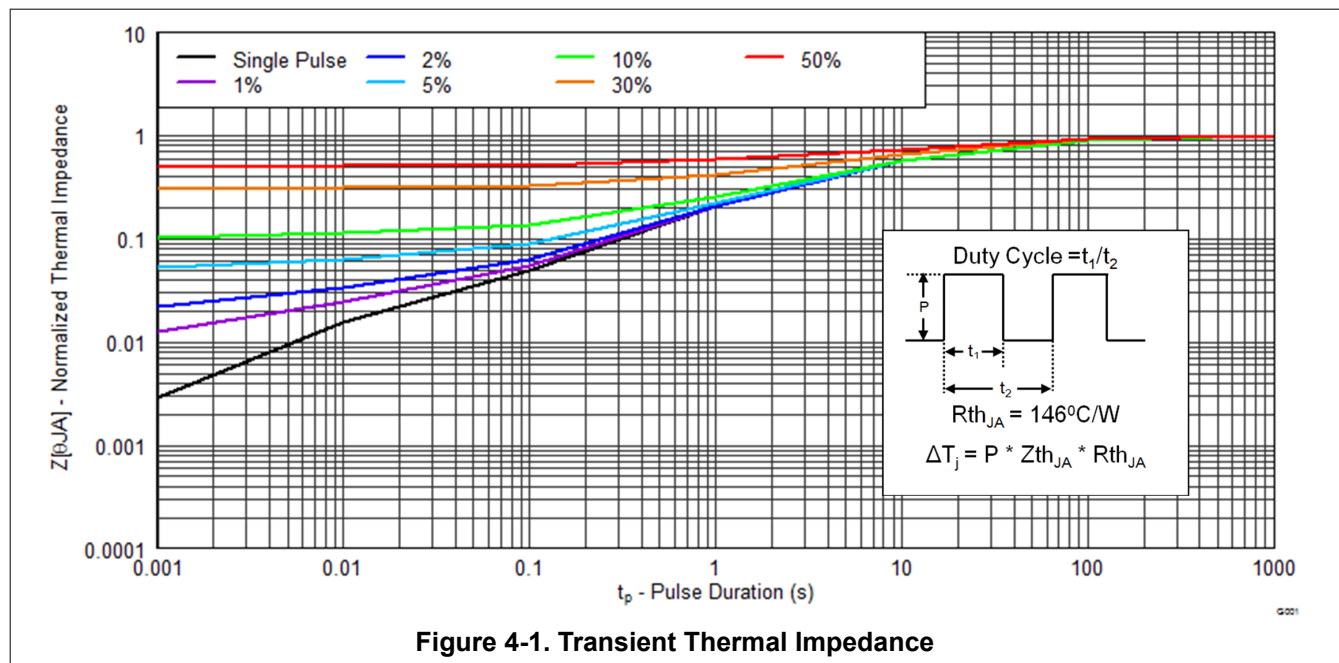
Max $R_{\theta JA} = 60^{\circ}\text{C/W}$ when mounted on 1 inch² (6.45 cm²) of 2 oz. (0.071 mm thick) Cu.



Max $R_{\theta JA} = 146^{\circ}\text{C/W}$ when mounted on a minimum pad area of 2 oz. (0.071 mm thick) Cu.

4.3 Typical MOSFET Characteristics

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)



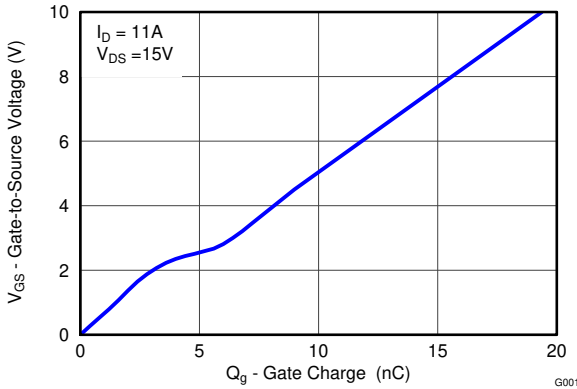


Figure 4-4. Gate Charge

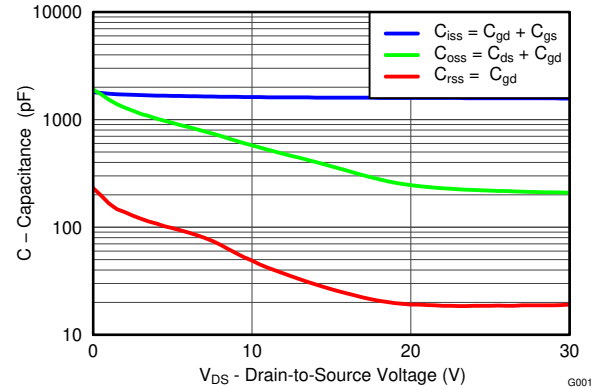


Figure 4-5. Capacitance

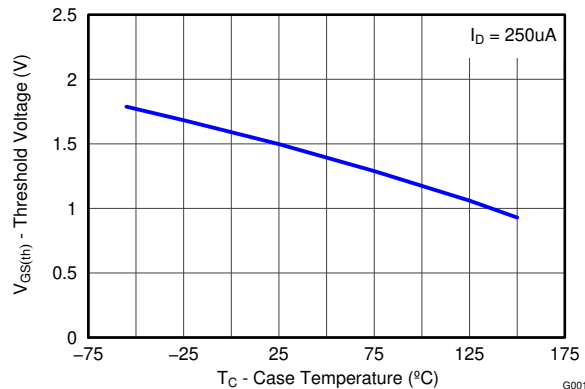


Figure 4-6. Threshold Voltage vs Temperature

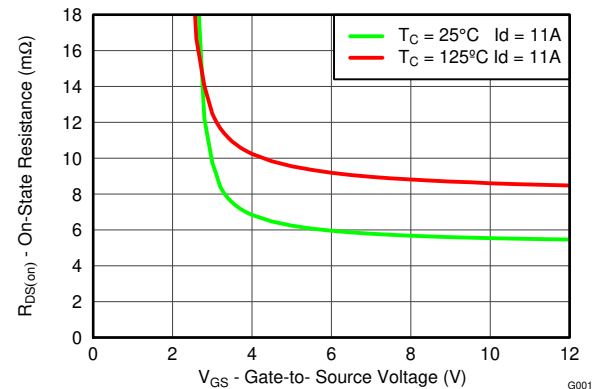


Figure 4-7. On-State Resistance vs Gate-to-Source Voltage

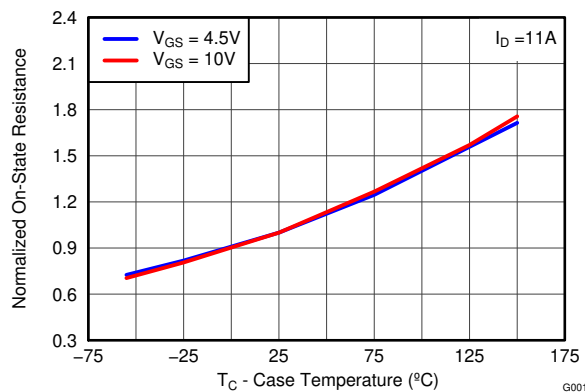


Figure 4-8. Normalized On-State Resistance vs Temperature

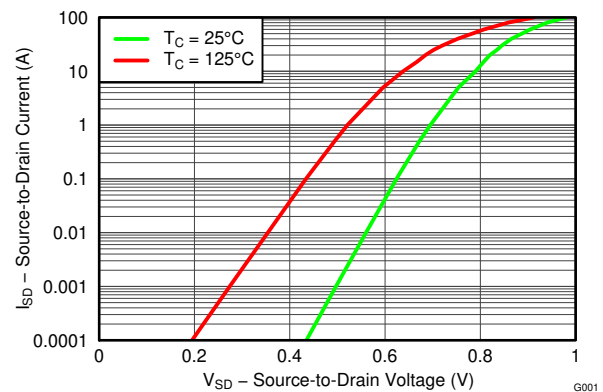
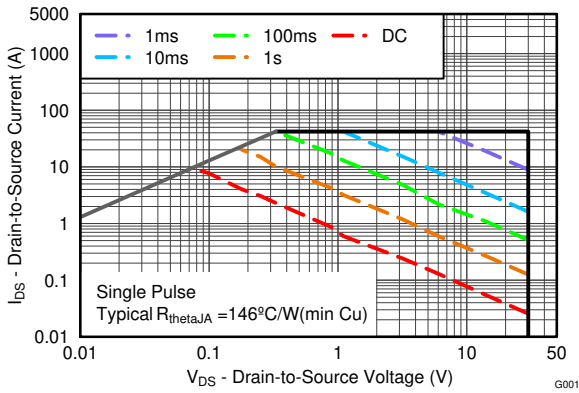
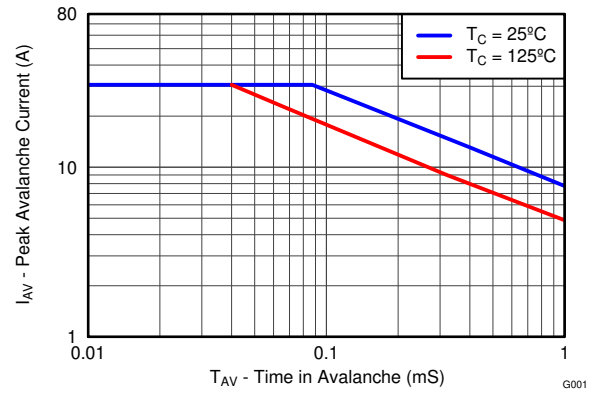
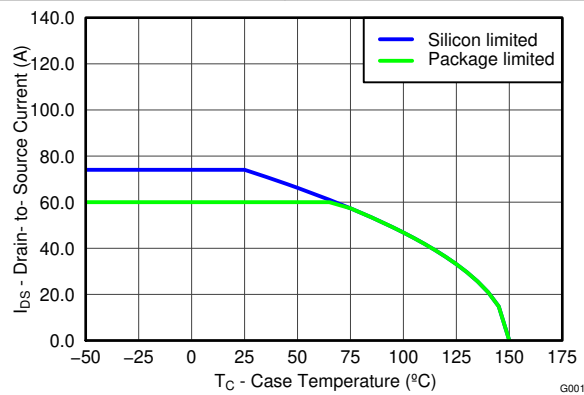


Figure 4-9. Typical Diode Forward Voltage

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**Figure 4-10. Maximum Safe Operating Area****Figure 4-11. Single Pulse Unclamped Inductive Switching****Figure 4-12. Maximum Drain Current vs Temperature**

5 Device and Documentation Support

5.1 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5.2 Trademarks

NexFET™ and TI E2E™ are trademarks of Texas Instruments.

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5.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.4 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (January 2016) to Revision C (November 2023)	Page
• Updated formatting for tables, figures, and cross-references throughout the document	1
Changes from Revision A (June 2014) to Revision B (January 2016)	Page
• Enhanced Section 3 text	1
Changes from Revision * (September 2012) to Revision A (June 2014)	Page
• Changed "Pb-Free terminal plating" feature to state "Pb Free"	1

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD17552Q3A	Active	Production	VSONP (DNH) 8	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 150	17552
CSD17552Q3A.B	Active	Production	VSONP (DNH) 8	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 150	17552

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

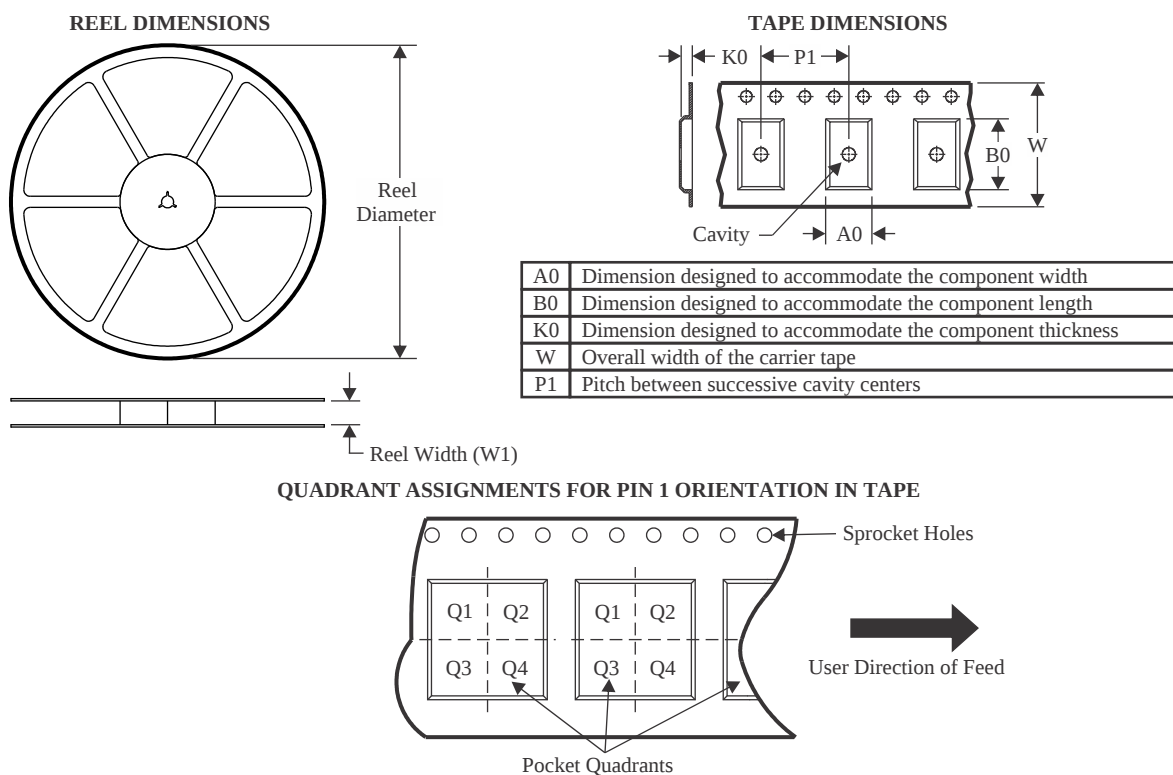
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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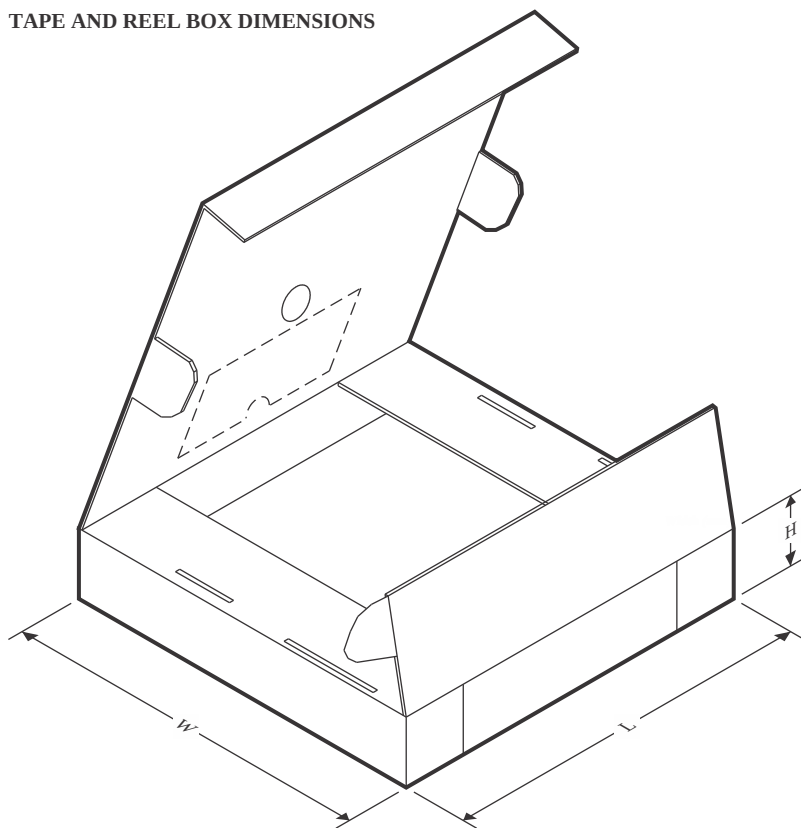
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD17552Q3A	VSONP	DNH	8	2500	330.0	12.4	3.6	3.6	1.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

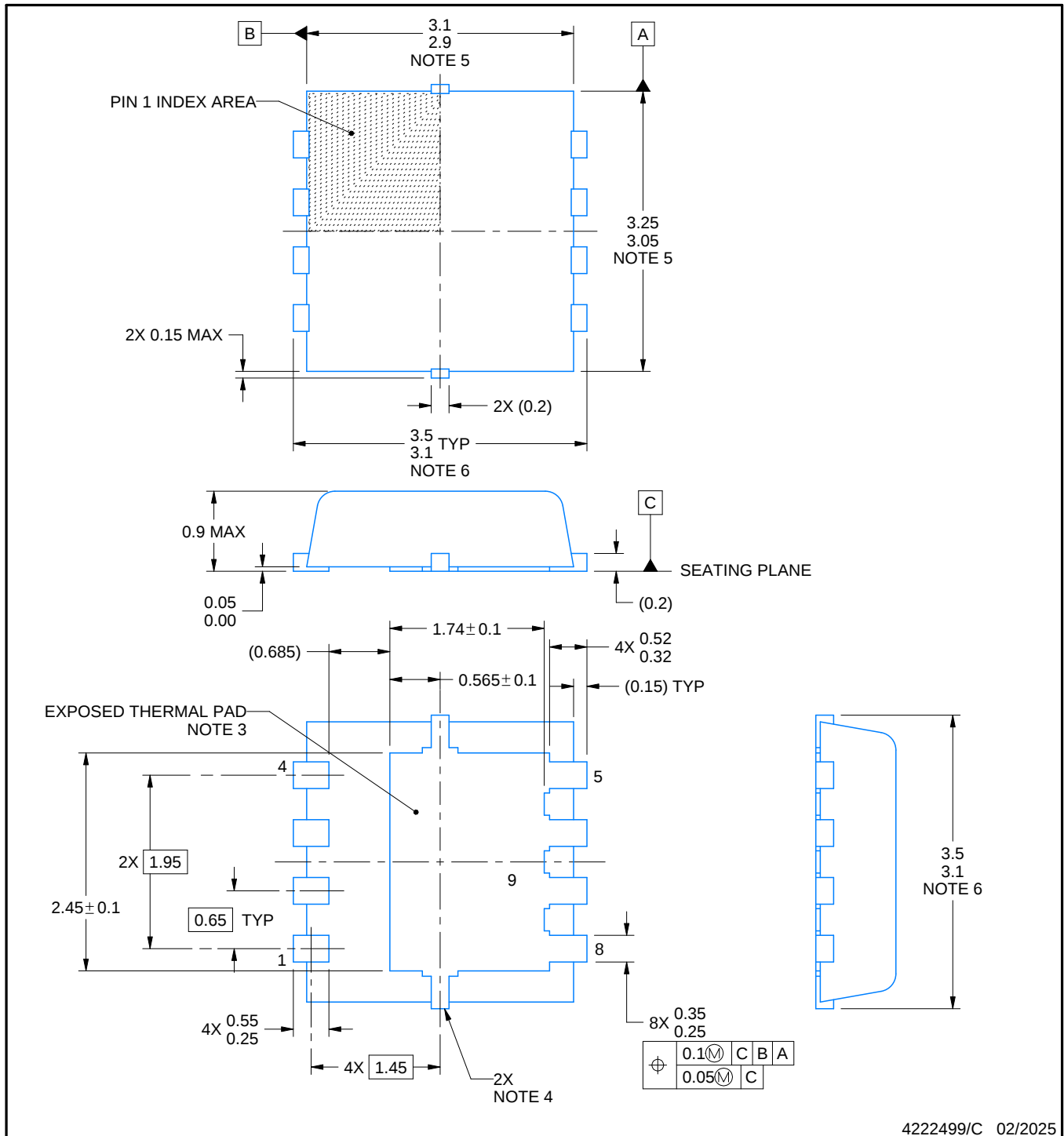
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD17552Q3A	VSONP	DNH	8	2500	340.0	340.0	38.0

DNH0008A

PACKAGE OUTLINE

VSONP - 0.9 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

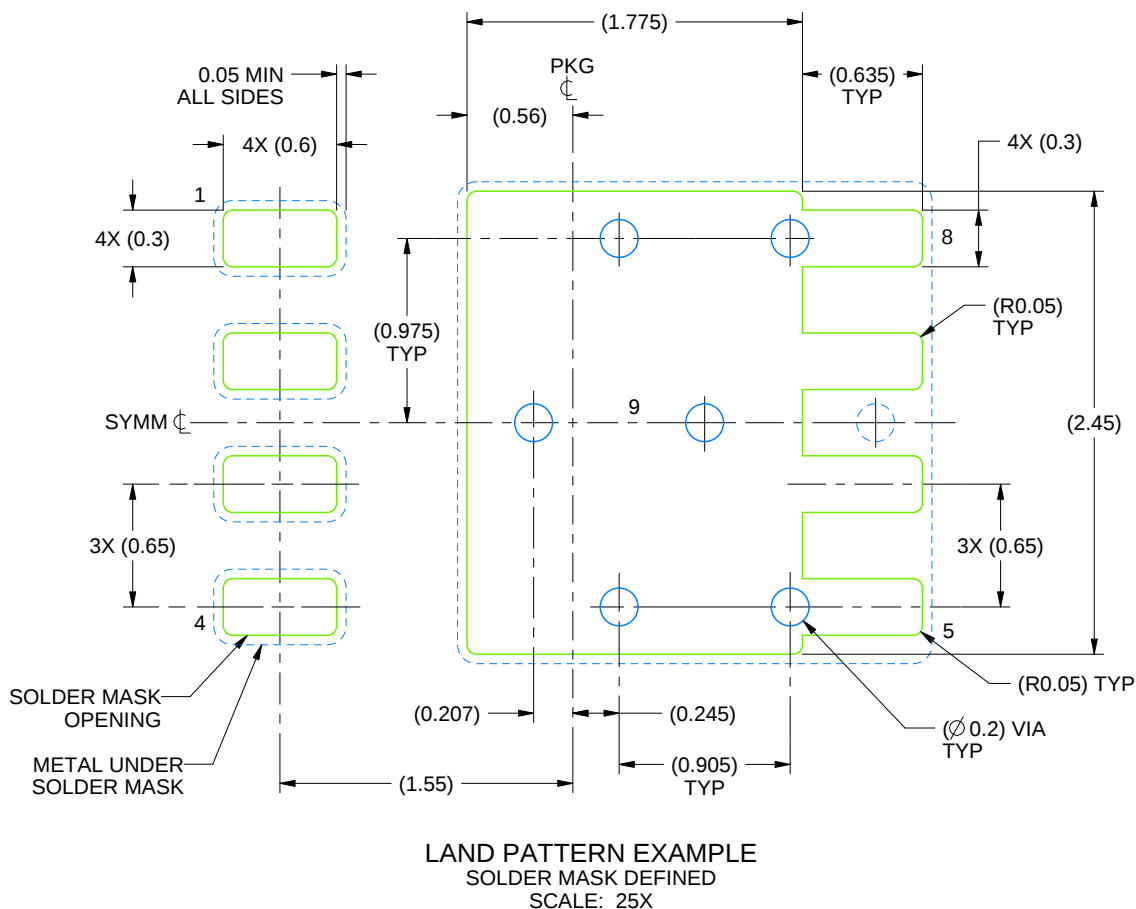
**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Metalized features are supplier options and may not be on the package.
5. These dimensions do not include mold flash protrusions or gate burrs.
6. These dimensions include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25 mm per side.

DNH0008A

VSONP - 0.9 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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NOTES: (continued)

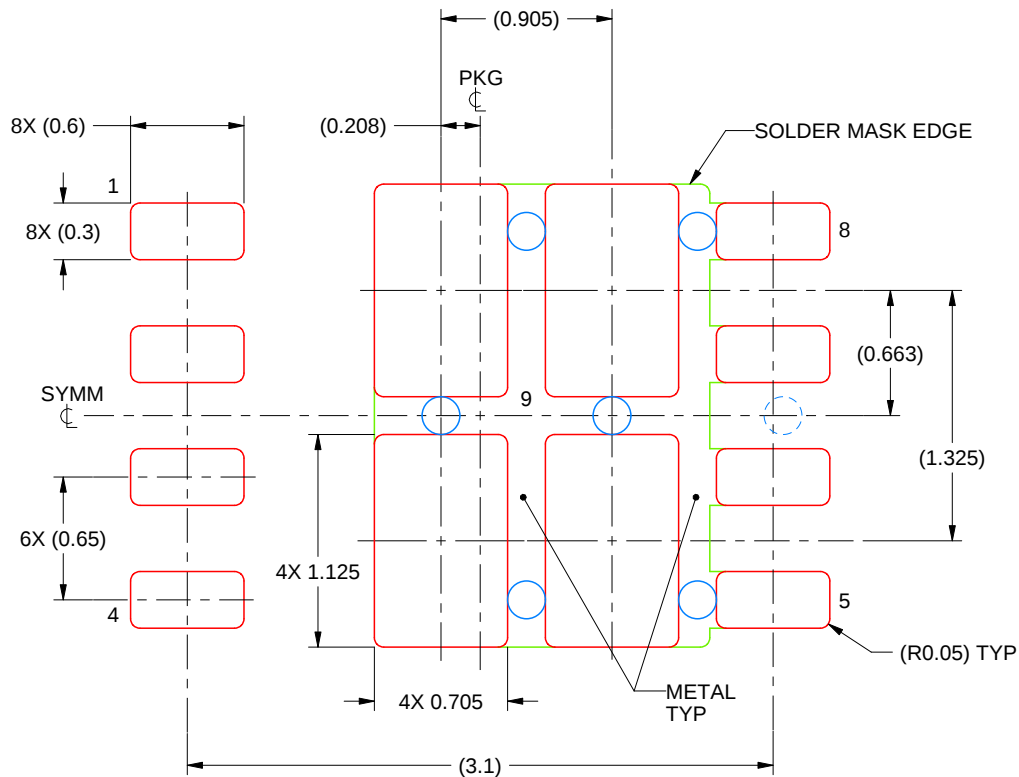
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DNH0008A

VSONP - 0.9 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 25X

4222499/C 02/2025

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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