







CSD17381F4 SLPS411G - APRIL 2013 - REVISED JANUARY 2022

CSD17381F4 30-V N-Channel FemtoFET MOSFET

1 Features

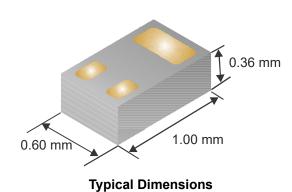
- Ultra-low on-resistance
- Ultra-low $\mathbf{Q}_{\mathbf{g}}$ and $\mathbf{Q}_{\mathbf{gd}}$
- Low threshold voltage
- Ultra-small footprint (0402 case size)
 - 1.0 mm × 0.6 mm
- Ultra-low profile
 - 0.36 mm height
- Integrated ESD protection diode
 - Rated >4 kV HBM
 - Rated >2 kV CDM
- Lead and halogen free
- RoHS compliant

2 Applications

- Optimized for load switch applications
- Optimized for general purpose switching applications
- Single-cell battery applications
- Handheld and mobile applications

3 Description

This 90 mΩ, 30 V N-Channel FemtoFET™ MOSFET technology is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing at least a 60% reduction in footprint size.



Product Summary

$T_A = 25^{\circ}$	C	TYPICAL V	UNIT	
V _{DS}	Drain-to-source voltage	30	V	
Qg	Gate charge total (4.5 V)	1040	рC	
Q _{gd}	Gate charge gate-to-drain	133	рC	
		V _{GS} = 1.8 V	160	mΩ
R _{DS(on)}	Drain-to-source on-resistance	V _{GS} = 2.5 V	V _{GS} = 2.5 V 110	
		V _{GS} = 4.5 V 90		mΩ
V _{GS(th)}	Threshold voltage	0.85	V	

Ordering Information

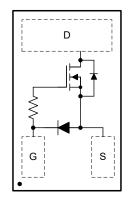
DEVICE ⁽¹⁾	QTY	MEDIA	PACKAGE	SHIP
CSD17381F4	3000	7-Inch	Femto (0402) 1.0 mm	Tape and
CSD17381F4T	250	reel	×0.6 mm SMD Lead Less	reel

For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

T _A = 25	°C unless otherwise stated	VALUE	UNIT	
V _{DS}	Drain-to-source voltage	30	V	
V _{GS}	Gate-to-source voltage	12	V	
I _D	Continuous drain current, T _A = 25°C ⁽¹⁾	3.1	Α	
I _{DM}	Pulsed Drain Current, T _A = 25°C ⁽²⁾	12	Α	
1.	Continuous gate clamp current	35	mA	
l _G	Pulsed gate clamp current ⁽²⁾	350] "	
P _D	Power dissipation ⁽¹⁾	500	mW	
ESD	Human body model (HBM)	4	kV	
Rating	Charged device model (CDM)	2	kV	
T _J , T _{stg}	Operating junction and storage temperature range	-55 to 150	°C	
E _{AS}	Avalanche energy, single pulse I_D = 7.4 A, L = 0.1 mH, R_G = 25 Ω	2.7	mJ	

- Typical $R_{\theta JA} = 90^{\circ} \text{C/W} \text{ on 1 inch}^2 (6.45 \text{ cm}^2), 2 \text{ oz.}$ (0.071 mm thick) Cu pad on a 0.06 inch (1.52 mm) thick FR4 PCB.
- Pulse duration ≤ 100 µs, duty cycle ≤ 1%.



Top View



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4 Revision History NOTE: Page numbers for previous revisions may differ Changes from Revision F (October 2021) to Revision	. •	Page							
 Changed height dimension from "0.35 mm" to "0.36 	· · · · · · · · · · · · · · · · · · ·								
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 Updated the numbering format for tables, figures, a 		1							
Changed footnote to refer to correct support docum									
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Changes from Revision D (August 2014) to Revision E (December 2017)

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Changed Pulsed Drain Current value From: 10 A To: 12 A in the Absolute Maximum Ratings table.1 Change Note 2 From: Pulse duration ≤300 µs, duty cycle ≤2% To: Pulse duration ≤ 100 µs, duty cycle ≤ 1%. 1 Updated Figure 5-1.4

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5 Specifications

5.1 Electrical Characteristics

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC	CHARACTERISTICS			,	-	
BV _{DSS}	Drain-to-Source Voltage	V _{GS} = 0 V, I _{DS} = 250 μA	30			V
I _{DSS}	Drain-to-Source Leakage Current	V _{GS} = 0 V, V _{DS} = 24 V			100	nA
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = 10 V			50	nA
V _{GS(th)}	Gate-to-Source Threshold Voltage	$V_{DS} = V_{GS}$, $I_{DS} = 250 \mu A$	0.65	0.85	1.10	V
		V _{GS} = 1.8 V, I _{DS} =0.5 A		160	250	mΩ
D	Drain-to-Source On-Resistance	V _{GS} = 2.5 V, I _{DS} =0.5 A		110	143	mΩ
R _{DS(on)}	Dialii-lo-Source On-Resistance	V _{GS} = 4.5 V, I _{DS} = 0.5 A		90	117	mΩ
		V _{GS} = 8 V, I _{DS} =0.5 A		84	109	mΩ
g _{fs}	Transconductance	V _{DS} = 15 V, I _{DS} = 0.5 A		4.8		S
DYNAMI	IC CHARACTERISTICS					
C _{iss}	Input Capacitance			150	195	pF
C _{oss}	Output Capacitance	$V_{GS} = 0 \text{ V, } V_{DS} = 15 \text{ V,}$ f = 1 MHz		44	57	pF
C _{rss}	Reverse Transfer Capacitance	J 1 WH 12		2.2	2.9	pF
R _G	Series Gate Resistance			23		Ω
Qg	Gate Charge Total (4.5 V)			1040	1350	рС
Q _{gd}	Gate Charge Gate-to-Drain	V _{DS} = 15 V, I _{DS} = 0.5 A		133		рС
Q _{gs}	Gate Charge Gate-to-Source	V _{DS} - 15 V, I _{DS} - 0.5 A		226		рС
Q _{g(th)}	Gate Charge at V _{th}			150		рС
Q _{oss}	Output Charge	V _{DS} = 15 V, V _{GS} = 0 V		1110		рС
t _{d(on)}	Turn On Delay Time			3.4		ns
t _r	Rise Time	V _{DS} = 15 V, V _{GS} = 4.5 V,		1.4		ns
t _{d(off)}	Turn Off Delay Time	$I_{DS} = 0.5 \text{ A}, R_G = 2 \Omega$		10.8		ns
t _f	Fall Time			3.6		ns
DIODE C	CHARACTERISTICS					
V _{SD}	Diode Forward Voltage	I _{SD} = 0.5 A, V _{GS} = 0 V		0.73	0.9	V
Q _{rr}	Reverse Recovery Charge	V _{DS} = 15 V, I _E = 0.5 A, di/dt = 300 A/μs		1500		рС
t _{rr}	Reverse Recovery Time	V _{DS} - 15 v, 1 _F - 0.5 A, αl/αι - 500 A/μs		5.6		ns

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

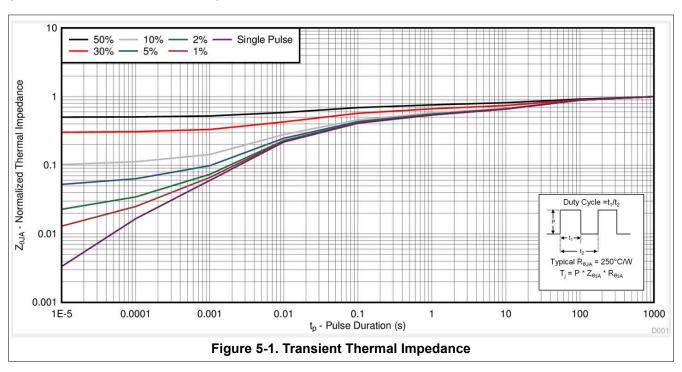
	THERMAL METRIC	TYPICAL VALUES	UNIT
D	Junction-to-Ambient Thermal Resistance ⁽¹⁾	90	°C/W
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ⁽²⁾	250	C/VV

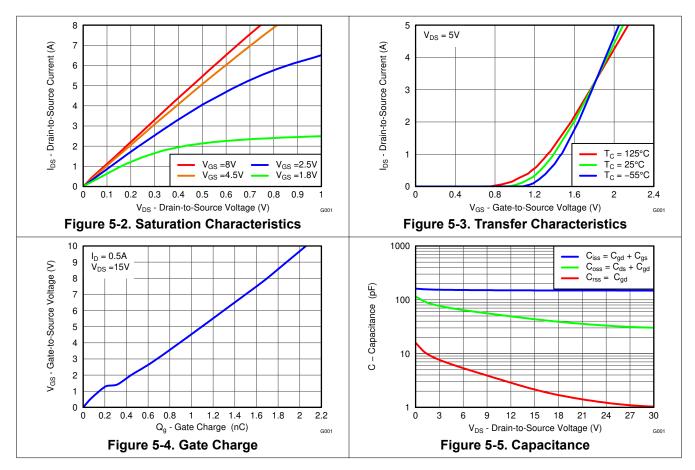
 ⁽¹⁾ Device mounted on FR4 material with 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu.
 (2) Device mounted on FR4 material with minimum Cu mounting area.



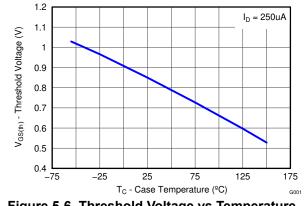
5.3 Typical MOSFET Characteristics

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$





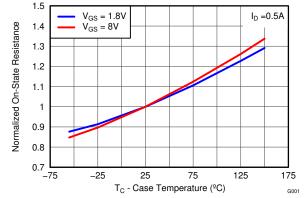
12



160 $T_C = 25^{\circ}C$ Id = 0.5A $R_{DS(on)}$ - On-State Resistance $(m\Omega)$ 150 $T_C = 125^{\circ}C \text{ Id} = 0.5A$ 140 130 120 110 100 90 80 70 60 0 6 8 V_{GS} - Gate-to- Source Voltage (V)

Figure 5-6. Threshold Voltage vs Temperature

Figure 5-7. On-State Resistance vs Gate-to-Source Voltage



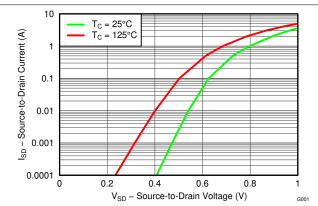
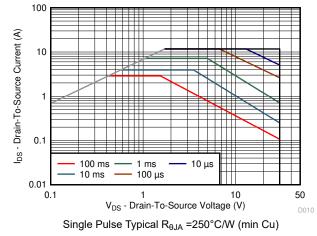


Figure 5-8. Normalized On-State Resistance vs **Temperature**

Figure 5-9. Typical Diode Forward Voltage



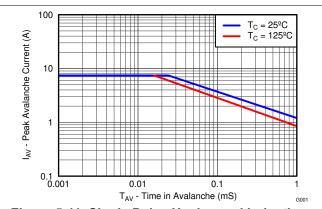
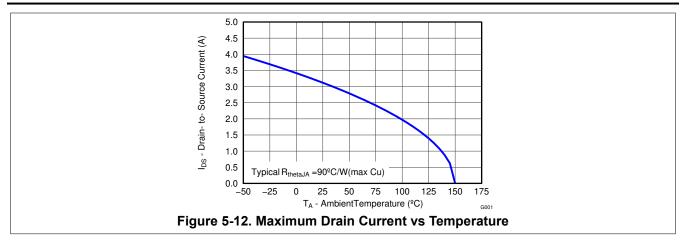


Figure 5-10. Maximum Safe Operating Area

Figure 5-11. Single Pulse Unclamped Inductive **Switching**







6 Device and Documentation Support

6.1 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6.2 Trademarks

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6.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.4 Glossary

TI Glossary

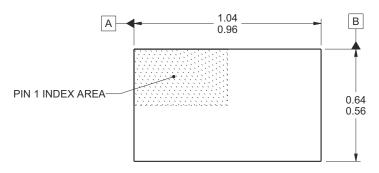
This glossary lists and explains terms, acronyms, and definitions.



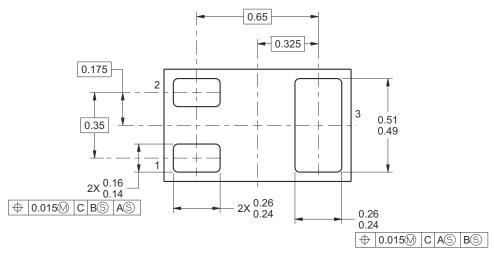
7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions



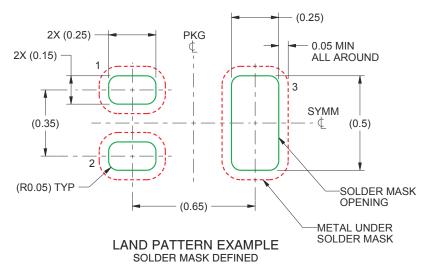




- A. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- B. This drawing is subject to change without notice.
- C. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device data sheet or contact a local TI representative.

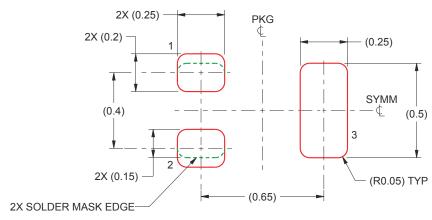


7.2 Recommended Minimum PCB Layout



- A. All dimensions are in millimeters.
- B. For more information, see FemtoFET Surface Mount Guide (SLRA003D).

7.3 Recommended Stencil Pattern



SOLDER PASTE EXAMPLE

- A. All dimensions are in millimeters.
- B. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
CSD17381F4	Active	Production	PICOSTAR (YJC) 3	3000 LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	CQ
CSD17381F4.B	Active	Production	PICOSTAR (YJC) 3	3000 LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	CQ
CSD17381F4T	Active	Production	PICOSTAR (YJC) 3	250 SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	CQ
CSD17381F4T.B	Active	Production	PICOSTAR (YJC) 3	250 SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	CQ

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

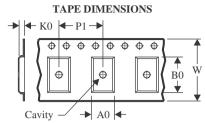
⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD17381F4	PICOSTAF	YJC	3	3000	180.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2
CSD17381F4T	PICOSTAF	YJC	3	250	180.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD17381F4	PICOSTAR	YJC	3	3000	182.0	182.0	20.0
CSD17381F4T	PICOSTAR	YJC	3	250	182.0	182.0	20.0

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Last updated 10/2025