

CSD17308Q3 30-V N-Channel NexFET™ Power MOSFETs

1 Features

- Optimized for 5-V gate drive
- Ultra-low Q_g and Q_{gd}
- Low thermal resistance
- Avalanche rated
- Lead-free terminal plating
- RoHS compliant
- Halogen free
- VSON 3.3 mm × 3.3 mm plastic package

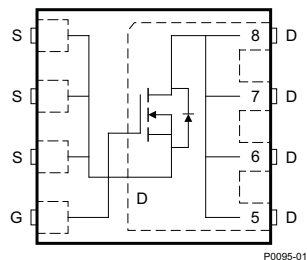
2 Applications

- Notebook point of load
- Point-of-load synchronous buck in networking, telecom, and computing systems

3 Description

This 30-V, 8.2-m Ω , 3.3 mm × 3.3 mm VSON NexFET™ power MOSFET is designed to minimize losses in power conversion applications and optimized for 5-V gate drive applications.

Top View



P0095-01

Product Summary

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{DS}	Drain-to-source voltage	30	V
Q_g	Gate charge total (4.5 V)	3.9	nC
Q_{gd}	Gate charge gate-to-drain	0.8	nC
$R_{DS(on)}$	Drain-to-source on-resistance	$V_{GS} = 3\text{ V}$	12.5
		$V_{GS} = 4.5\text{ V}$	9.4
		$V_{GS} = 8\text{ V}$	8.2
$V_{GS(th)}$	Threshold voltage	1.3	V

Device Information⁽¹⁾

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD17308Q3	2500	13-Inch Reel	SON 3.30 mm × 3.30 mm Plastic Package	Tape and Reel

(1) For all available packages, see the orderable addendum at the end of the data sheet.

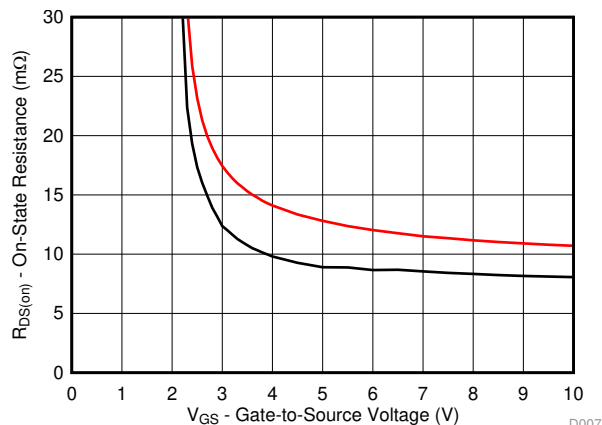
Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
V_{DS}	Drain-to-source voltage	30	V
V_{GS}	Gate-to-source voltage	+10 / -8	V
I_D	Continuous drain current (package limited)	50	A
	Continuous drain current, $T_C = 25^\circ\text{C}$	44	
	Continuous drain current ⁽¹⁾	14	
I_{DM}	Pulsed drain current, $T_A = 25^\circ\text{C}$ ⁽²⁾	167	A
P_D	Power dissipation ⁽¹⁾	2.7	W
	Power dissipation, $T_C = 25^\circ\text{C}$	28	
T_J , T_{stg}	Operating junction and storage temperature	-55 to 150	$^\circ\text{C}$
E_{AS}	Avalanche energy, single pulse $I_D = 36\text{ A}$, $L = 0.1\text{ mH}$, $R_G = 25\ \Omega$	65	mJ

(1) Typical $R_{\theta JA} = 46^\circ\text{C/W}$ when mounted on a 1-in² (6.45-cm²), 2-oz (0.071-mm) thick Cu pad on a 0.06-in (1.52-mm) thick FR4 PCB.

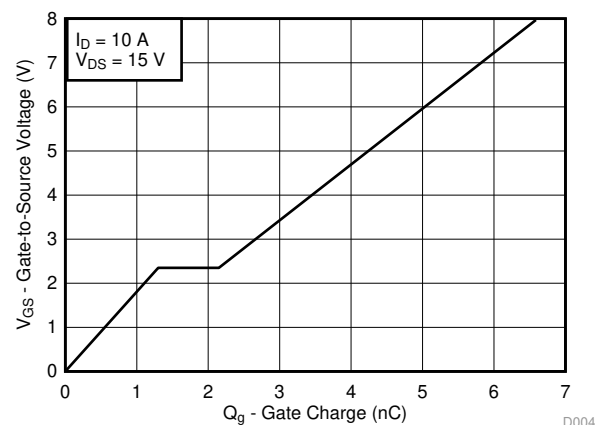
(2) Max $R_{\theta JC} = 4.5^\circ\text{C/W}$, pulse duration $\leq 100\ \mu\text{s}$, duty cycle $\leq 1\%$.

$R_{DS(on)}$ vs V_{GS}



D007

Gate Charge



D004



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2015) to Revision C Page

- Changed $V_{GS(th)}$ MAX specification in the *Electrical Characteristics* table, From 1.8 V : To 1.6 V **3**

Changes from Revision A (February 2010) to Revision B Page

- Added part number to title **1**
- Added Package Limited Continuous Drain Current **1**
- Added line for Power Dissipation, $T_C = 25^\circ\text{C}$ in *Absolute Maximum Ratings* table **1**
- Updated pulsed current conditions **1**
- Updated [Figure 1](#) to show $R_{\theta JC}$ curves **5**
- Added 4.5 V curve in [Figure 8](#) **6**
- Updated [Figure 10](#) **7**
- Added the *Device and Documentation Support* section **8**
- Updated the [Mechanical, Packaging, and Orderable Information](#) section **9**

Changes from Original (February 2010) to Revision A Page

- Deleted the Package Marking Information section **11**

5 Specifications

5.1 Electrical Characteristics

 $T_A = 25^\circ\text{C}$ unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-source voltage	V _{GS} = 0 V, I _D = 250 μA	30			V
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0 V, V _{DS} = 24 V			1	μA
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0 V, V _{GS} = +10 / –8 V			100	nA
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	0.9	1.3	1.6	V
R _{DS(on)}	Drain-to-source on-resistance	V _{GS} = 3 V, I _D = 10 A		12.5	16.5	mΩ
		V _{GS} = 4.5 V, I _D = 10 A		9.4	11.8	
		V _{GS} = 8 V, I _D = 10 A		8.2	10.3	
g _{fs}	Transconductance	V _{DS} = 15 V, I _D = 10 A		37		S
DYNAMIC CHARACTERISTICS						
C _{ISS}	Input capacitance	V _{GS} = 0 V, V _{DS} = 15 V, f = 1 MHz		540	700	pF
C _{OSS}	Output capacitance			280	365	pF
C _{RSS}	Reverse transfer capacitance			27	35	pF
R _g	Series gate resistance	V _{DS} = 15 V, I _D = 10 A		0.9	1.8	Ω
Q _g	Gate charge total (4.5 V)			3.9	5.1	nC
Q _{gd}	Gate charge gate-to-drain			0.8		nC
Q _{gs}	Gate charge gate-to-source			1.3		nC
Q _{g(th)}	Gate charge at V _{th}			0.7		nC
Q _{OSS}	Output charge	V _{DS} = 13 V, V _{GS} = 0 V		7.4		nC
t _{d(on)}	Turnon delay time	V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 10 A, R _G = 2 Ω		4.5		ns
t _r	Rise time			5.7		ns
t _{d(off)}	Turnoff delay time			9.9		ns
t _f	Fall time			2.3		ns
DIODE CHARACTERISTICS						
V _{SD}	Diode forward voltage	I _{DS} = 10 A, V _{GS} = 0 V		0.85	1	V
Q _{rr}	Reverse recovery charge	V _{DD} = 13 V, I _F = 10 A, di/dt = 300 A/μs		9.3		nC
t _{rr}	Reverse recovery time			14.3		ns

5.2 Thermal Information

 $T_A = 25^\circ\text{C}$ unless otherwise stated

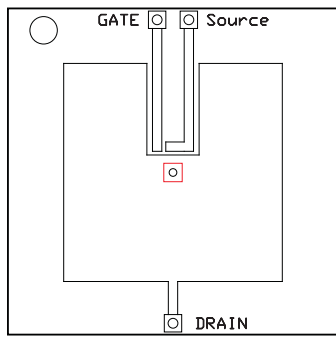
THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance ⁽¹⁾			4.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾⁽²⁾			58	$^\circ\text{C}/\text{W}$

- (1) $R_{\theta JC}$ is determined with the device mounted on a 1-in² (6.45-cm²), 2-oz (0.071-mm) thick Cu pad on a 1.5-in $\times$ 1.5-in (3.81-cm $\times$ 3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-in² (6.45-cm²), 2-oz (0.071-mm) thick Cu.

CSD17308Q3

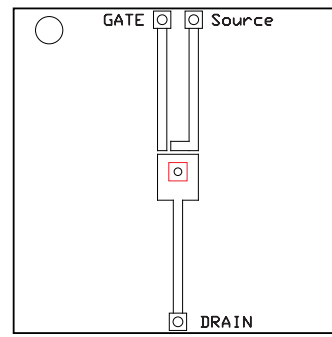
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Max $R_{\theta JA} = 58^{\circ}\text{C/W}$
when mounted on 1 in²
(6.45 cm²) of
2-oz (0.071-mm) thick
Cu.

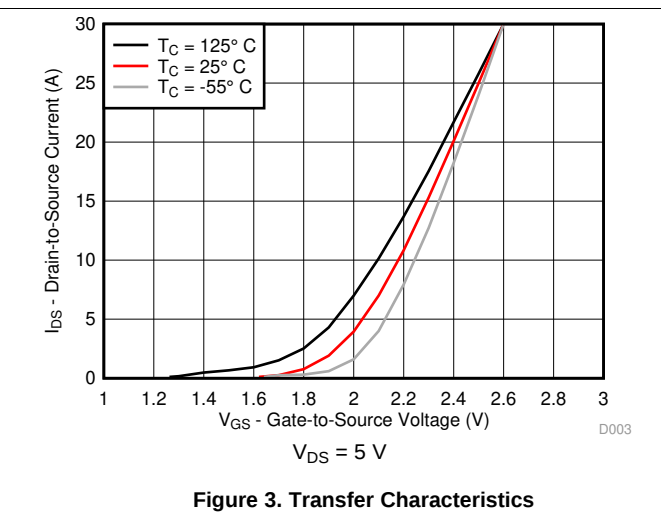
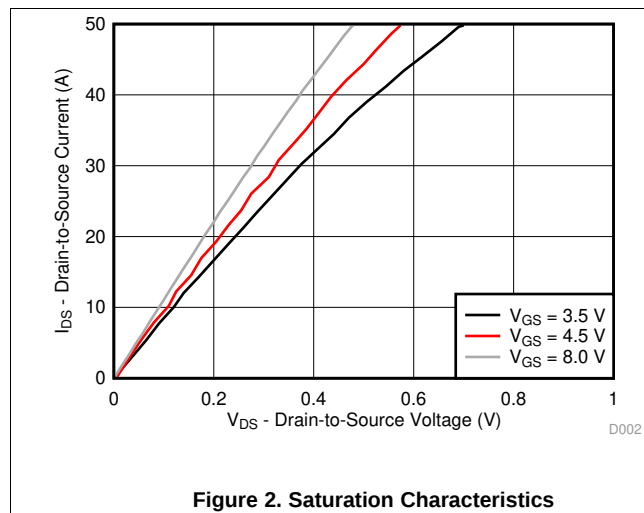
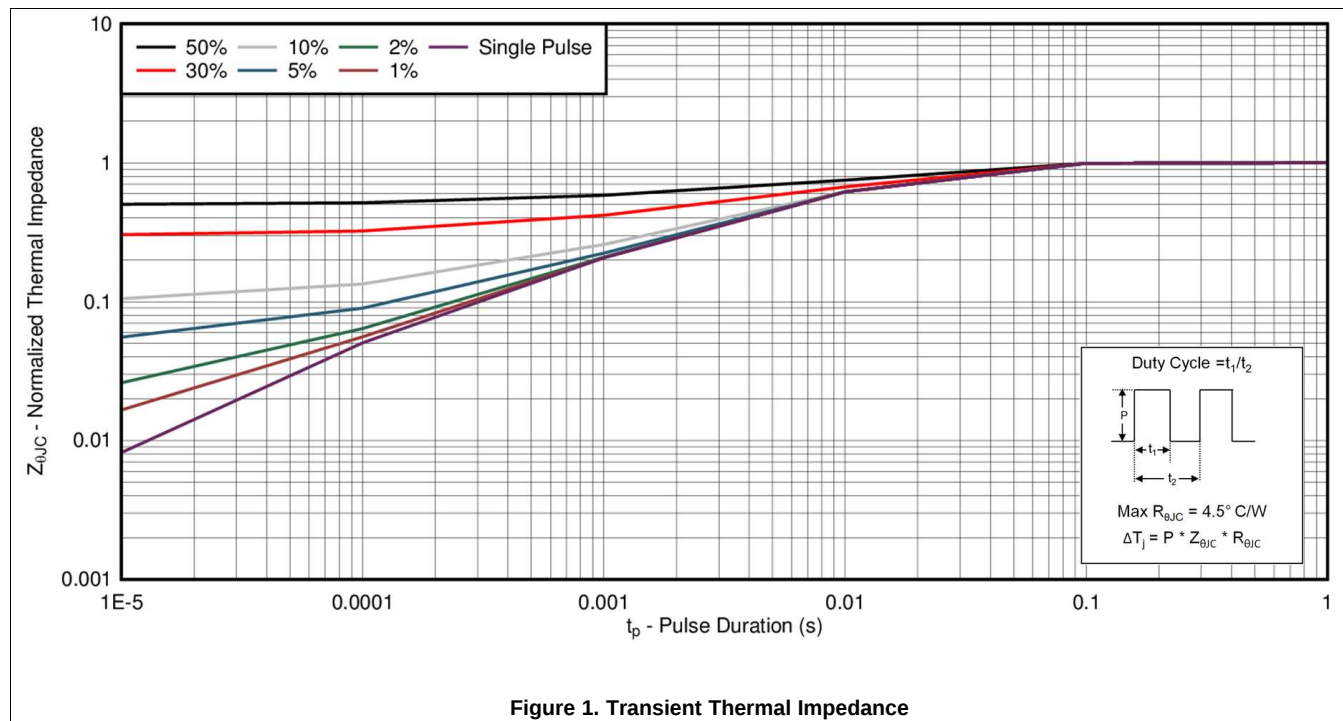


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Max $R_{\theta JA} = 165^{\circ}\text{C/W}$
when mounted on a
minimum pad area of
2-oz (0.071-mm) thick
Cu.

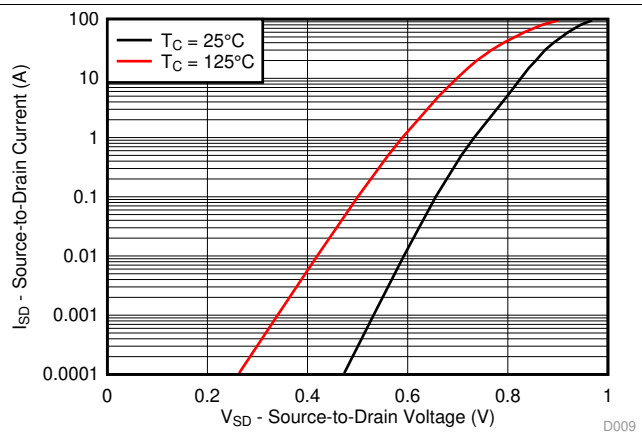
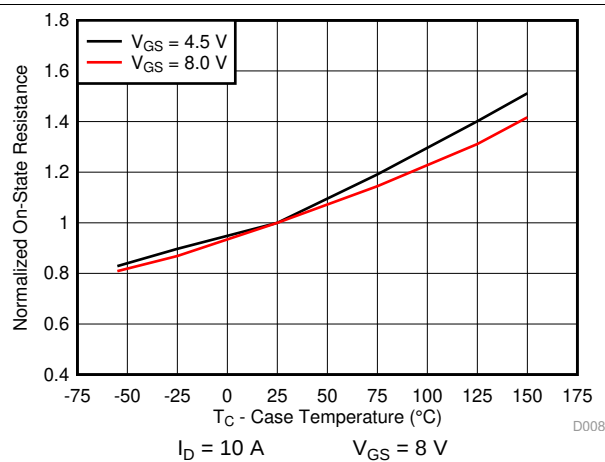
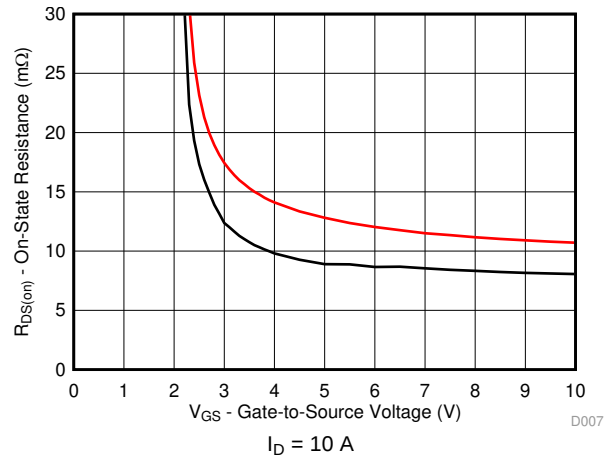
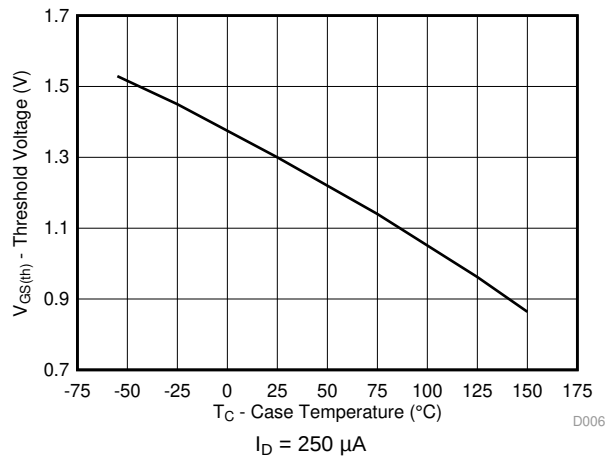
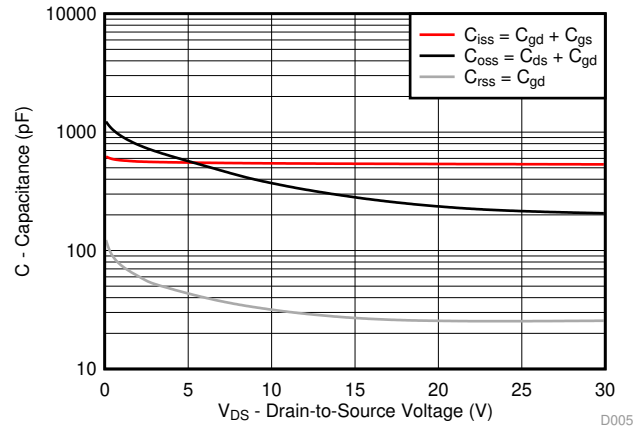
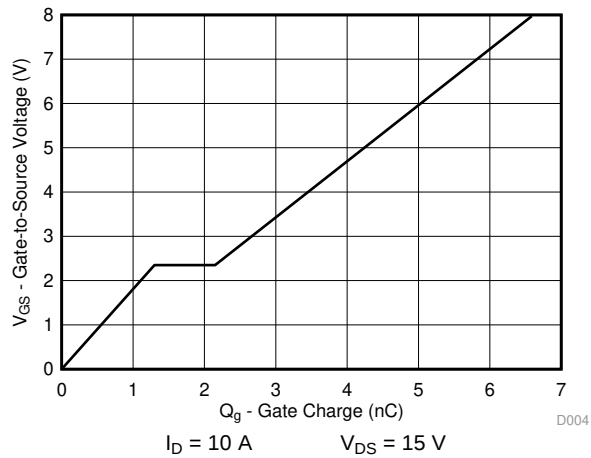
5.3 Typical MOSFET Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise stated



Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ unless otherwise stated



Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ unless otherwise stated

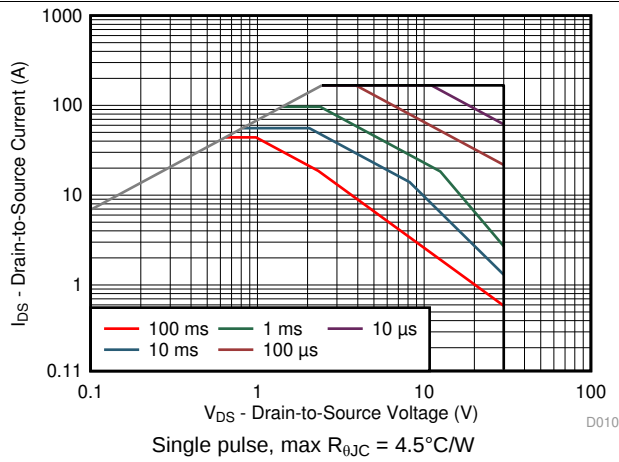


Figure 10. Maximum Safe Operating Area

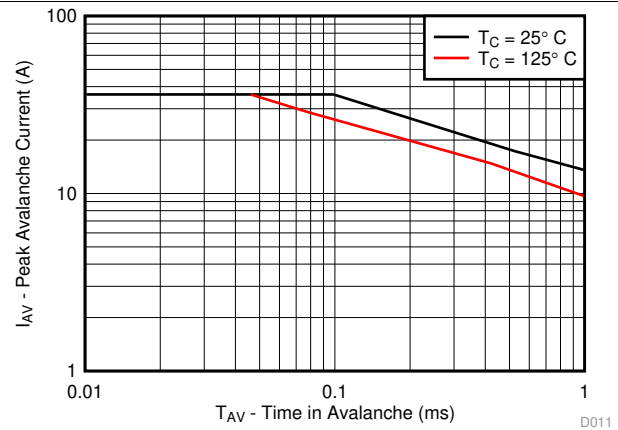


Figure 11. Single Pulse Unclamped Inductive Switching

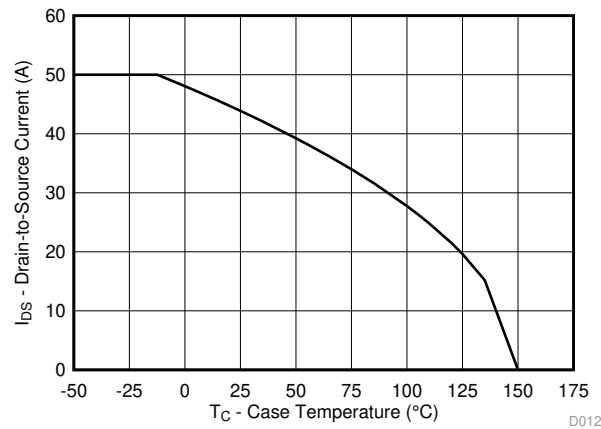


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6.2 Trademarks

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All other trademarks are the property of their respective owners.

6.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.4 Glossary

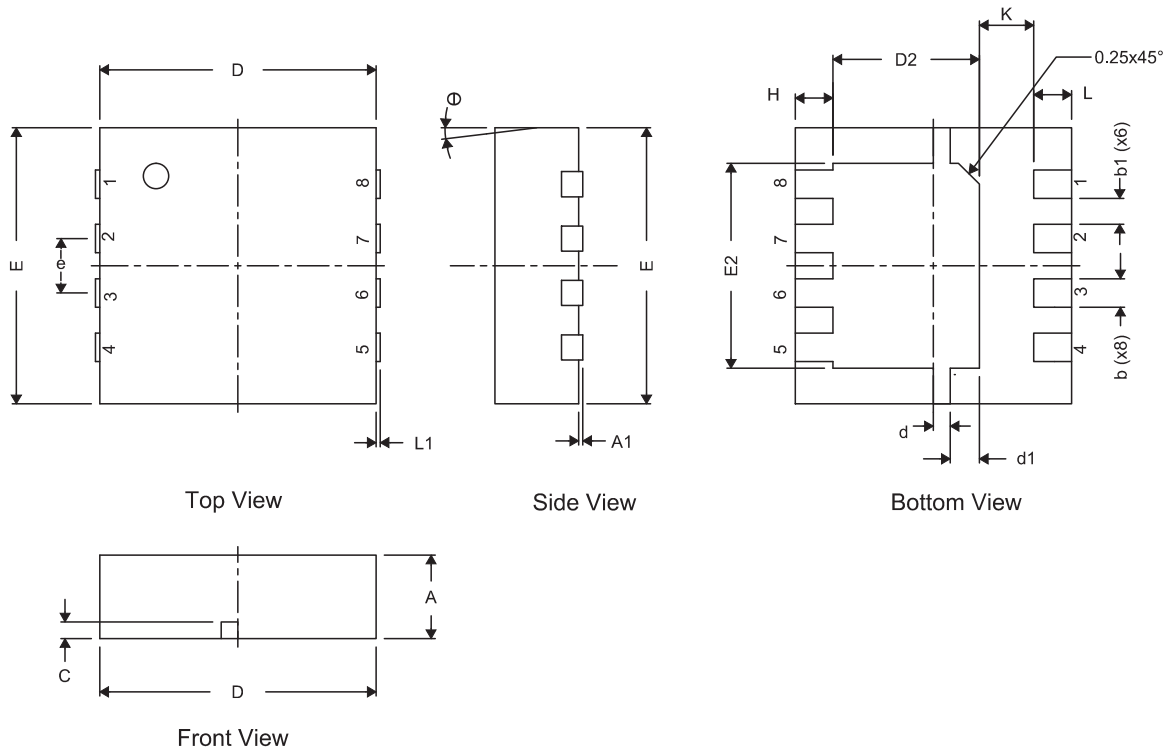
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

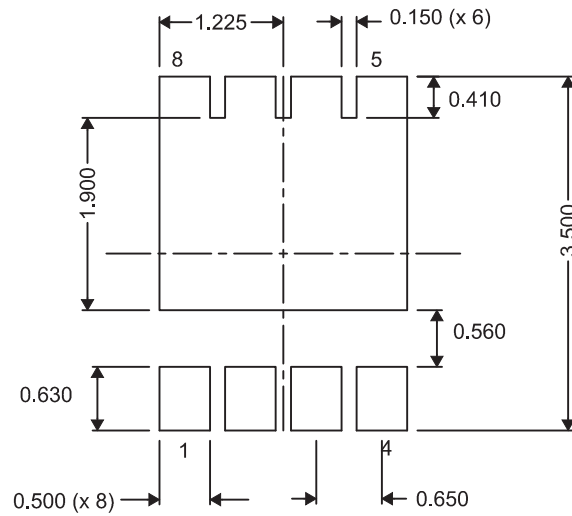
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Q3 Package Dimensions



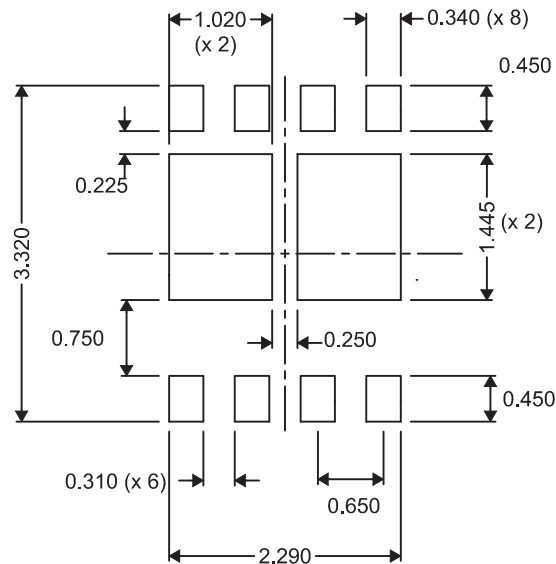
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
b1	0.310 NOM			0.012 NOM		
c	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D2	1.650	1.750	1.800	0.065	0.069	0.071
d	0.150	0.200	0.250	0.006	0.008	0.010
d1	0.300	0.350	0.400	0.012	0.014	0.016
E	3.200	3.300	3.400	0.126	0.130	0.134
E2	2.350	2.450	2.550	0.093	0.096	0.100
e	0.650 TYP			0.026 TYP		
H	0.35	0.450	0.550	0.014	0.018	0.022
K	0.650 TYP			0.026 TYP		
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	0	—	0	0	—	0
θ	0	—	0	0	—	0

7.2 Recommended PCB Pattern



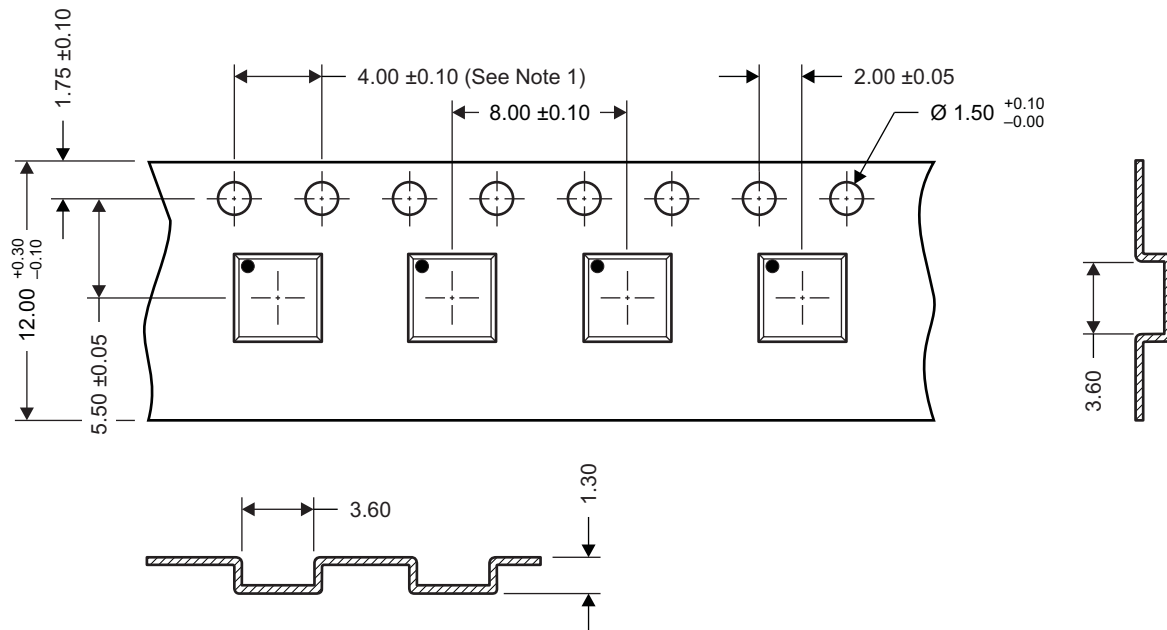
For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

7.3 Recommended Stencil Opening



All dimensions are in mm, unless otherwise specified.

7.4 Q3 Tape and Reel Information



M0144-01

Notes:

1. 10 sprocket hole pitch cumulative tolerance ± 0.2
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
3. Material: black static dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified).
5. Thickness: 0.30 ± 0.05 mm
6. MSL1 260°C (IR and Convection) PbF-Reflow Compatible

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD17308Q3	Active	Production	VSON-CLIP (DQG) 8	2500 LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17308
CSD17308Q3.B	Active	Production	VSON-CLIP (DQG) 8	2500 LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17308
CSD17308Q3T	Active	Production	VSON-CLIP (DQG) 8	250 SMALL T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17308
CSD17308Q3T.B	Active	Production	VSON-CLIP (DQG) 8	250 SMALL T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17308

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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