

N-Channel NexFET™ Power MOSFET

1 Features

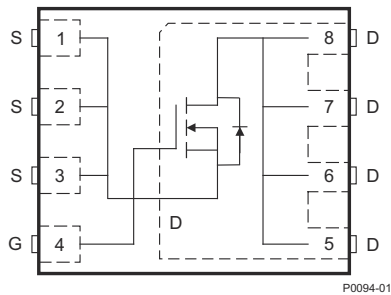
- Ultralow Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- SON 5-mm × 6-mm Plastic Package

2 Applications

- Point-of-Load Synchronous Buck in Networking, Telecom and Computing Systems
- Optimized for Control FET Applications

3 Description

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.



Top View

Product Summary

V_{DS}	Drain-to-source voltage	25	V
Q_g	Gate charge, total (4.5 V)	6.7	nC
Q_{gd}	Gate charge, gate-to-drain	1.9	nC
$r_{DS(on)}$	Drain-to-source on-resistance	$V_{GS} = 4.5\text{ V}$	5.4 mΩ
		$V_{GS} = 10\text{ V}$	3.6 mΩ
$V_{GS(th)}$	Threshold voltage	1.8	V

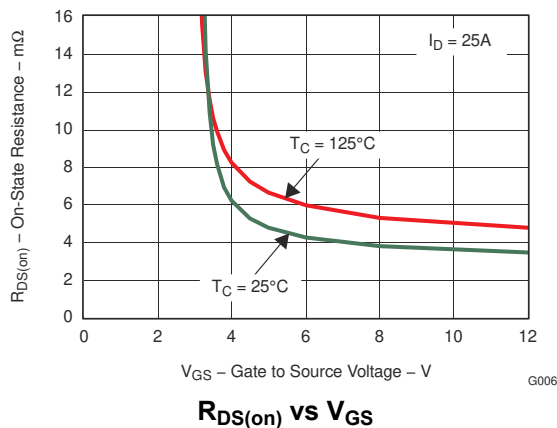
Ordering Information

Device	Package	Media	Qty	Ship
CSD16408Q5	SON 5-mm × 6-mm plastic package	13-inch (33-cm) reel	2500	Tape and reel

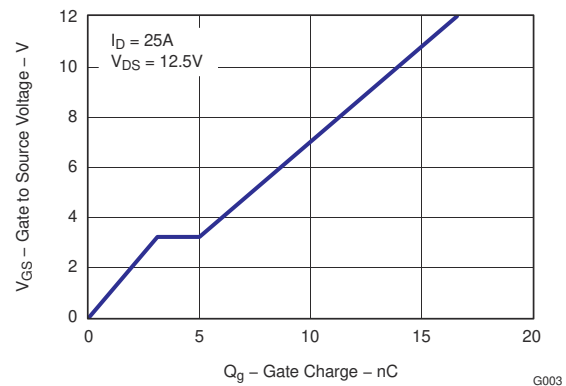
ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
V_{DS}	Drain-to-source voltage	25	V
V_{GS}	Gate-to-source voltage	–12 to 16	V
I_D	Continuous drain current, $T_C = 25^\circ\text{C}$	113	A
	Continuous drain current ⁽¹⁾	22	A
I_{DM}	Pulsed drain current, $T_A = 25^\circ\text{C}$ ⁽²⁾	141	A
P_D	Power dissipation ⁽¹⁾	3.1	W
T_J , T_{STG}	Operating junction and storage temperature range	–55 to 150	$^\circ\text{C}$
E_{AS}	Avalanche energy, single-pulse $I_D = 23\text{ A}$, $L = 0.1\text{ mH}$, $R_G = 25\text{ }\Omega$	126	mJ

- (1) Typical $R_{\theta JA} = 41^\circ\text{C/W}$ on 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.
- (2) Pulse duration $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$



$R_{DS(on)}$ vs V_{GS}



GATE CHARGE



Table of Contents

1 Features	1	5 Electrical Characteristics	3
2 Applications	1	6 Thermal Characteristics	3
3 Description	1	7 Typical MOSFET Characteristics	4
4 Revision History	2	8 Mechanical, Packaging, and Orderable Information	7

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2010) to Revision B (October 2023) Page

- Updated the numbering format for tables, figures, and cross-references throughout the document..... [1](#)

Changes from Revision * (October 2009) to Revision A (September 2010) Page

- Deleted environmental bullets from features list..... [1](#)

5 Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise stated

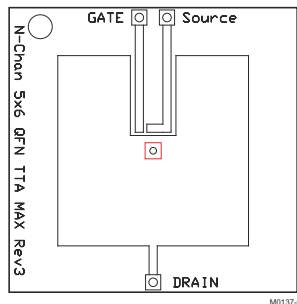
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV _{DSS}	Drain-to-source voltage	V _{GS} = 0 V, I _D = 250 μA	25			V
I _{DSS}	Drain-to-source leakage	V _{GS} = 0 V, V _{DS} = 20 V			1	μA
I _{GSS}	Gate-to-source leakage	V _{DS} = 0 V, V _{GS} = −12 V to 16 V			100	nA
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	1.4	1.8	2.1	V
r _{DS(on)}	Drain-to-source on-resistance	V _{GS} = 4.5 V, I _D = 25 A		5.4	6.8	mΩ
		V _{GS} = 10 V, I _D = 25 A		3.6	4.5	mΩ
g _{fs}	Transconductance	V _{DS} = 15 V, I _D = 25 A		60		S
Dynamic Characteristics						
C _{ISS}	Input capacitance	V _{GS} = 0 V, V _{DS} = 12.5 V , f = 1 MHz		990	1300	pF
C _{OSS}	Output capacitance			760	1000	pF
C _{RSS}	Reverse transfer capacitance			75	100	pF
R _g	Series gate resistance			0.8	1.6	Ω
Q _g	Gate charge total (4.5 V)	V _{DS} = 12.5 V, I _D = 25 A		6.7	8.9	nC
Q _{gd}	Gate charge, gate-to-drain			1.9		nC
Q _{gs}	Gate charge, gate-to-source			3.1		nC
Q _{g(th)}	Gate charge at V _{th}			1.8		nC
Q _{OSS}	Output charge	V _{DS} = 13 V, V _{GS} = 0 V		15.7		nC
t _{d(on)}	Turnon delay time	V _{DS} = 12.5 V, V _{GS} = 4.5 V, I _D = 20 A, R _G = 2 Ω		11.3		ns
t _r	Rise time			25		ns
t _{d(off)}	Turnoff delay time			11		ns
t _f	Fall time			10.8		ns
Diode Characteristics						
V _{SD}	Diode forward voltage	I _S = 25 A, V _{GS} = 0 V		0.8	1	V
Q _{rr}	Reverse recovery charge	V _{DD} = 13 V, I _F = 2 5A, di/dt = 300 A/μs		17		nC
t _{rr}	Reverse recovery time	V _{DD} = 13 V, I _F = 25 A, di/dt = 300 A/μs		21		ns

6 Thermal Characteristics

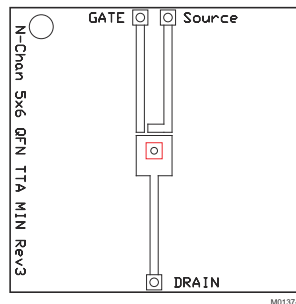
$T_A = 25^\circ\text{C}$ unless otherwise stated

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case ⁽¹⁾			1.9	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ^{(1) (2)}			51	$^\circ\text{C}/\text{W}$

- (1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch $\times$ 1.5-inch (3.81-cm $\times$ 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



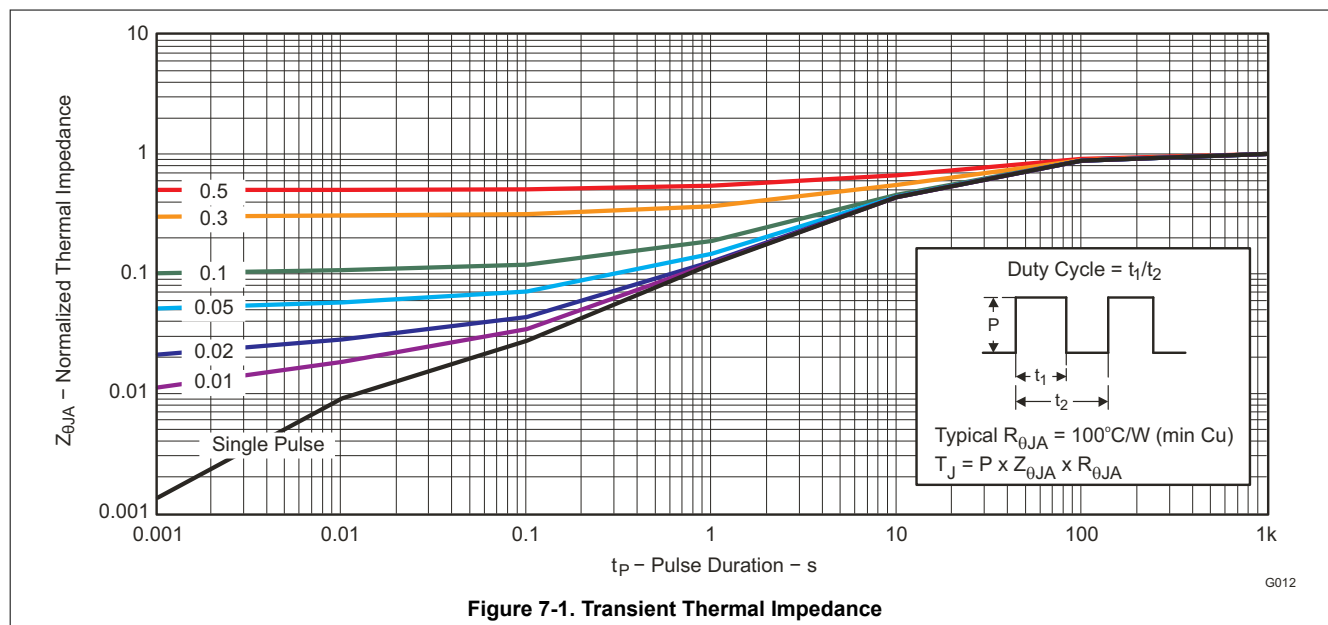
Max $R_{\theta JA} = 51^{\circ}\text{C/W}$
when mounted on 1 inch²
(6.45 cm²) of 2-oz. (0.071-mm
thick) Cu.



Max $R_{\theta JA} = 125^{\circ}\text{C/W}$ when
mounted on minimum pad
area of 2-oz. (0.071-mm
thick) Cu.

7 Typical MOSFET Characteristics

$T_A = 25^{\circ}\text{C}$ unless otherwise stated



7 Typical MOSFET Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise stated

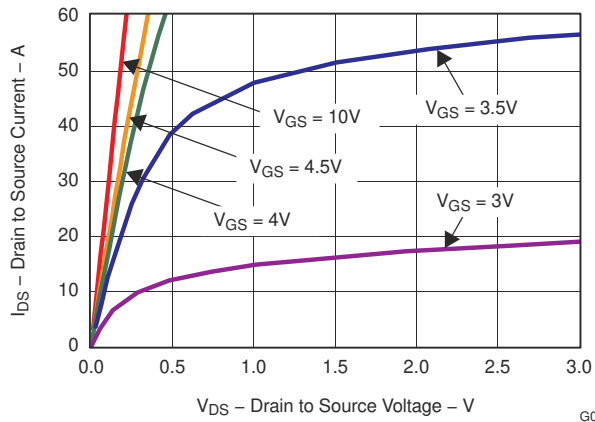


Figure 7-2. Saturation Characteristics

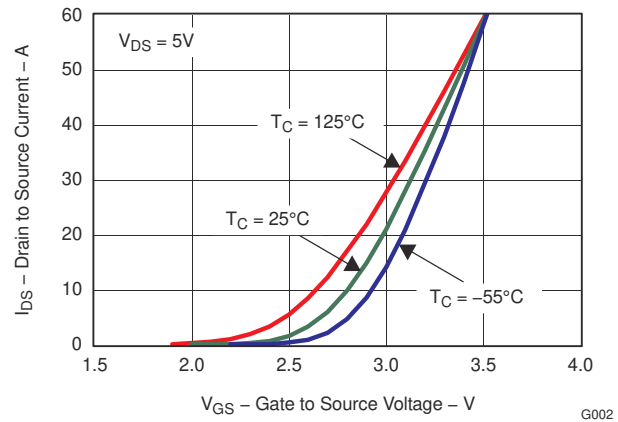


Figure 7-3. Transfer Characteristics

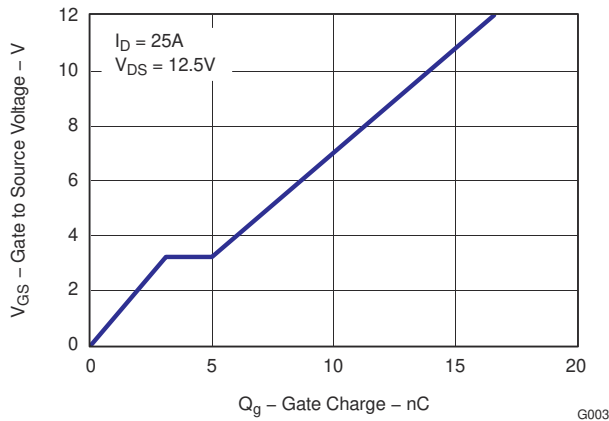


Figure 7-4. Gate Charge

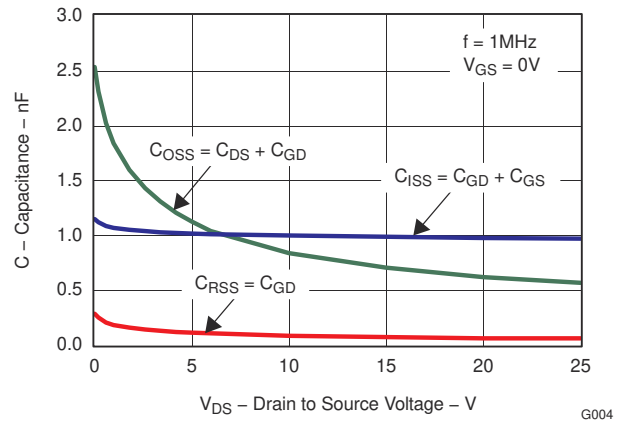


Figure 7-5. Capacitance

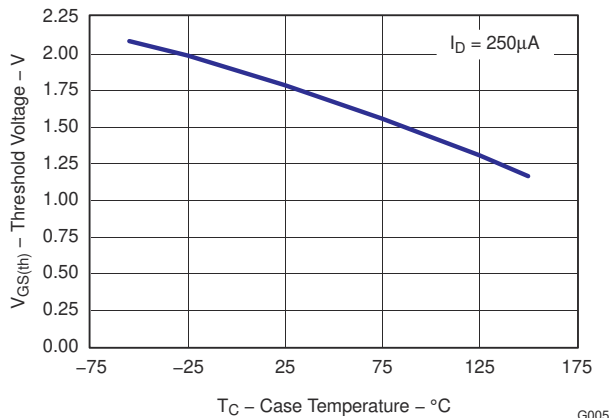


Figure 7-6. Threshold Voltage vs. Temperature

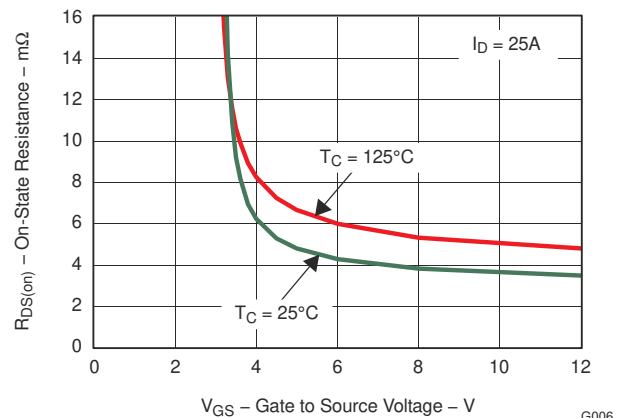


Figure 7-7. On-State Resistance vs. Gate-to-Source Voltage

7 Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ unless otherwise stated

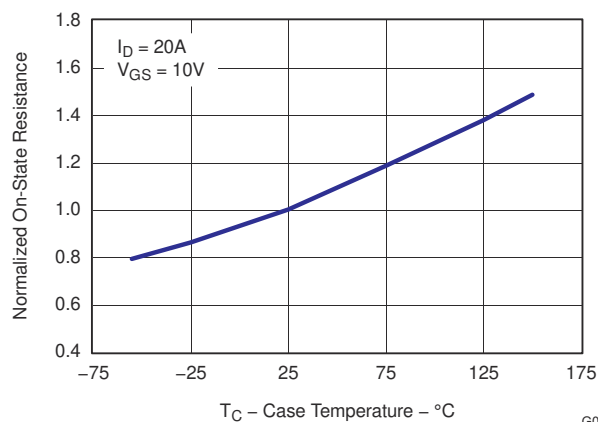


Figure 7-8. Normalized On-State Resistance vs. Temperature

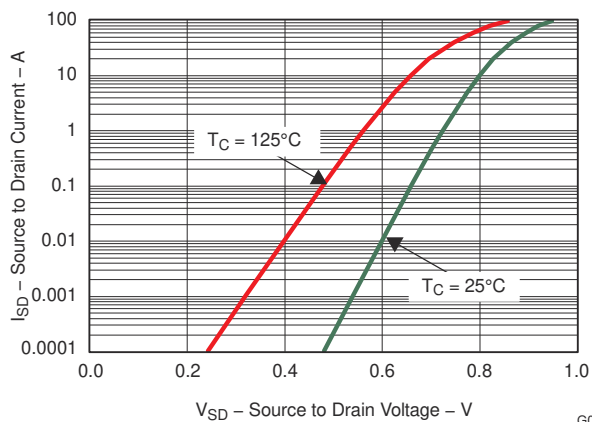


Figure 7-9. Typical Diode Forward Voltage

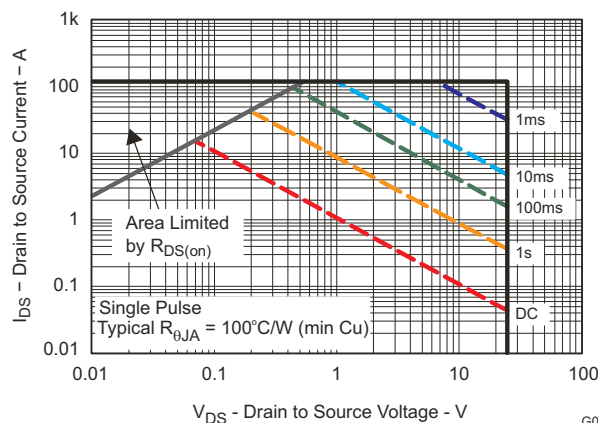


Figure 7-10. Maximum Safe Operating Area

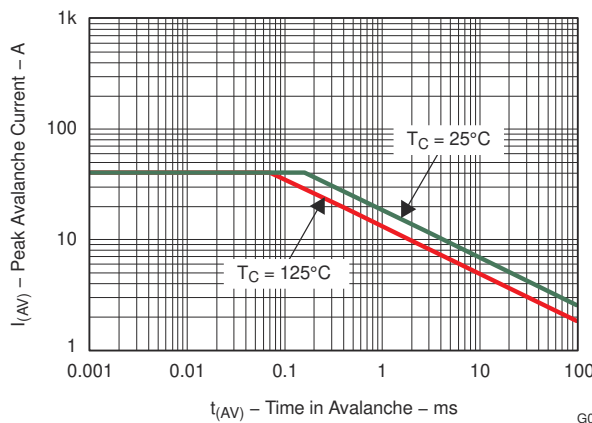


Figure 7-11. Single-Pulse Unclamped Inductive Switching

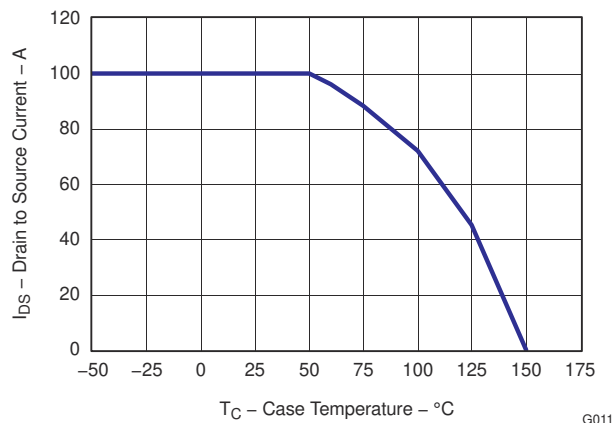


Figure 7-12. Maximum Drain Current vs. Temperature

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD16408Q5	Active	Production	VSON-CLIP (DQH) 8	2500 LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16408
CSD16408Q5.B	Active	Production	VSON-CLIP (DQH) 8	2500 LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16408

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



VSON-CLIP - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

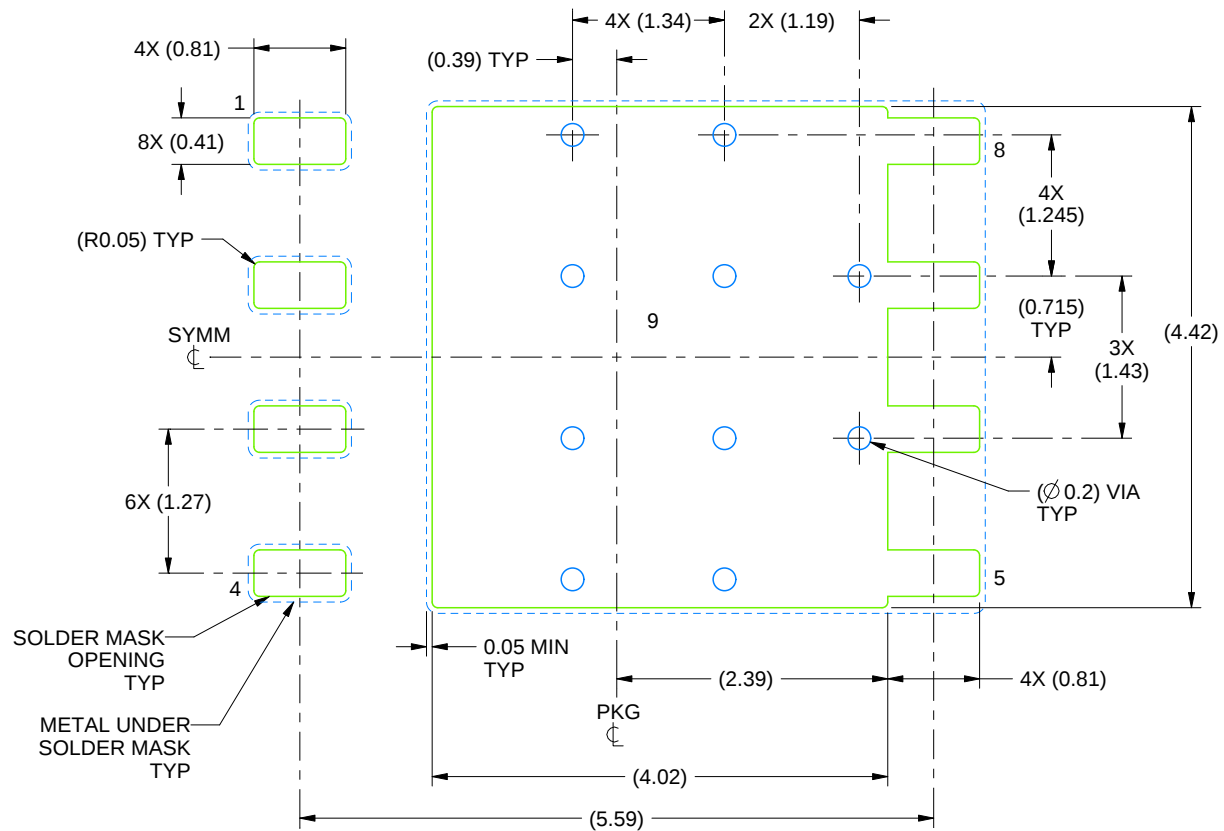


1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

DQH0008A

VSON-CLIP - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:15X

4223292/A 10/2016

NOTES: (continued)

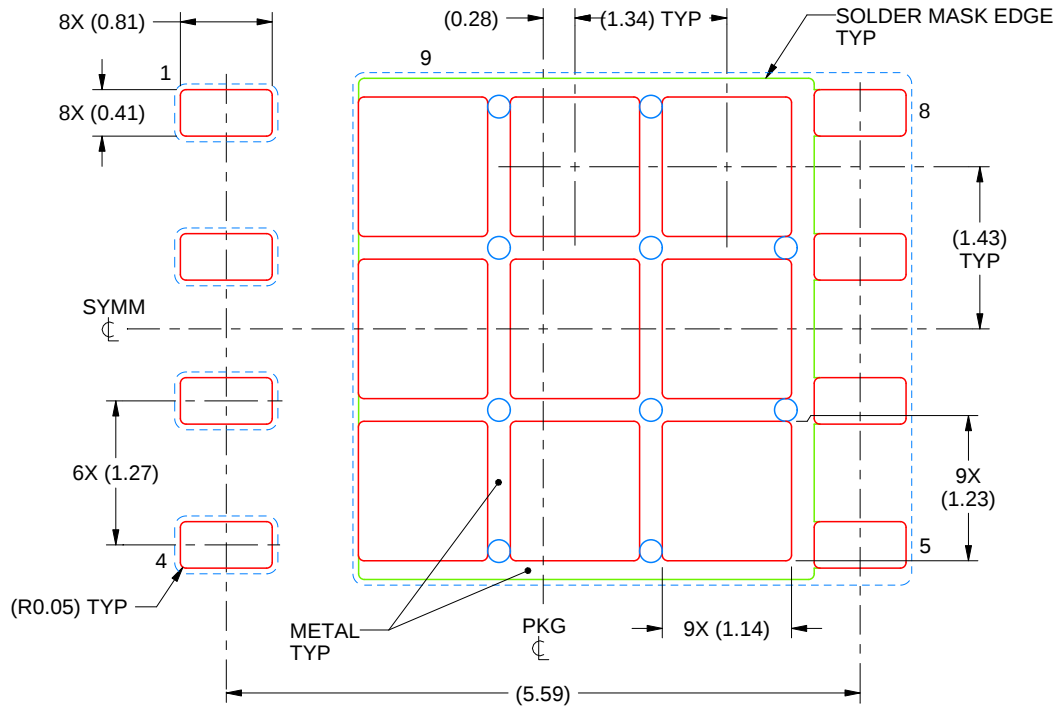
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DQH0008A

VSON-CLIP - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

4223292/A 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated