



CSD16406Q3 N-Channel NexFET™ Power MOSFET

1 Features

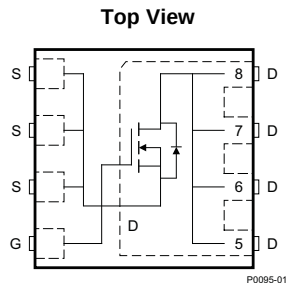
- Ultra-Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 3.3 mm × 3.3 mm Plastic Package

2 Applications

- Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom, and Computing Systems
- Optimized for Control or Synchronous FET Applications

3 Description

This 25 V, 4.2 mΩ, 3.3 mm × 3.3 mm SON NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.



Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	25		V
Q_g	Gate Charge Total (4.5 V)	5.8		nC
Q_{gd}	Gate Charge Gate to Drain	1.5		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 4.5\text{ V}$	5.9	mΩ
		$V_{GS} = 10\text{ V}$	4.2	mΩ
V_{th}	Threshold Voltage	1.8		V

Ordering Information⁽¹⁾

DEVICE	MEDIA	QTY	PACKAGE	SHIP
CSD16406Q3	13-Inch Reel	2500	SON 3.3 × 3.3 mm Plastic Package	Tape and Reel
CSD16406Q3T	13-Inch Reel	250		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

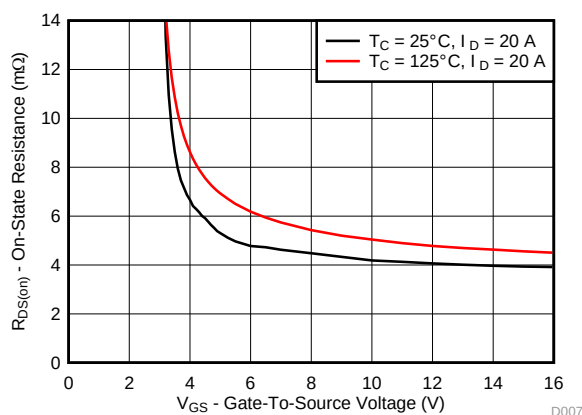
Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	25	V
V_{GS}	Gate-to-Source Voltage	+16 / -12	V
I_D	Continuous Drain Current (Package limited)	60	A
	Continuous Drain Current (Silicon limited), $T_C = 25^\circ\text{C}$	79	
	Continuous Drain Current ⁽¹⁾	19	
I_{DM}	Pulsed Drain Current ⁽²⁾	240	A
P_D	Power Dissipation ⁽¹⁾	2.8	W
	Power Dissipation, $T_C = 25^\circ\text{C}$	46	
T_J , T_{stg}	Operating Junction Temperature, Storage Temperature	-55 to 150	°C
E_{AS}	Avalanche Energy, single pulse $I_D = 45\text{ A}$, $L = 0.1\text{ mH}$, $R_G = 25\ \Omega$	101	mJ

(1) Typical $R_{\theta JA} = 45^\circ\text{C/W}$ on a 1 inch², 2 oz. Cu pad on a 0.06 inch thick FR4 PCB.

(2) Max $R_{\theta JC} = 2.7^\circ\text{C/W}$, pulse duration $\leq 100\ \mu\text{s}$, duty cycle $\leq 1\%$

$R_{DS(on)}$ vs V_{GS}



Gate Charge

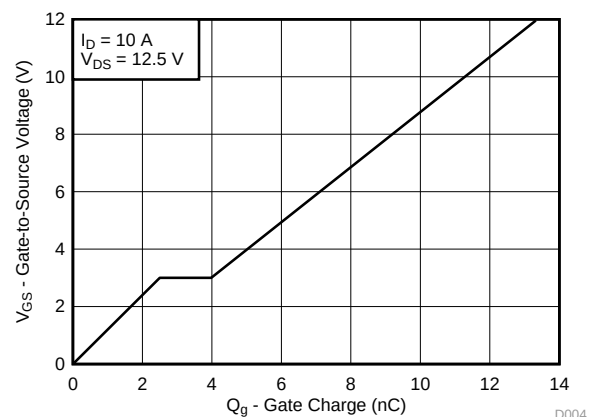


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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2010) to Revision B	Page
• Added part number to title	1
• Added Silicon Limited I_D , $T_C = 25^\circ\text{C}$	1
• Added Power Dissipation, $T_C = 25^\circ\text{C}$	1
• Updated Typical $R_{\theta JA}$	1
• Updated pulsed current conditions	1
• Added <i>Device and Documentation Support</i> section	7
• Updated <i>Mechanical, Packaging, and Orderable Information</i>	8

Changes from Original (August 2009) to Revision A	Page
• Deleted the Package Marking Information section.....	8

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-source voltage	V _{GS} = 0 V, I _D = 250 μA	25			V
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0 V, V _{DS} = 20 V			1	μA
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0 V, V _{GS} = +16/–12 V			100	nA
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	1.4	1.8	2.2	V
R _{DS(on)}	Drain-to-source on-resistance	V _{GS} = 4.5 V, I _D = 20 A	5.9		7.4	mΩ
		V _{GS} = 10 V, I _D = 20 A	4.2		5.3	mΩ
g _{fs}	Transconductance	V _{DS} = 15 V, I _D = 20 A	53			S
DYNAMIC CHARACTERISTICS						
C _{ISS}	Input capacitance	V _{GS} = 0 V, V _{DS} = 12.5 V, f = 1 MHz		840	1100	pF
C _{OSS}	Output capacitance			680	950	pF
C _{RSS}	Reverse transfer capacitance			57	80	pF
R _g	Series gate resistance			1.2	2.4	Ω
Q _g	Gate charge total (4.5 V)	V _{DS} = 12.5 V, I _D = 20 A		5.8	8.1	nC
Q _{gd}	Gate charge gate to drain			1.5		nC
Q _{gs}	Gate charge gate to source			2.5		nC
Q _{g(th)}	Gate charge at V _{th}			1.5		nC
Q _{OSS}	Output charge	V _{DS} = 13.6 V, V _{GS} = 0 V		13.9		nC
t _{d(on)}	Turn on delay time	V _{DS} = 12.5 V, V _{GS} = 4.5 V I _D = 20 A R _G = 2 Ω		7.3		ns
t _r	Rise time			12.9		ns
t _{d(off)}	Turn off delay time			8.5		ns
t _f	Fall time			4.8		ns
DIODE CHARACTERISTICS						
V _{SD}	Diode forward voltage	I _S = 20 A, V _{GS} = 0 V		0.85	1.0	V
Q _{rr}	Reverse recovery charge	V _{DD} = 13.6 V, I _F = 20 A, di/dt = 300 A/μs		18		nC
t _{rr}	Reverse recovery time	V _{DD} = 13.6 V, I _F = 20 A, di/dt = 300 A/μs		22		ns

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

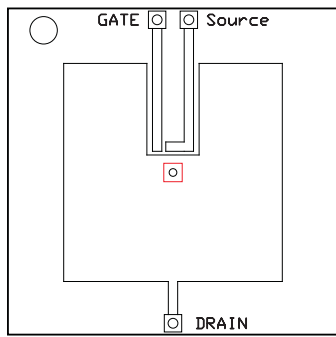
THERMAL METRIC		MIN	TYP	MAX	UNIT
R _{θJC}	Junction-to-case thermal resistance ⁽¹⁾			2.7	°C/W
R _{θJA}	Junction-to-ambient thermal resistance ⁽¹⁾⁽²⁾			55	°C/W

- (1) R_{θJC} is determined with the device mounted on a 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inch × 1.5 inch (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 PCB. R_{θJC} is specified by design, whereas R_{θJA} is determined by the user's board design.
- (2) Device mounted on FR4 material with 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu.

CSD16406Q3

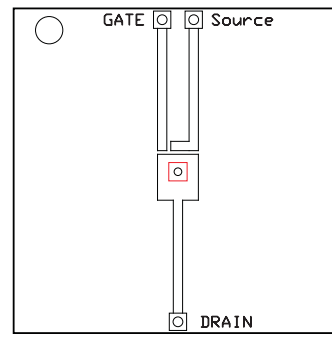
SLPS202B – AUGUST 2009 – REVISED DECEMBER 2015

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M0161-01

Max $R_{\theta JA} = 55^{\circ}\text{C/W}$
when mounted on 1
 inch^2 of 2 oz. Cu.

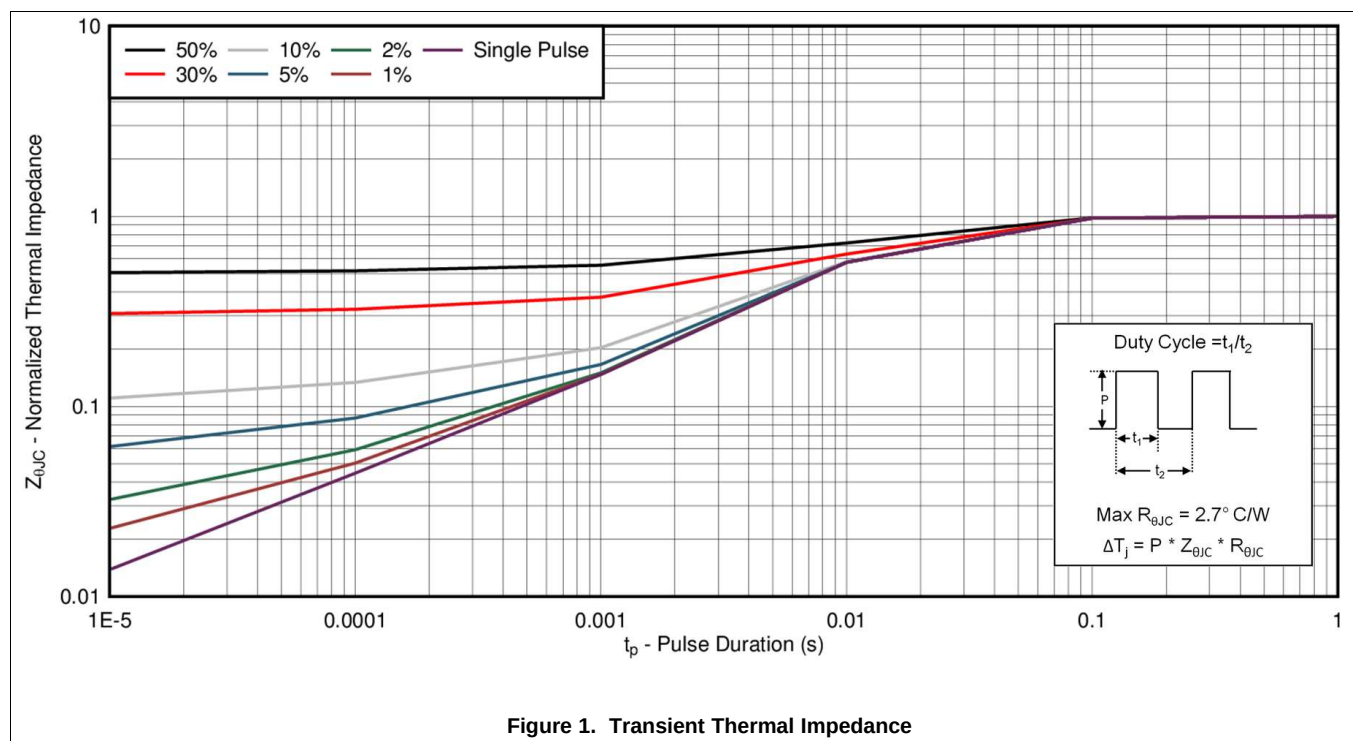


M0161-02

Max $R_{\theta JA} = 160^{\circ}\text{C/W}$
when mounted on
minimum pad area of 2
oz. Cu.

5.3 Typical MOSFET Characteristics

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)



Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

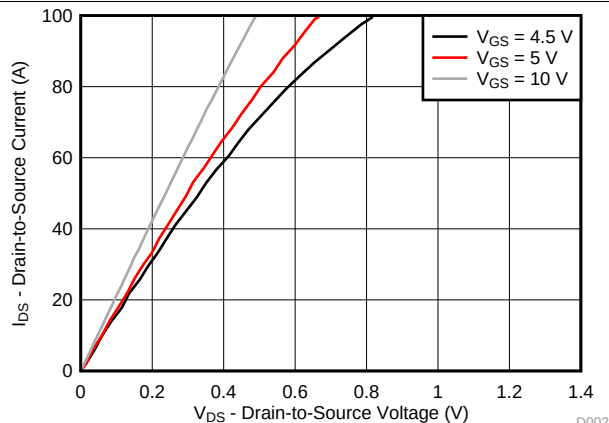


Figure 2. Saturation Characteristics

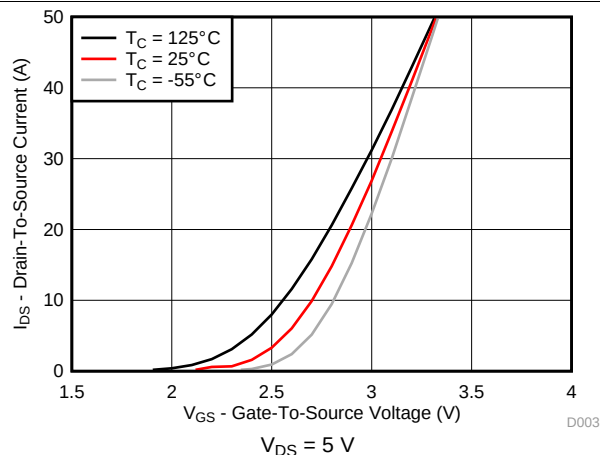


Figure 3. Transfer Characteristics

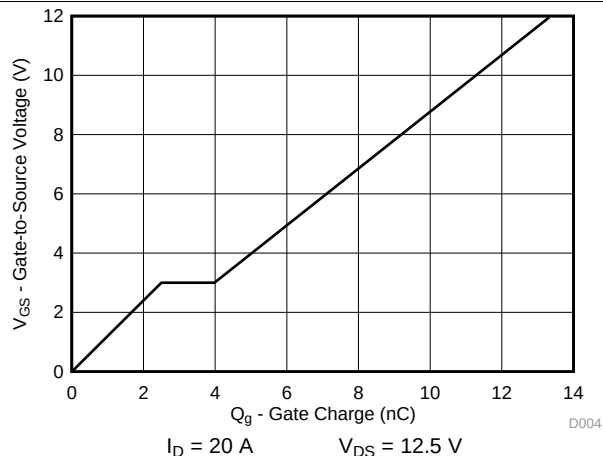


Figure 4. Gate Charge

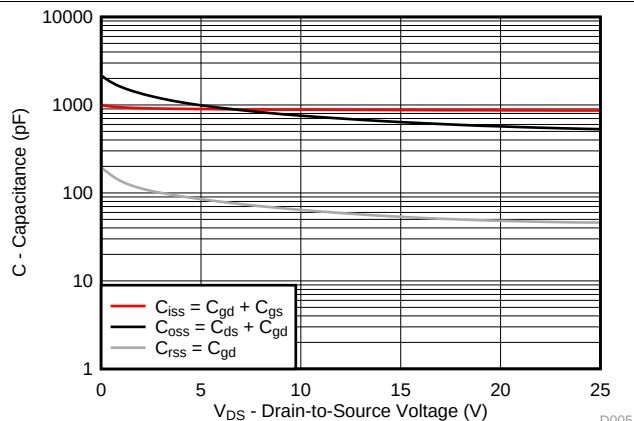


Figure 5. Capacitance

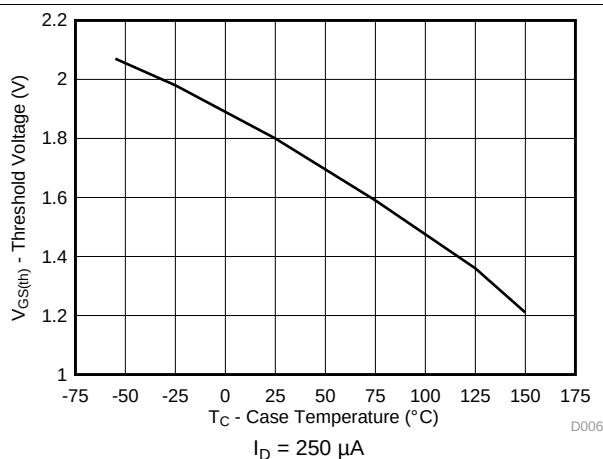


Figure 6. Threshold Voltage vs Temperature

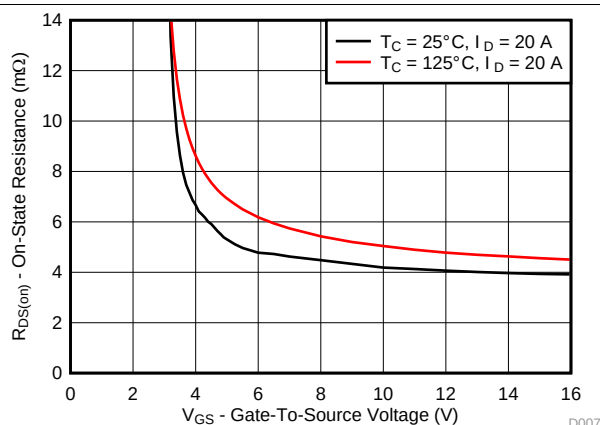


Figure 7. On Resistance vs Gate Voltage

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

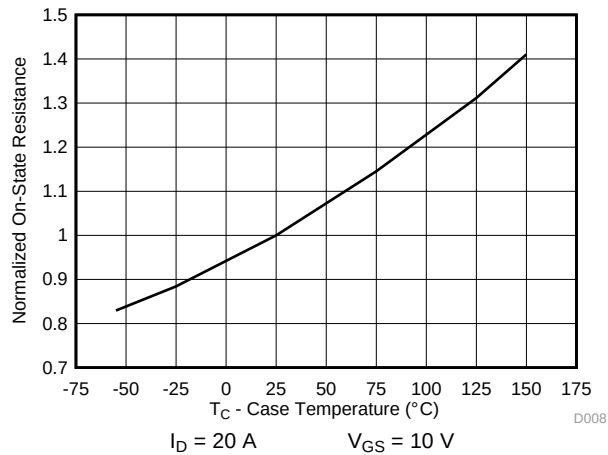


Figure 8. Normalized On-Resistance vs Temperature

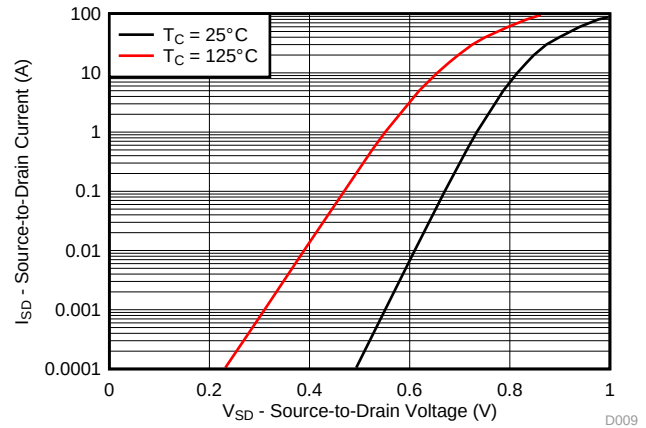


Figure 9. Typical Diode Forward Voltage

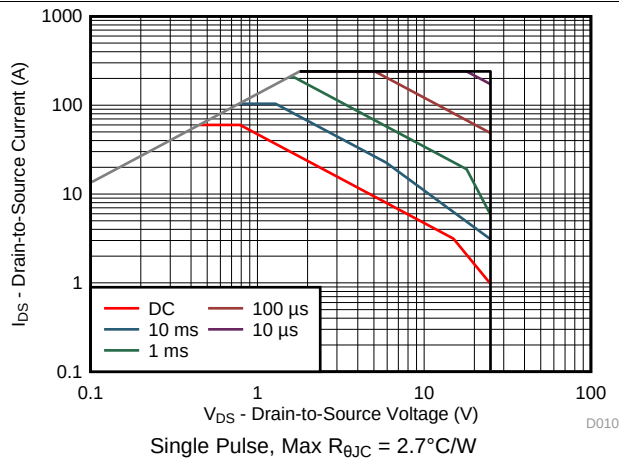


Figure 10. Maximum Safe Operating Area

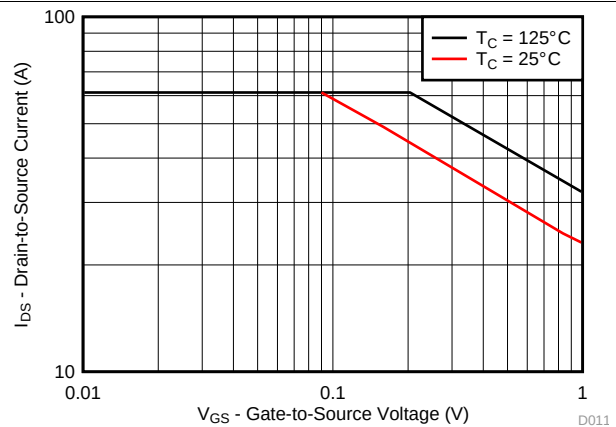


Figure 11. Single Pulse Unclamped Inductive Switching

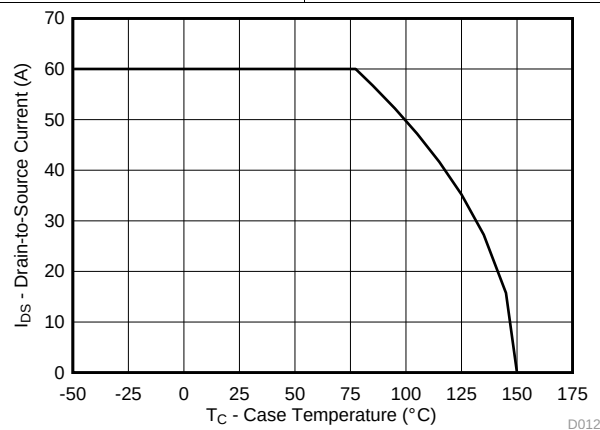


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.2 Trademarks

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.4 Glossary

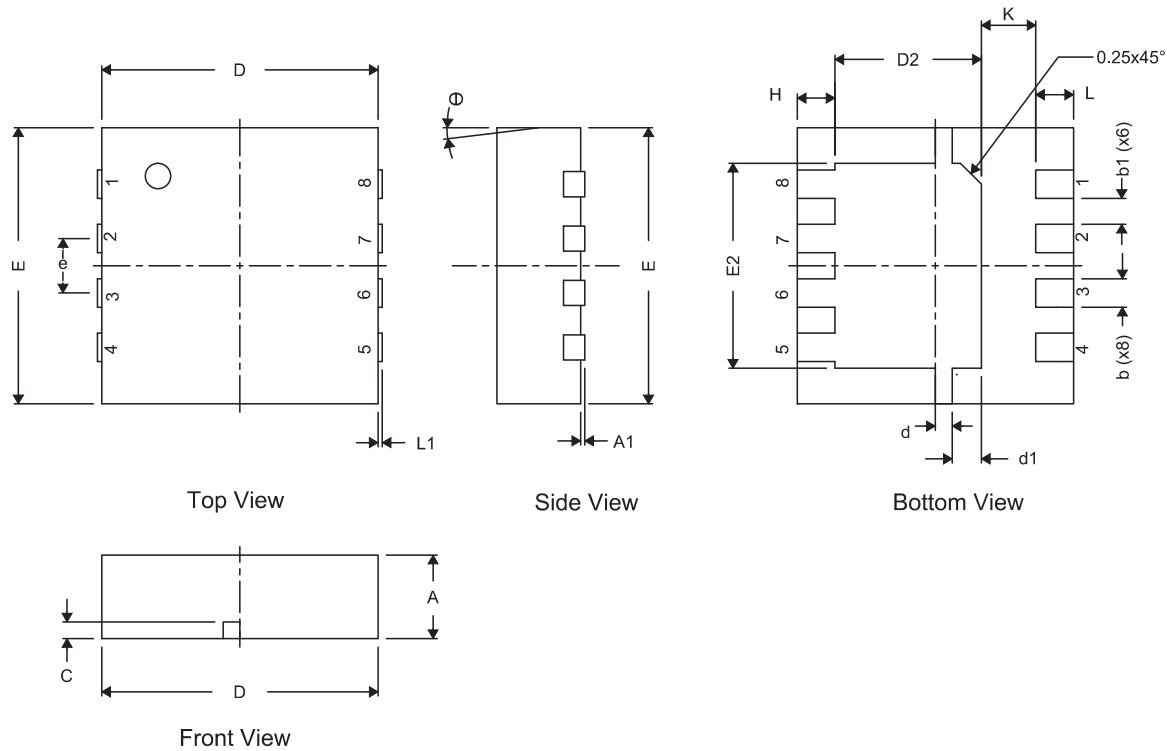
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

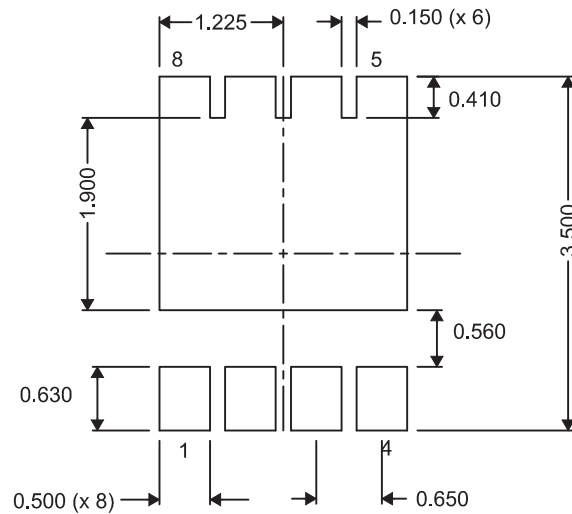
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Q3 Package Dimensions



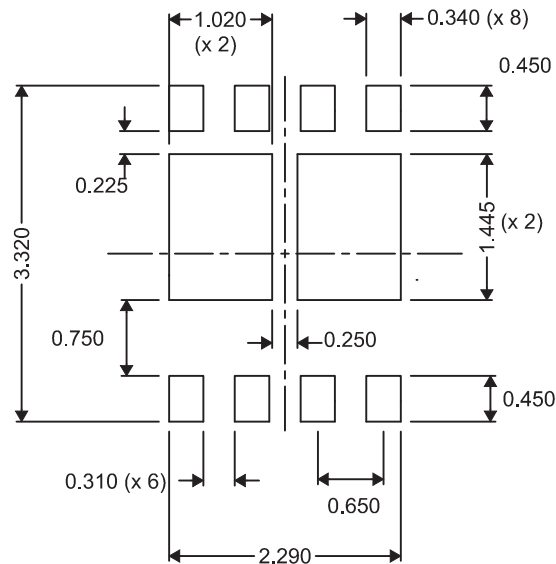
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
b1	0.310 NOM			0.012 NOM		
c	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D2	1.650	1.750	1.800	0.065	0.069	0.071
d	0.150	0.200	0.250	0.006	0.008	0.010
d1	0.300	0.350	0.400	0.012	0.014	0.016
E	3.200	3.300	3.400	0.126	0.130	0.134
E2	2.350	2.450	2.550	0.093	0.096	0.100
e	0.650 TYP			0.026 TYP		
H	0.35	0.450	0.550	0.014	0.018	0.022
K	0.650 TYP			0.026 TYP		
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	0	—	0	0	—	0
θ	0	—	0	0	—	0

7.2 Recommended PCB Pattern



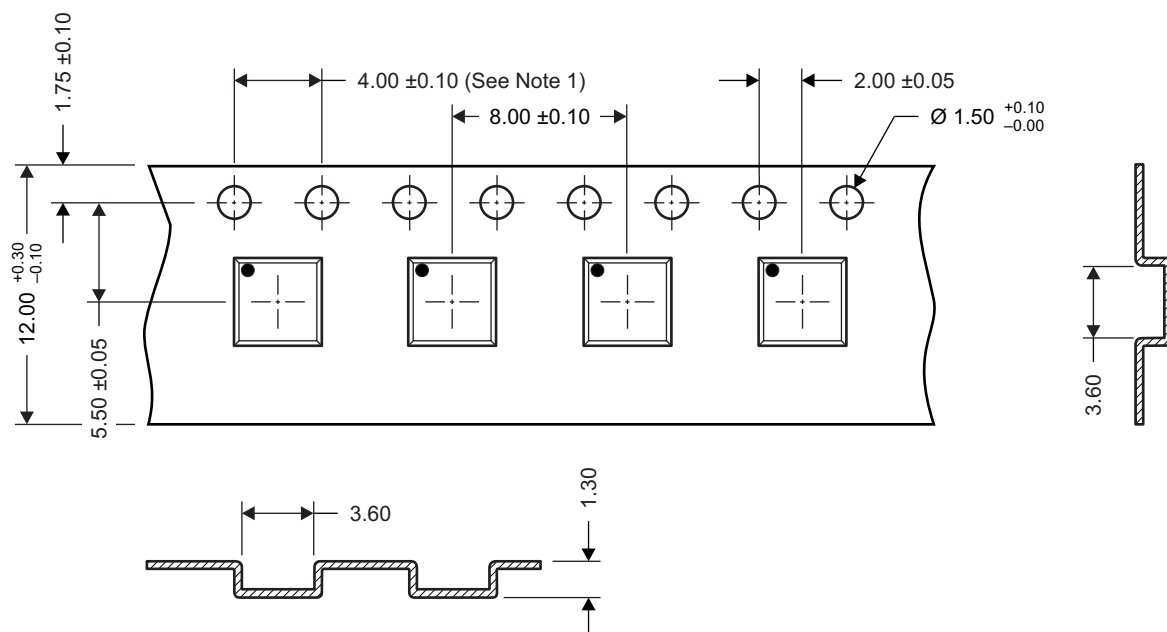
For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

7.3 Recommended Stencil Opening



All dimensions are in mm, unless otherwise specified.

7.4 Q3 Tape and Reel Information



M0144-01

Notes:

1. 10 sprocket hole pitch cumulative tolerance ± 0.2
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
3. Material: black static dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified).
5. Thickness: 0.30 ± 0.05 mm
6. MSL1 260°C (IR and Convection) PbF-Reflow Compatible

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD16406Q3	Active	Production	VSON-CLIP (DQG) 8	2500 LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16406
CSD16406Q3.B	Active	Production	VSON-CLIP (DQG) 8	2500 LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16406

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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