

CSD16342Q5A 25V N-Channel NexFET™ Power MOSFET

1 Features

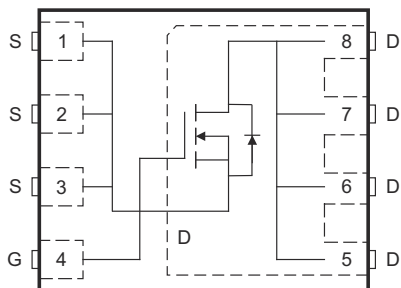
- Optimized for 5V gate drive
- Resistance rated at $V_{GS} = 2.5V$
- Ultra low Q_g and Q_{gd}
- Low thermal resistance
- Avalanche rated
- Pb free terminal plating
- RoHS compliant
- Halogen free
- SON 5mm x 6mm plastic package

2 Applications

- Point-of-load synchronous buck converter for applications in networking, telecom and computing systems
- Optimized for control or synchronous FET applications

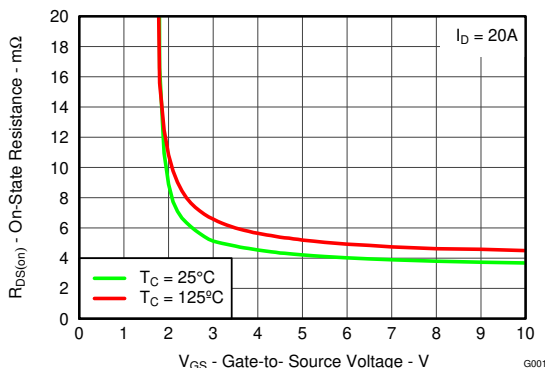
3 Description

The NexFET™ power MOSFET has been designed to minimize losses in power conversion and optimized for 5V gate drive applications.

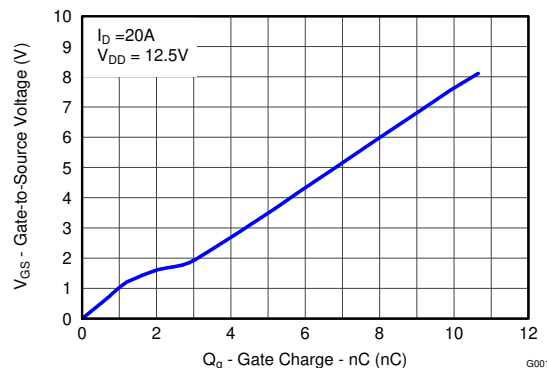


P0095-01

Top View



$R_{DS(ON)}$ vs V_{GS}



Gate Charge

Product Summary

V_{DS}	Drain to Source Voltage	25	V
Q_g	Gate Charge Total (4.5V)	6.8	nC
Q_{gd}	Gate Charge Gate to Drain	1.2	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 2.5V$	6.1 mΩ
		$V_{GS} = 4.5V$	4.3 mΩ
		$V_{GS} = 8V$	3.8 mΩ
V_{th}	Threshold Voltage	0.85	V

Ordering Information

Device	Package	Media	Qty	Ship
CSD16342Q5A	SON 5 × 6 Plastic Package	13-inch reel	2500	Tape and Reel

Absolute Maximum Ratings

$T_A = 25^\circ C$ unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	25	V
V_{GS}	Gate to Source Voltage	+10 / -8	V
I_D	Continuous Drain Current, $T_C = 25^\circ C$	100	A
	Continuous Drain Current ⁽¹⁾	21	A
I_{DM}	Pulsed Drain Current, $T_A = 25^\circ C$ ⁽²⁾	131	A
P_D	Power Dissipation ⁽¹⁾	3	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ C$
E_{AS}	Avalanche Energy, single pulse $I_D = 40A, L = 0.1mH, R_G = 25\Omega$	80	mJ

- (1) Typical $R_{\theta JA} = 40^\circ C/W$ on 1in² Cu (2 oz.) on 0.060" thick FR4 PCB.
 (2) Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$



4 Specifications

4.1 Electrical Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)

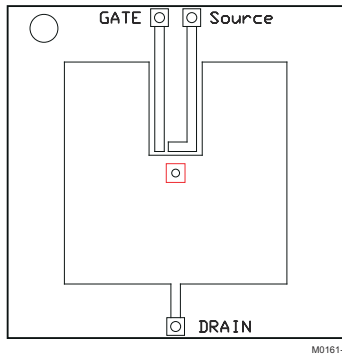
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Static Characteristics							
BV _{DSS}	Drain to Source Voltage	V _{GS} = 0V, I _{DS} = 250μA	25			V	
I _{DSS}	Drain to Source Leakage Current	V _{GS} = 0V, V _{DS} = 20V			1	μA	
I _{GSS}	Gate to Source Leakage Current	V _{DS} = 0V, V _{GS} = +10/-8V			100	nA	
V _{GS(th)}	Gate to Source Threshold Voltage	V _{DS} = V _{GS} , I _{DS} = 250μA	0.6	0.85	1.1	V	
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 2.5V, I _{DS} = 20A			6.1	7.8	mΩ
		V _{GS} = 4.5V, I _{DS} = 20A			4.3	5.5	mΩ
		V _{GS} = 8V, I _{DS} = 20A			3.8	4.7	mΩ
g _{fs}	Transconductance	V _{DS} = 15V, I _{DS} = 20A			91	S	
Dynamic Characteristics							
C _{ISS}	Input Capacitance	V _{GS} = 0V, V _{DS} = 12.5V, f = 1MHz		1050	1350	pF	
C _{OSS}	Output Capacitance			730	950	pF	
C _{RSS}	Reverse Transfer Capacitance			53	69	pF	
R _g	Series Gate Resistance			1.5	3	Ω	
Q _g	Gate Charge Total (4.5V)	V _{DS} = 12.5V, I _D = 20A		6.8	7.1	nC	
Q _{gd}	Gate Charge Gate to Drain			0.9		nC	
Q _{gs}	Gate Charge Gate to Source			1.9		nC	
Q _{g(th)}	Gate Charge at V _{th}			1.2		nC	
Q _{OSS}	Output Charge	V _{DS} = 13V, V _{GS} = 0V		13.7		nC	
t _{d(on)}	Turn On Delay Time	V _{DS} = 12.5V, V _{GS} = 4.5V, I _D = 20A , R _G = 2Ω		5.2		ns	
t _r	Rise Time			16.6		ns	
t _{d(off)}	Turn Off Delay Time			13.4		ns	
t _f	Fall Time			3.1		ns	
Diode Characteristics							
V _{SD}	Diode Forward Voltage	I _S = 20A, V _{GS} = 0V		0.8	1	V	
Q _{rr}	Reverse Recovery Charge	V _{DD} = 13V, I _F = 20A, di/dt = 300A/μs		14.5		nC	
t _{rr}	Reverse Recovery Time			20		ns	

4.2 Thermal Characteristics

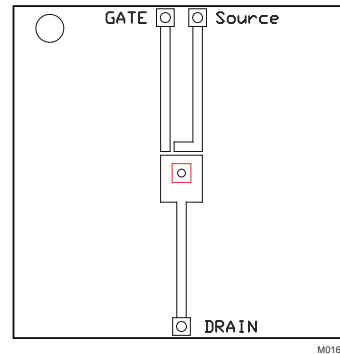
($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER	MIN	TYP	MAX	UNIT
$R_{\theta JC}$ Thermal Resistance Junction to Case ⁽¹⁾			1.2	$^\circ\text{C/W}$
$R_{\theta JA}$ Thermal Resistance Junction to Ambient ^{(1) (2)}			50	$^\circ\text{C/W}$

- (1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch² (6.45cm²), 2oz. (0.071mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81cm × 3.81cm), 0.06-inch (1.52mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch² (6.45cm²), 2oz. (0.071mm thick) Cu.



Max $R_{\theta JA} = 50^\circ\text{C/W}$ when mounted on 1 inch² of 2oz. Cu.



Max $R_{\theta JA} = 123^\circ\text{C/W}$ when mounted on minimum pad area of 2oz. Cu.

5 Typical MOSFET Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)

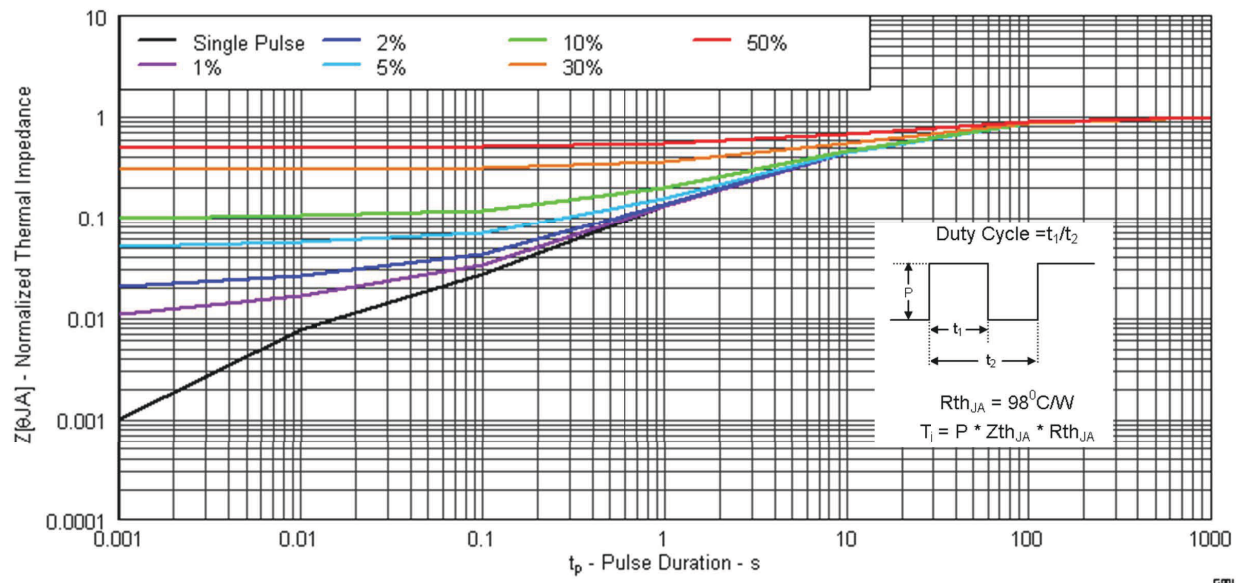


Figure 5-1. Transient Thermal Impedance

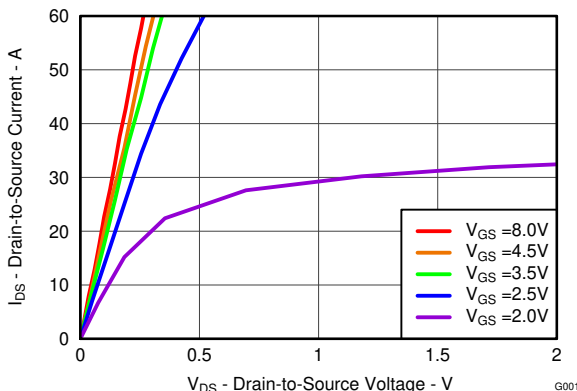


Figure 5-2. Saturation Characteristics

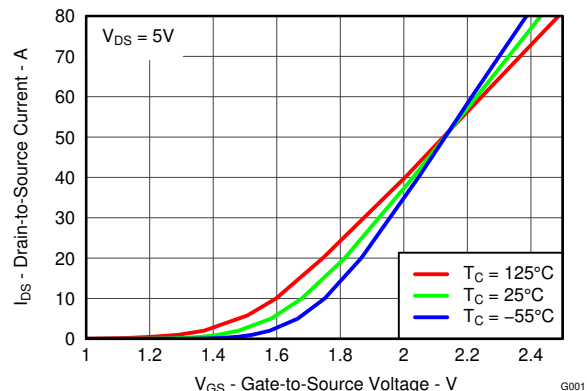


Figure 5-3. Transfer Characteristics

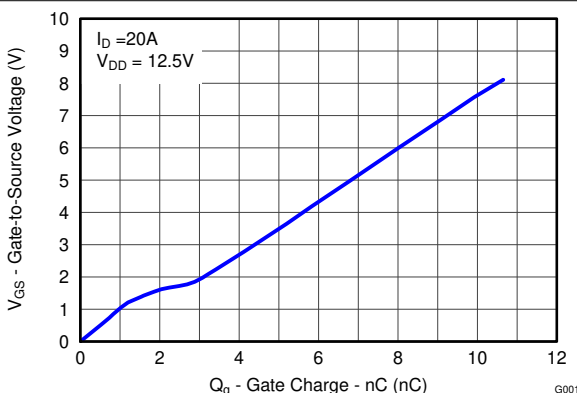


Figure 5-4. Gate Charge

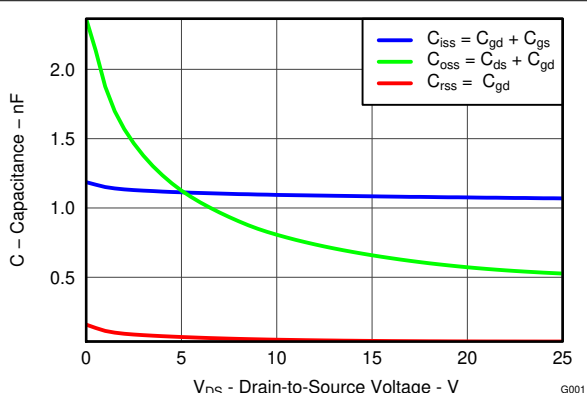


Figure 5-5. Capacitance

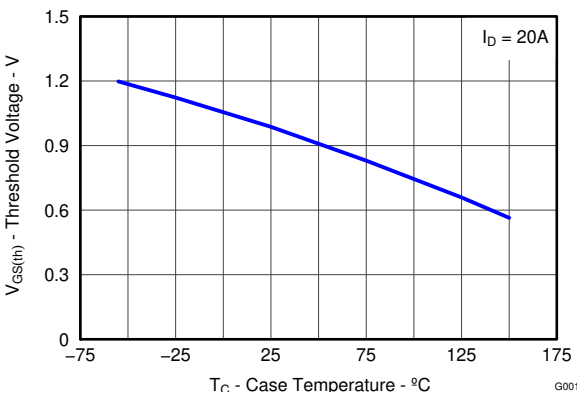


Figure 5-6. Threshold Voltage vs. Temperature

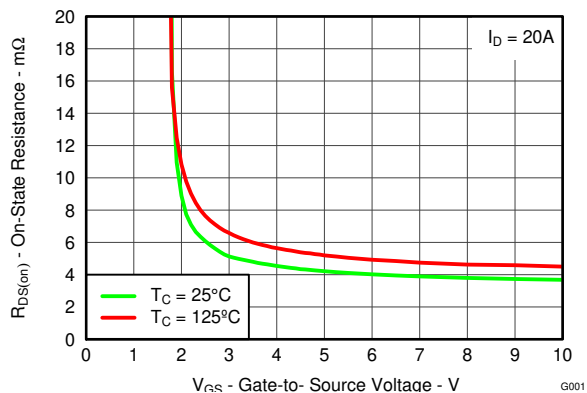


Figure 5-7. On Resistance vs. Gate Voltage

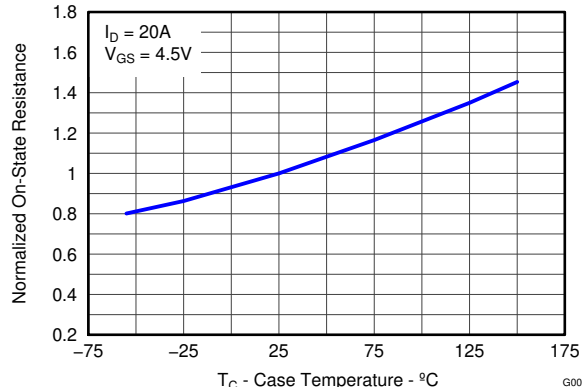


Figure 5-8. Normalized On Resistance vs. Temperature

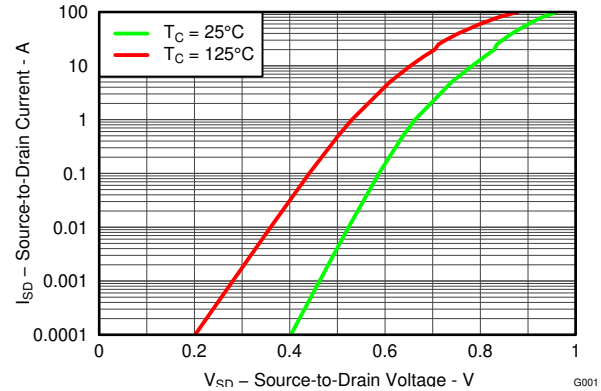


Figure 5-9. Typical Diode Forward Voltage

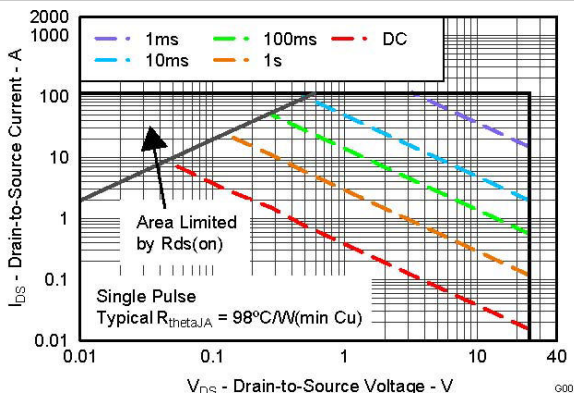


Figure 5-10. Maximum Safe Operating Area

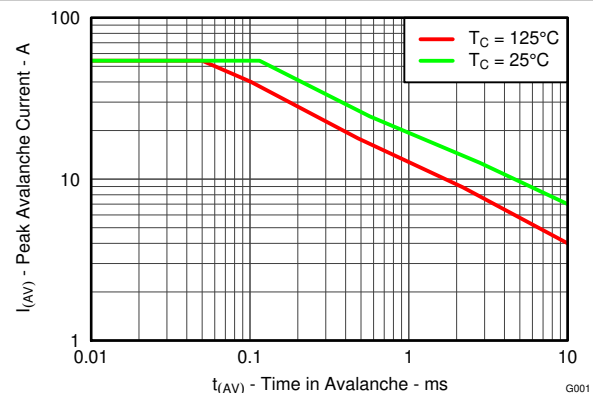


Figure 5-11. Single Pulse Unclamped Inductive Switching

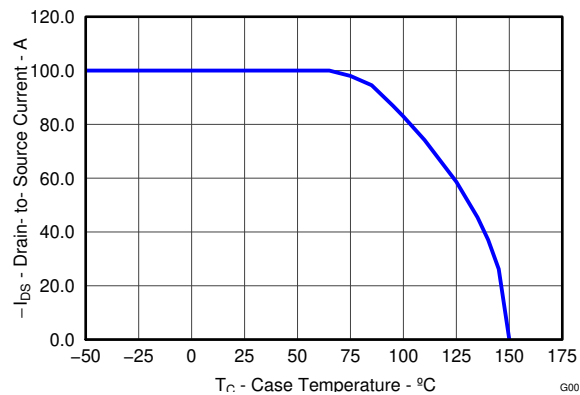


Figure 5-12. Maximum Drain Current vs. Temperature

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (January 2025) to Revision C (May 2025)	Page
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- | | |
|---|---|
| • Updated the document title from CSD16342Q5A 40V N-Channel NexFET™ Power MOSFET to CSD16342Q5A 25V N-Channel NexFET™ Power MOSFET..... | 1 |
|---|---|

Changes from Revision A (March 2012) to Revision B (January 2025)	Page
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- | | |
|---|---|
| • Updated the numbering format for tables, figures, and cross-references throughout the document..... | 1 |
|---|---|

Changes from Revision * (February 2012) to Revision A (March 2012)	Page
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- | | |
|---|---|
| • Changed the device status from: Product Preview to Production Data..... | 1 |
|---|---|

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD16342Q5A	Active	Production	VSONP (DQJ) 8	2500 LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16342
CSD16342Q5A.B	Active	Production	VSONP (DQJ) 8	2500 LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16342

- ⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).
- ⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- ⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- ⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- ⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- ⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

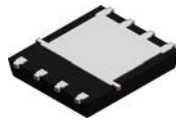
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD16342Q5A	VSONP	DQJ	8	2500	330.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

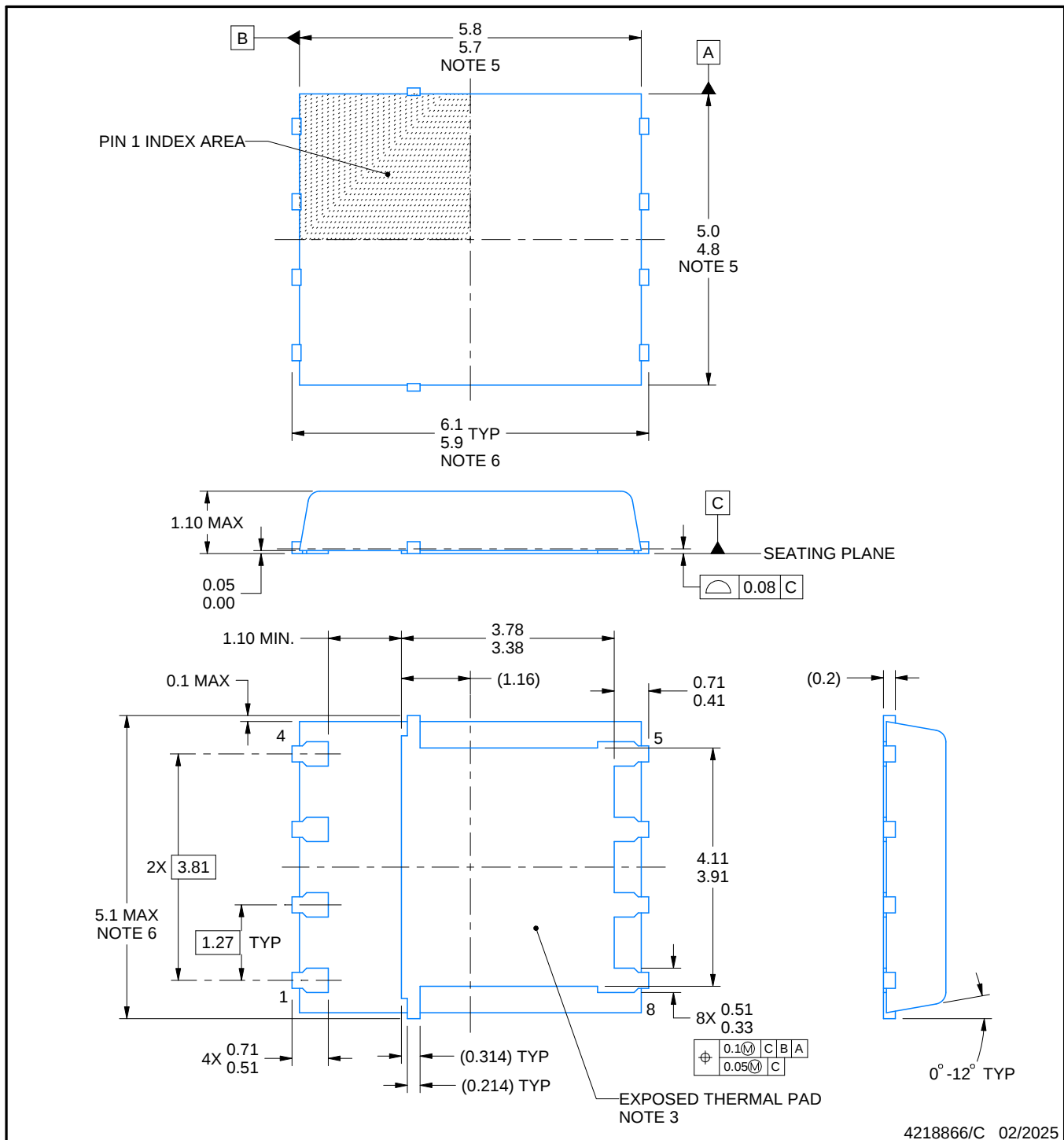


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD16342Q5A	VSONP	DQJ	8	2500	340.0	340.0	38.0

DQJ0008A**PACKAGE OUTLINE****VSONP - 1.1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



4218866/C 02/2025

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Metalized features are supplier options and may not be on the package.
5. These dimensions do not include mold flash protrusions or gate burrs.
6. These dimensions include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25 mm per side.

PLASTIC SMALL OUTLINE - NO LEAD

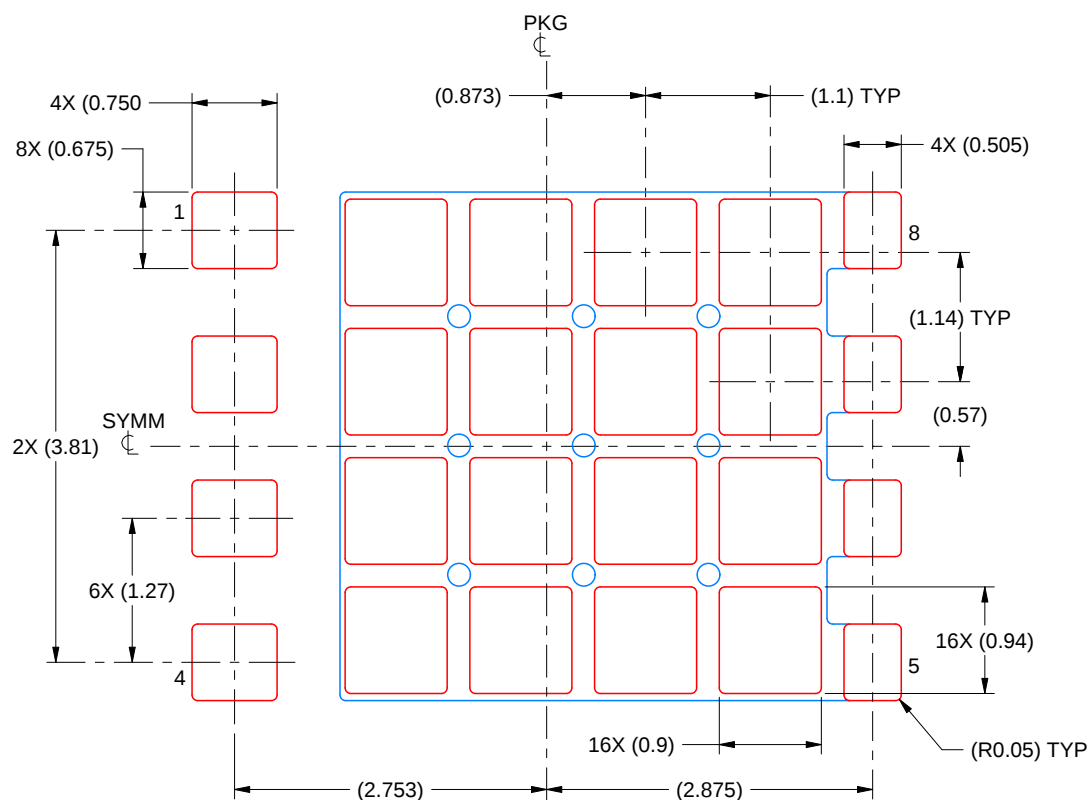
LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE: 15X

SOLDER MASK DETAILS

DQJ0008A

VSONP - 1.1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD:
70% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 15X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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