

CSD13383F4 12 V N-Channel FemtoFET™ MOSFET

1 Features

- Low on-resistance
- Ultra low Q_g and Q_{gd}
- Ultra-small footprint (0402 case size)
 - 1.0 mm × 0.6 mm
- Low profile
 - 0.36 mm height
- Integrated ESD protection diode
 - Rated >2 kV HBM
 - Rated >2 kV CDM
- Lead and halogen free
- RoHS compliant

2 Applications

- Optimized for load switch applications
- Optimized for general purpose Switching Applications
- Single-cell battery applications
- Handheld and mobile applications

3 Description

This 37 mΩ, 12 V N-channel FemtoFET™ MOSFET technology is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing at least a 60% reduction in footprint size.

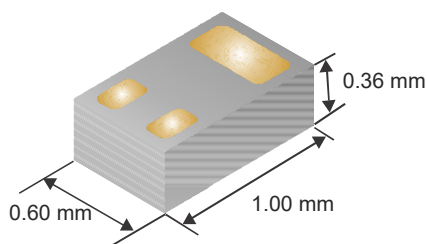


Figure 3-1. Typical Part Dimensions

Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	12	V
Q_g	Gate Charge Total (4.5 V)	2.0	nC
Q_{gd}	Gate Charge Gate-to-Drain	0.6	nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 2.5\text{ V}$	53
		$V_{GS} = 4.5\text{ V}$	37
$V_{GS(th)}$	Threshold Voltage	1.0	V

Ordering Information

DEVICE ⁽¹⁾	QTY	MEDIA	PACKAGE	SHIP
CSD13383F4	3000	7-Inch Reel	Femto (0402) 1.0 mm × 0.6 mm SMD Lead Less	Tape and Reel
CSD13383F4T	250			

- (1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	12	V
V_{GS}	Gate-to-Source Voltage	±10	V
I_D	Continuous Drain Current ⁽¹⁾	2.9	A
I_{DM}	Pulsed Drain Current ^{(1) (2)}	18.5	A
I_G	Continuous Gate Clamp Current	25	mA
	Pulsed Gate Clamp Current ^{(1) (2)}	250	
P_D	Power Dissipation	500	mW
ESD Rating	Human Body Model (HBM)	2	kV
	Charged Device Model (CDM)	2	kV
T_J, T_{stg}	Operating Junction Temperature Storage Temperature	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse $I_D = 6.7$, $L = 0.1\text{ mH}$, $R_G = 25\ \Omega$	2.2	mJ

- (1) Typical $R_{\theta JA} = 250^\circ\text{C/W}$.
 (2) Pulse duration ≤ 100 μs, duty cycle ≤ 1%.

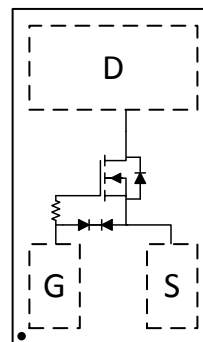


Figure 3-2. Top View



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (December 2017) to Revision C (February 2022)	Page
• Changed ultra-low profile bullet from 0.35 mm to 0.36 mm in height.....	1
• Updated ultra-low profile image height from 0.35 mm to 0.36 mm.....	1
• Changed ultra-low profile image height from 0.35 mm to 0.36 mm.....	8
• Added FemtoFET Surface Mount Guide note.....	9

Changes from Revision A (January 2016) to Revision B (December 2017)	Page
• Changed I_{DM} value From: 27 A To: 18.5 A in the <i>Absolute Maximum Ratings</i> table.....	1
• Updated Figure 5-1	3
• Updated Figure 5-10 using Typ $R_{\theta JA} = 250^{\circ}\text{C/W}$	3
• Updated all mechanical drawings, increased the size of the pads in the Section 7.3 section.	8

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
STATIC CHARACTERISTICS							
BV _{DSS}	Drain-to-source voltage	V _{GS} = 0 V, I _{DS} = 250 μA	12			V	
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0 V, V _{DS} = 9.6 V	1			μA	
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0 V, V _{GS} = 10 V	10			μA	
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _{DS} = 250 μA	0.70	1.00	1.25	V	
R _{DS(on)}	Drain-to-source on-resistance	V _{GS} = 2.5 V, I _{DS} = 0.5 A	53			65	mΩ
		V _{GS} = 4.5 V, I _{DS} = 0.5 A	37			44	mΩ
g _{fs}	Transconductance	V _{DS} = 6 V, I _{DS} = 0.5 A	5.4			S	
DYNAMIC CHARACTERISTICS							
C _{iss}	Input capacitance	V _{GS} = 0 V, V _{DS} = 6 V, f = 1 MHz	224			291	pF
C _{oss}	Output capacitance		68			88	pF
C _{rss}	Reverse transfer capacitance		47			61	pF
R _G	Series gate resistance		240			Ω	
Q _g	Gate charge total (4.5 V)	V _{DS} = 6 V, I _{DS} = 0.5 A	2.0			2.6	nC
Q _{gd}	Gate charge gate-to-drain		0.6				nC
Q _{gs}	Gate charge gate-to-source		0.4				nC
Q _{g(th)}	Gate charge at V _{th}		0.1				nC
Q _{oss}	Output charge	V _{DS} = 6 V, V _{GS} = 0 V	0.9			nC	
t _{d(on)}	Turn on delay time	V _{DS} = 6 V, V _{GS} = 4.5 V, I _{DS} = 0.5 A, R _G = 2 Ω	46			ns	
t _r	Rise time		122			ns	
t _{d(off)}	Turn off delay time		250			ns	
t _f	Fall time		290			ns	
DIODE CHARACTERISTICS							
V _{SD}	Diode forward voltage	I _{SD} = 0.5 A, V _{GS} = 0 V	0.7			1.0	V

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
R _{θJA}	Junction-to-ambient thermal resistance ⁽¹⁾		90		°C/W
	Junction-to-ambient thermal resistance ⁽²⁾		250		

(1) Device mounted on FR4 material with 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu.

(2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

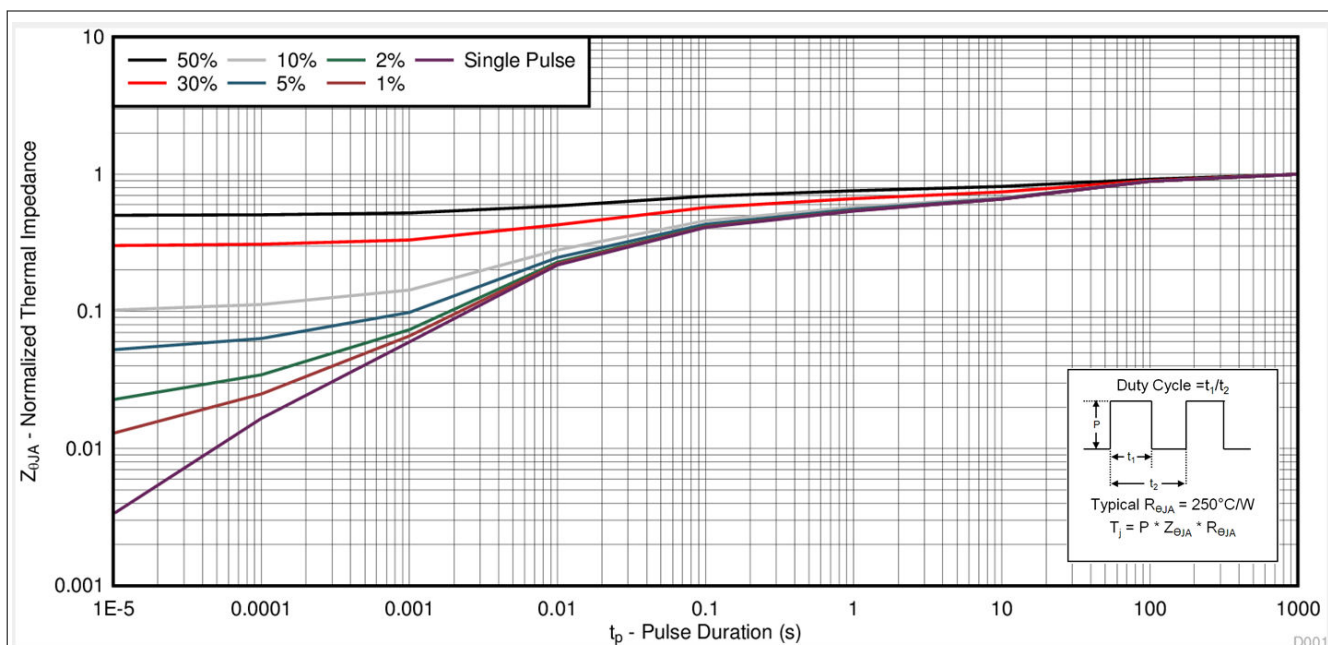


Figure 5-1. Transient Thermal Impedance

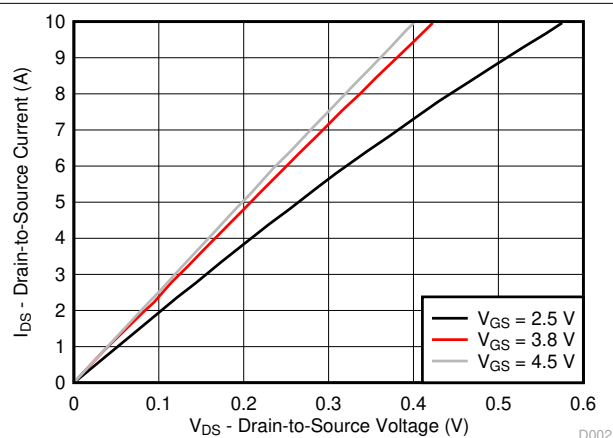


Figure 5-2. Saturation Characteristics

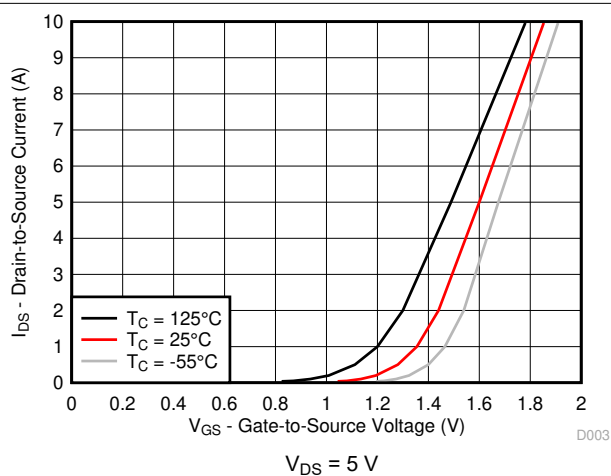


Figure 5-3. Transfer Characteristics

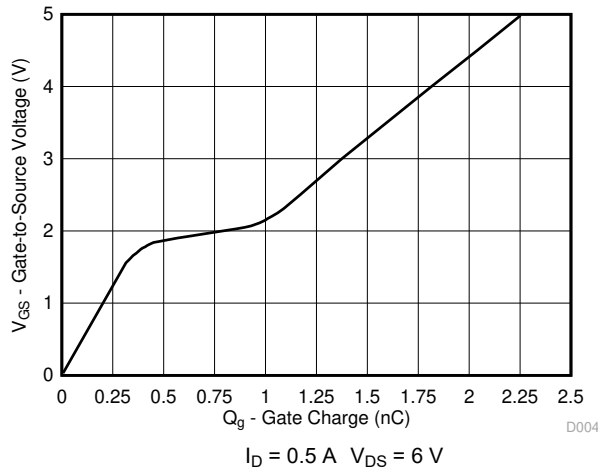


Figure 5-4. Gate Charge

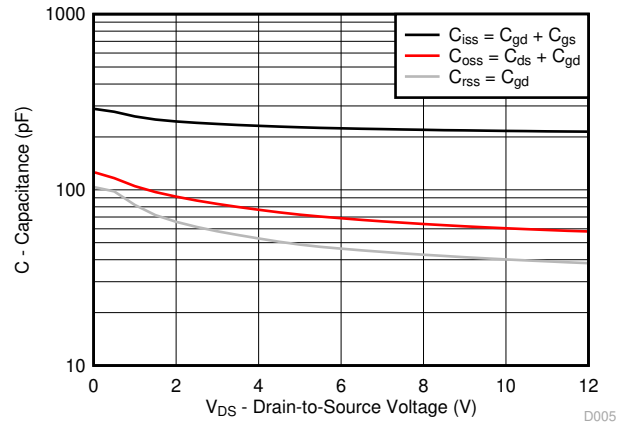


Figure 5-5. Capacitance

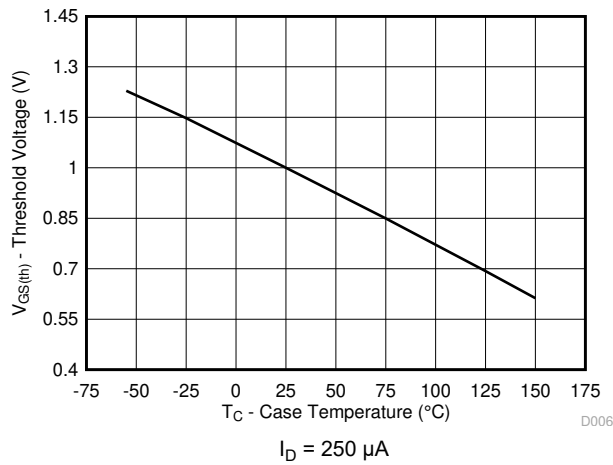


Figure 5-6. Threshold Voltage vs Temperature

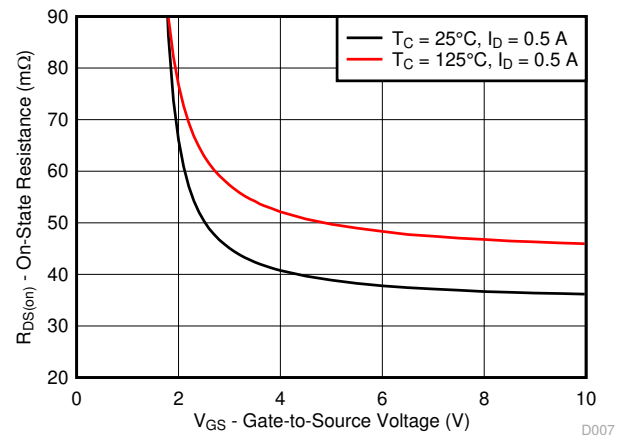


Figure 5-7. On-State Resistance vs Gate-to-Source Voltage

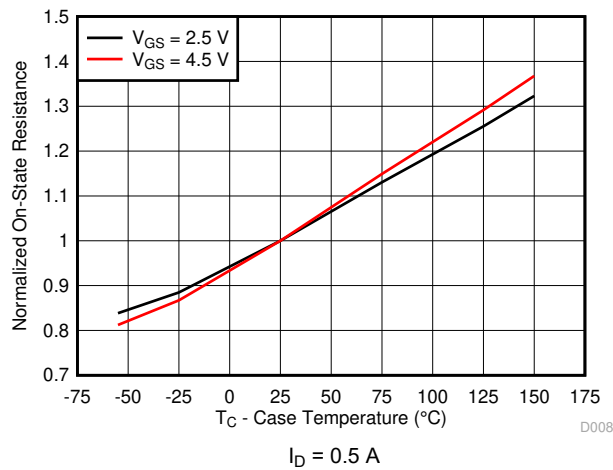


Figure 5-8. Normalized On-State Resistance vs Temperature

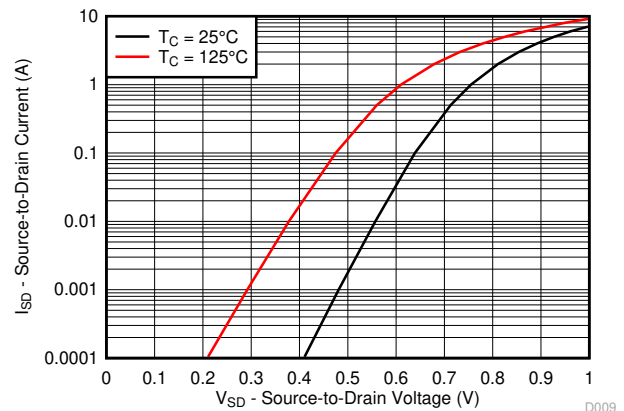


Figure 5-9. Typical Diode Forward Voltage

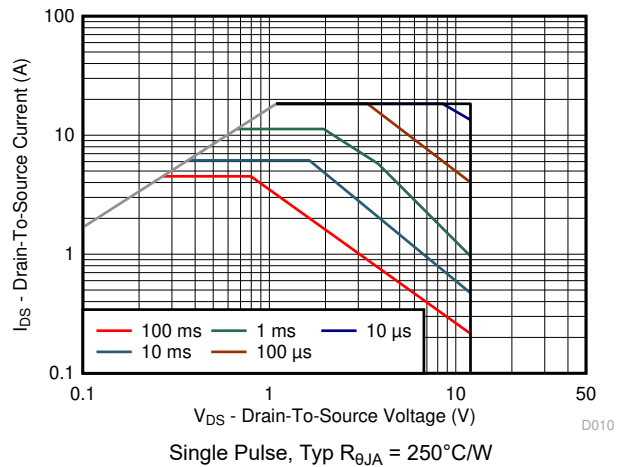


Figure 5-10. Maximum Safe Operating Area (SOA)

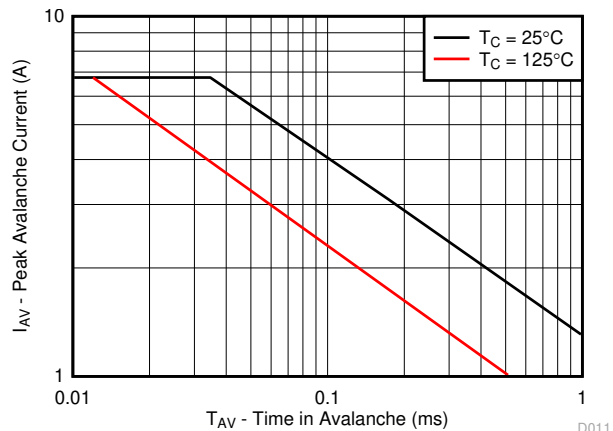


Figure 5-11. Single Pulse Unclamped Inductive Switching

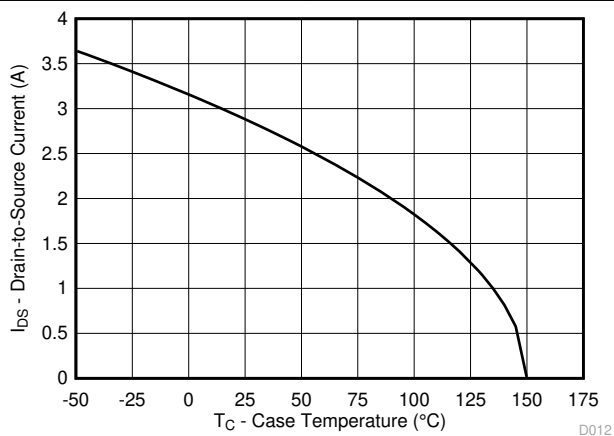


Figure 5-12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6.2 Trademarks

FemtoFET™ is a trademark of Texas Instruments.

TI E2E™ is a trademark of Texas Instruments.

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6.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

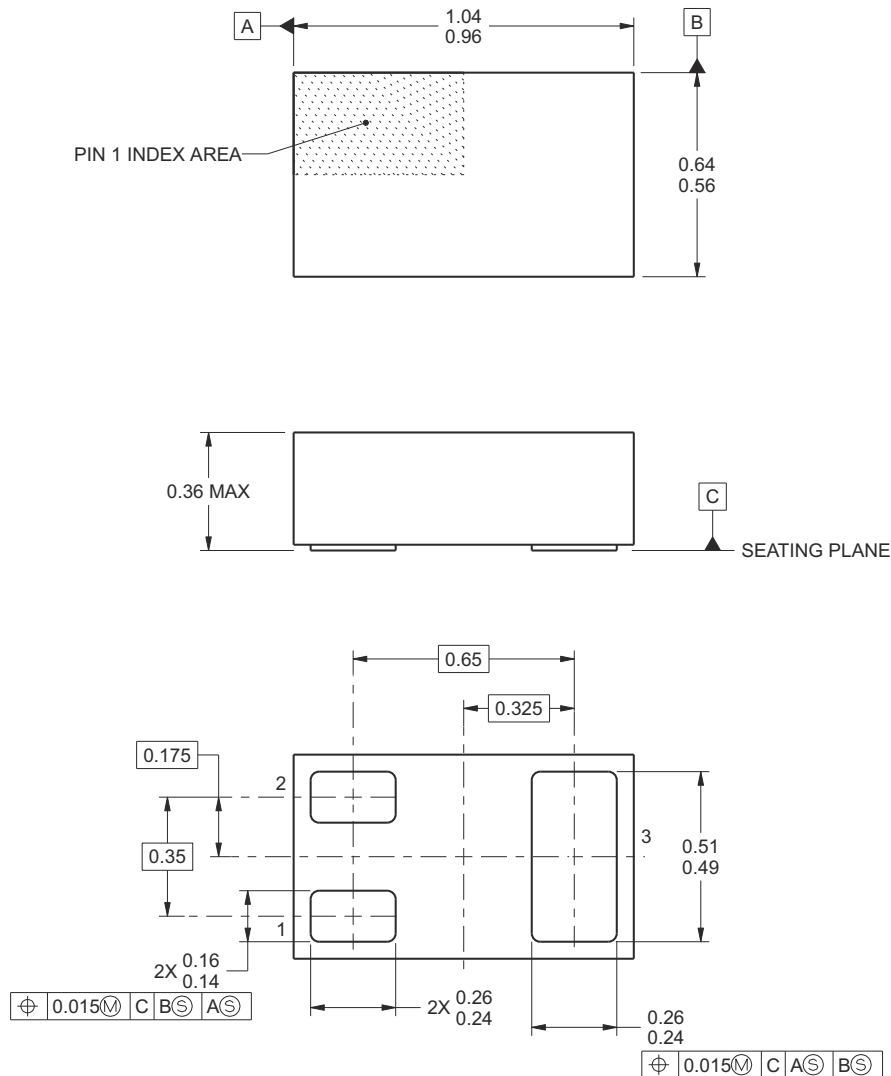
6.4 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

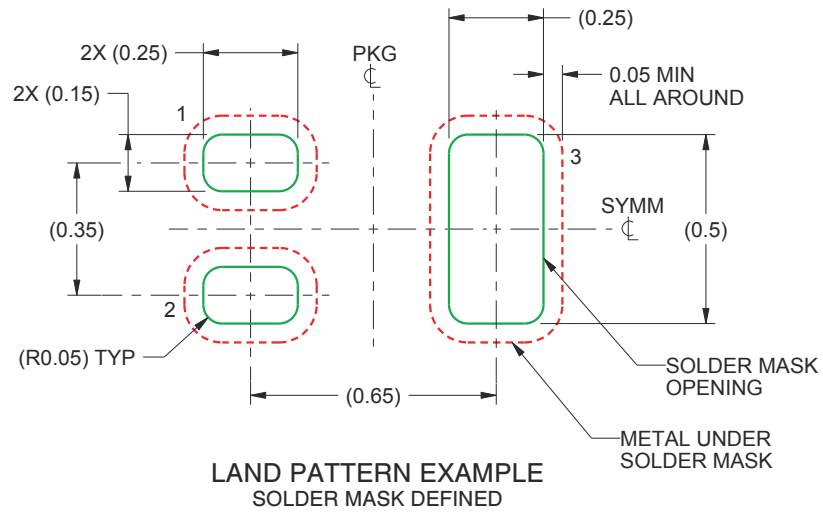
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions



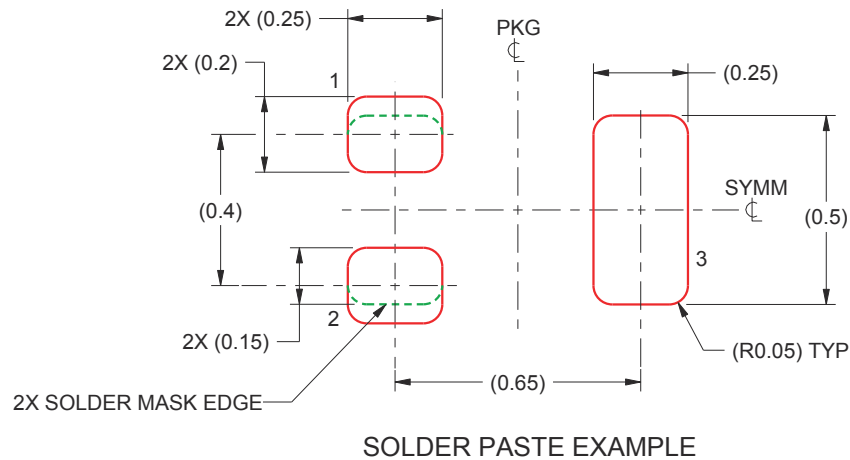
- A. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- B. This drawing is subject to change without notice.
- C. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device data sheet or contact a local TI representative.

7.2 Recommended Minimum PCB Layout



- A. All dimensions are in millimeters.
- B. For more information, see [FemtoFET Surface Mount Guide](#) (SLRA003D).

7.3 Recommended Stencil Pattern



- A. All dimensions are in millimeters.
- B. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD13383F4	Active	Production	PICOSTAR (YJC) 3	3000 LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	GC
CSD13383F4.B	Active	Production	PICOSTAR (YJC) 3	3000 LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	GC
CSD13383F4T	Active	Production	PICOSTAR (YJC) 3	250 SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	GC
CSD13383F4T.B	Active	Production	PICOSTAR (YJC) 3	250 SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	GC

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD13383F4	PICOSTAR	YJC	3	3000	180.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2
CSD13383F4T	PICOSTAR	YJC	3	250	180.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD13383F4	PICOSTAR	YJC	3	3000	182.0	182.0	20.0
CSD13383F4T	PICOSTAR	YJC	3	250	182.0	182.0	20.0

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