

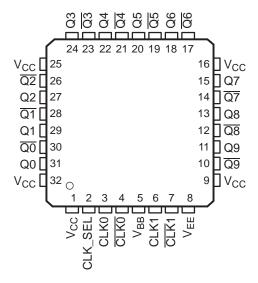
# Low-Voltage 1:10 LVPECL/HSTL With Selectable Input Clock Driver

Check for Samples: CDCLVP110

#### **FEATURES**

- Distributes One Differential Clock Input Pair LVPECL/HSTL to 10 Differential LVPECL Clock Outputs
- Fully Compatible With LVECL/LVPECL/HSTL
- Single Supply Voltage Required, ±3.3-V or ±2.5-V Supply
- Selectable Clock Input Through CLK\_SEL
- Low-Output Skew (Typ 15 ps) for Clock-Distribution Applications
- VBB Reference Voltage Output for Single-Ended Clocking
- Available in a 32-Pin LQFP Package
- Frequency Range From DC to 3.5 GHz
- Pin-to-Pin Compatible With MC100 Series EP111, ES6111, LVEP111, PTN1111





#### DESCRIPTION

The CDCLVP110 clock driver distributes one differential clock pair of either LVPECL or HSTL (selectable) input, (CLK0, CLK1) to ten pairs of differential LVPECL clock (Q0, Q9) outputs with minimum skew for clock distribution. The CDCLVP110 can accept two clock sources into an input multiplexer. The CLK0 input accepts either LVECL/LVPECL input signals, while CLK1 accepts an HSTL input signal when operated under LVPECL conditions. The CDCLVP110 is specifically designed for driving  $50\text{-}\Omega$  transmission lines.

The VBB reference voltage output is used if single-ended input operation is required. In this case the VBB pin should be connected to CLKO and bypassed to GND via a 10-nF capacitor.

However, for high-speed performance up to 3.5 GHz, the differential mode is strongly recommended.

The CDCLVP110 is characterized for operation from -40°C to 85°C.

**Table 1. FUNCTION TABLE** 

CLK_SEL	ACTIVE CLOCK INPUT
0	CLK0, CLK0
1	CLK1, CLK1

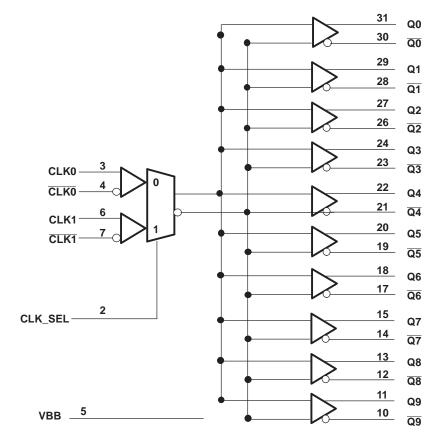


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



### **TERMINAL FUNCTIONS**

TER	MINAL	DESCRIPTION
NAME	NO.	DESCRIPTION
CLK_SEL	2	Clock select. Used to select between CLK0 and CLK1 input pairs.
CLK0, CLK0	3, 4	Differential LVECL/LVPECL input pair
CLK1, CLK1	6, 7	Differential HSTL input pair
Q [9:0]	11, 13, 15, 18, 20, 22, 24, 27, 29, 31	LVECL/LVPECL clock outputs, these outputs provide low-skew copies of CLKn.
Q[9:0]	10, 12, 14, 17, 19, 21,23, 26, 28, 30	LVECL/LVPECL complementary clock outputs, these outputs provide copies of CLKn.
$V_{BB}$	5	Reference voltage output for single-ended input operation
V <sub>CC</sub>	1, 9, 16, 25, 32	Supply voltage
V <sub>EE</sub>	8	Device ground or negative supply voltage in ECL mode



### **ABSOLUTE MAXIMUM RATINGS**(1)

		VALUE	UNIT
$V_{CC}$	Supply voltage	-0.3 to 4.6	V
VI	Input voltage	$-0.3$ to $V_{CC} + 0.5$	V
Vo	Output voltage	-0.3 to V <sub>CC</sub> + 0.5	V
I <sub>IN</sub>	Input current	±20	mA
$V_{EE}$	Negative supply voltage	-0.3 to 4.6	V
$I_{BB}$	Sink/source current	-1 to 1	mA
Io	DC output current	<b>-</b> 50	mA
T <sub>stg</sub>	Storage temperature range	-65 to 150	°C

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage (relative to V <sub>EE</sub> )	2.375	2.5/3.3	3.8	V
T <sub>A</sub> (1)	Operating free-air temperature	-40		85	°C

<sup>(1)</sup> Operating junction temperature affects device lifetime. The continuous operation junction temperature is recommended to be at max 110°C. The device ac and dc parameters are specified up to 85°C ambient temperature. See the PCB Layout Guidelines for CDCLVP110 application note, literature number SCAA057 for more details.

#### PACKAGE THERMAL IMPEDANCE

		TEST CONDITIONS	MIN MAX	UNIT
		0 LFM	74	°C/W
	Thermal registeres innetion to embient(1)	150 LFM	66	°C/W
$\Theta_{JA}$	Thermal resistance junction to ambient <sup>(1)</sup>	250 LFM	64	°C/W
		500 LFM	61	°C/W
$\Theta_{JC}$	Thermal resistance junction to case		39	°C/W

<sup>(1)</sup> According to JESD 51-7 standard.

### LVECL DC ELECTRICAL CHARACTERISTICS

Vsupply:  $V_{CC} = 0 \text{ V}$ ,  $V_{EE} = -2.375 \text{ V}$  to -3.8 V

	PARAMETER	TEST CONDITIONS			TYP	MAX	UNIT
			-40°C	40		78	
$I_{EE}$	Supply internal current	Absolute value of current	25°C	45		82	mA
			85°C	48		85	
			-40°C			343	
$I_{CC}$	Output and internal supply current	All outputs terminated 50 $\Omega$ to $V_{CC}$ – 2 $V$	25°C			370	mA
	Carrent		85°C			380	
I <sub>IN</sub>	Input current		–40°C, 25°C, 85°C			150	μΑ
.,		For $V_{EE} = -3$ to -3.8 V, $I_{BB} = -0.2$ mA	–40°C, 25°C, 85°C	-1.45	-1.3	-1.15	V
$V_{BB}$	Internally generated bias voltage	$V_{EE} = -2.375 \text{ to } -2.75 \text{ V}, I_{BB} = -0.2 \text{ mA}$	–40°C, 25°C, 85°C	-1.4	-1.25	-1.1	V
V <sub>IH</sub>	High-level input voltage (CLK_SEL)		–40°C, 25°C, 85°C	-1.165		-0.88	V
V <sub>IL</sub>	Low-level input voltage (CLK_SEL)		–40°C, 25°C, 85°C	-1.81		-1.475	V
VIN <sub>PP</sub>	Input amplitude (CLK0, CLK0)	Difference of input 9 V <sub>IH</sub> –V <sub>IL</sub> , See Note <sup>(1)</sup>	–40°C, 25°C, 85°C	0.5		1.3	V
V <sub>CM</sub>	Common-mode voltage (CLK0, CLK0)	Cross point of input 9 average (V <sub>IH</sub> , V <sub>IL</sub> )	–40°C, 25°C, 85°C	V <sub>EE</sub> + 0.975		-0.3	V
			-40°C	-1.26		-0.9	
$V_{OH}$	High-level output voltage	I <sub>OH</sub> = -21 mA	25°C	-1.2		-0.9	٧
			85°C	-1.15		-0.9	

<sup>(1)</sup> VIN<sub>PP</sub> minimum and maximum is required to maintain ac specifications, actual device function tolerates a minimum VIN<sub>PP</sub> of 100 mV.



### LVECL DC ELECTRICAL CHARACTERISTICS (continued)

Vsupply:  $V_{CC} = 0 \text{ V}$ ,  $V_{EE} = -2.375 \text{ V}$  to -3.8 V

	PARAMETER	TEST CONDITIONS			TYP MAX	UNIT
			-40°C	-1.85	-1.5	
V <sub>OL</sub>	Low-level output voltage	$I_{OL} = -5 \text{ mA}$	25°C	-1.85	-1.45	V
			85°C	-1.85	-1.4	
V <sub>OD</sub>	Differential output voltage swing	Terminated with 50 $\Omega$ to V <sub>CC</sub> – 2 V, See Figure 3	–40°C, 25°C, 85°C	600		V

### LVPECL/HSTL DC ELECTRICAL CHARACTERISTICS

Vsupply:  $V_{CC} = 2.375 \text{ V to } 3.8 \text{ V}, V_{EE} = 0 \text{ V}$ 

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
			-40°C	40		78	
I <sub>EE</sub>	Supply internal current	Absolute value of current	25°C	45		82	mA
			85C	48		85	
			-40°C			343	
$I_{CC}$	Output and internal supply current	All outputs terminated 50 $\Omega$ to $V_{CC}$ – 2 $V$	25°C			370	mA
`	ourron.		85°C			380	
I <sub>IN</sub>	Input current		–40°C, 25°C, 85°C			150	μΑ
V	Internally generated bias	$V_{EE} = -3 \text{ to } -3.8 \text{ V}, I_{BB} = -0.2 \text{ mA}$	–40°C, 25°C, 85°C	V <sub>CC</sub> – 1.45	V <sub>CC</sub> – 1.3	V <sub>CC</sub> – 1.15	V
$V_{BB}$	voltage	$V_{EE} = -2.375 \text{ to } -2.75 \text{ V}, I_{BB} = -0.2 \text{ mA}$	–40°C, 25°C, 85°C	V <sub>CC</sub> - 1.4	V <sub>CC</sub> - 1.25	V <sub>CC</sub> - 1.1	V
$V_{IH}$	High-level input voltage (CLK_SEL)		-40°C, 25°C, 85°C	V <sub>CC</sub> - 1.165		V <sub>CC</sub> - 0.88	٧
V <sub>IL</sub>	Low-level input voltage (CLK_SEL)		-40°C, 25°C, 85°C	V <sub>CC</sub> - 1.81		V <sub>CC</sub> - 1.475	V
VIN <sub>PP</sub>	Input amplitude (CLK0, CLK0)	Difference of input 9 V <sub>IH</sub> -V <sub>IL</sub> , see Note <sup>(1)</sup>	-40°C, 25°C, 85°C	0.5		1.3	V
V <sub>IC</sub>	Common-mode voltage (CLK0, CLK0)	Cross point of input 9 average (V <sub>IH</sub> , V <sub>IL</sub> )	-40°C, 25°C, 85°C	0.975		V <sub>CC</sub> - 0.3	V
$V_{\text{ID}}$	Differential input_voltage (CLK1, CLK1)	Difference of input V <sub>IH</sub> –V <sub>IL</sub> , See Note <sup>(1)</sup>	-40°C, 25°C, 85°C	0.4		1.9	٧
$V_{I(x)}$	Input crossover voltage (CLK1, CLK1)	Cross point of input 9 average (V <sub>IH</sub> , V <sub>IL</sub> )	-40°C, 25°C, 85°C	0.68		0.9	٧
			-40°C	V <sub>CC</sub> – 1.26		$V_{CC} - 0.9$	
$V_{OH}$	High-level output voltage	$I_{OH} = -21 \text{ mA}$	25°C	V <sub>CC</sub> - 1.2		$V_{CC} - 0.9$	V
	romago		85°C	V <sub>CC</sub> - 1.15		V <sub>CC</sub> - 0.9	
			-40°C	V <sub>CC</sub> - 1.85		V <sub>CC</sub> - 1.5	
$V_{OL}$	Low-level output voltage	$I_{OL} = -5 \text{ mA}$	25°C	V <sub>CC</sub> - 1.85		V <sub>CC</sub> - 1.45	V
				V <sub>CC</sub> - 1.85		V <sub>CC</sub> - 1.4	
V <sub>OD</sub>	Differential output voltage swing	Terminated with 50 $\Omega$ to $V_{CC}$ – 2 V, See Figure 4	-40°C, 25°C, 85°C	600			mV

<sup>(1)</sup> VINPP minimum and maximum is required to maintain ac specifications, actual device function tolerates a minimum VINPP of 100 mV.



### **AC ELECTRICAL CHARACTERISTICS**

Vsupply:  $V_{CC}$  = 2.375 V to 3.8 V,  $V_{EE}$  = 0 V or LVECL/LVPECL input  $V_{CC}$  = 0 V,  $V_{EE}$  = -2.375 V to -3.8 V

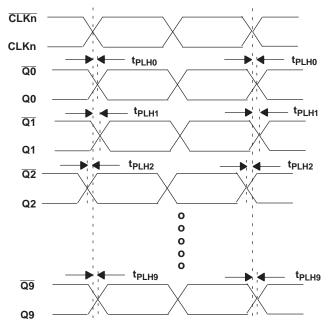
	PARAMETER	TEST CONDITIONS			TYP	MAX	UNIT
t <sub>pd</sub>	Differential propagation delay CLK0, CLK0 to all Q0, Q0 Q9, Q9	Input condition: VCM = 1 V, V <sub>PP</sub> = 0.5 V	-40°C, 25°C, 85°C	230		350	ps
t <sub>sk(pp)</sub>	Part-to-part skew	See Note B and Figure 1	–40°C, 25°C, 85°C			70	ps
t <sub>sk(o)</sub>	Output-to-output skew	See Note A and Figure 1	–40°C, 25°C, 85°C		15	30	ps
t <sub>(JITTER)</sub>	Cycle-to-cycle RMS jitter		-40°C, 25°C, 85°C			< 1	ps
f <sub>(max)</sub>	Maximum frequency	Functional up to 3.5 GHz, timing specifications apply at 1 GHz, see Figure 3	-40°C, 25°C, 85°C			3500	MHz
t <sub>r</sub> /t <sub>f</sub>	Output rise and fall time (20%, 80%)		–40°C, 25°C, 85°C	100		200	ps

### **HSTL INPUT**

Vsupply:  $V_{CC} = 2.375 \text{ V to } 3.8 \text{ V}, V_{EE} = 0 \text{ V}$ 

	PARAMETER	TEST CONDITIONS			TYP MAX	UNIT
t <sub>pd</sub>	Differential propagation delay CLK0, CLK0 to all Q0, Q0 Q9, Q9	Input condition: $V_x = 0.68 \text{ V}$ , $V_{dif} = 0.4 \text{ V}$	–40°C, 25°C, 85°C	290	370	ps
t <sub>sk(pp)</sub>	Part-to-part skew	See Note B and Figure 1	–40°C, 25°C, 85°C		70	ps
t <sub>sk(o)</sub>	Output to output skew	See Note A and Figure 1	–40°C, 25°C, 85°C		10 30	ps
t <sub>(JITTER)</sub>	Cycle-to-cycle RMS jitter		–40°C, 25°C, 85°C		<1	ps
f <sub>(max)</sub>	Maximum frequency	Functional up to 3.5 GHz, timing specifications apply at 1 GHz, See Figure 4	–40°C, 25°C, 85°C		3500	MHz
t <sub>r</sub> /t <sub>f</sub>	Output rise and fall time (20%, 80%)		–40°C, 25°C, 85°C	100	200	ps





- A. Output skew is calculated as the greater of: The difference between the fastest and the slowest  $t_{PLHn}$  (n = 0, 1,...9) or the difference between the fastest and the slowest  $t_{PHLn}$  (n = 0, 1,...9).
- B. Part-to-part skew, is calculated as the greater of: The difference between the fastest and the slowest  $t_{PLHn}$  (n = 0, 1,...9) across multiple devices or the difference between the fastest and the slowest  $t_{PHLn}$  (n = 0, 1,...9) across multiple devices.

Figure 1. Waveform for Calculating Both Output and Part-to-Part Skew

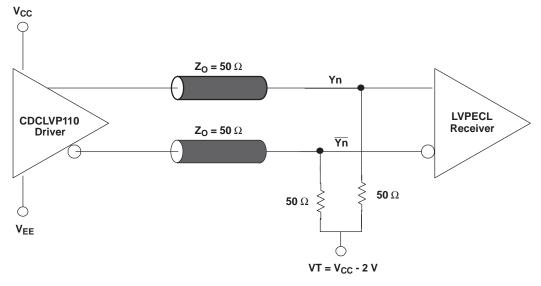


Figure 2. Typical Termination for Output Driver (See the Interfacing Between LVPECL, LVDS, and CML Application Note, Literature Number SCAA056)



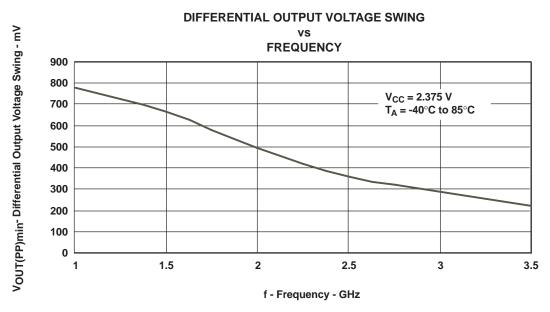


Figure 3. LVPECL Input Using CLK0 Pair, VCM = 1 V, VIN<sub>dif</sub> = 0.5 V

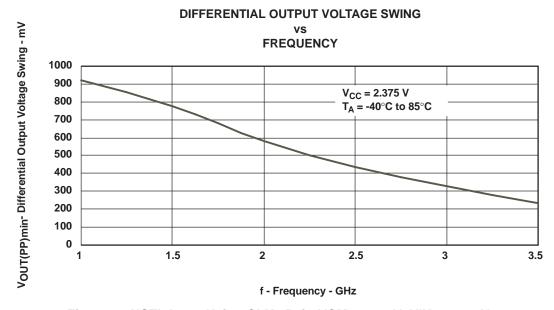


Figure 4. HSTL Input Using CLK1 Pair, VCM = 0.68 V, VIN<sub>dif</sub> = 0.4 V



### **REVISION HISTORY**

Changes from Revision A (August 2002) to Revision B	Page
Changed PACKAGE THERMAL IMPEDANCE max values	3
Deleted I <sub>IN</sub> test condition	3
Deleted I <sub>IN</sub> test condition	
Changes from Revision B (January 2010) to Revision C	Page
• Changed LVECL DC spec for V <sub>BB</sub> (V <sub>EE</sub> = −3 to −3.8 V) from 3 rows to 1 row and added TYP value	3
<ul> <li>Changed LVECL DC spec for V<sub>BB</sub> (V<sub>EE</sub> = -2.375 to -2.75 V); MIN value from -1.38 V to -1.4 V, MAX from -1.16 V to -1.1 V, and added TYP value of -1.25 V</li> </ul>	3
<ul> <li>Changed LVECL/HSTL DC spec for V<sub>BB</sub> (V<sub>EE</sub> = -3 to -3.8 V) from 3 rows to 1 row and added TYP value.</li> </ul>	4
• Changed LVECL/HSTL DC spec for $V_{BB}$ ( $V_{EE}$ = -2.375 to -2.75 V); MIN value from $V_{CC}$ -1.38 V to $V_{CC}$ -1.4 V; MAX from $V_{CC}$ -1.16 V to $V_{CC}$ -1.1 V; and added TYP value of $V_{CC}$ -1.25 V	
Changes from Revision C (January 2011) to Revision D	Page
Changed V <sub>CM</sub> spec from V <sub>EE</sub> +1 to V <sub>EE</sub> +0.975	3
Changed V <sub>IC</sub> spec from 1 to 0.975	

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
CDCLVP110MVFR	Active	Production	LQFP (VF)   32	1000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCLVP110
CDCLVP110MVFR.B	Active	Production	LQFP (VF)   32	1000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCLVP110
CDCLVP110VF	Active	Production	LQFP (VF)   32	250   JEDEC TRAY (10+1)	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCLVP110
CDCLVP110VF.B	Active	Production	LQFP (VF)   32	250   JEDEC TRAY (10+1)	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCLVP110
CDCLVP110VFG4	Active	Production	LQFP (VF)   32	250   JEDEC TRAY (10+1)	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCLVP110
CDCLVP110VFR	Active	Production	LQFP (VF)   32	1000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCLVP110
CDCLVP110VFR.B	Active	Production	LQFP (VF)   32	1000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCLVP110

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



## PACKAGE OPTION ADDENDUM

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and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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# **PACKAGE MATERIALS INFORMATION**

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### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCLVP110MVFR	LQFP	VF	32	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q1
CDCLVP110VFR	LQFP	VF	32	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2

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### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins SPQ		Length (mm)	Width (mm)	Height (mm)		
CDCLVP110MVFR	LQFP	VF	32	1000	367.0	367.0	38.0		
CDCLVP110VFR	LQFP	VF	32	1000	367.0	367.0	38.0		



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### **TRAY**



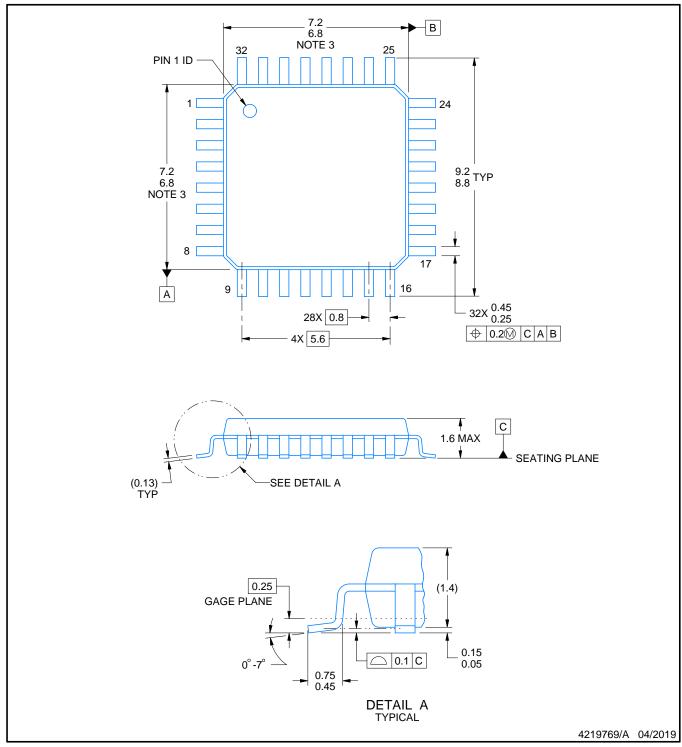
Chamfer on Tray corner indicates Pin 1 orientation of packed units.

#### \*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	Κ0 (μm)	P1 (mm)	CL (mm)	CW (mm)
CDCLVP110VF	VF	LQFP	32	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
CDCLVP110VF.B	VF	LQFP	32	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
CDCLVP110VFG4	VF	LQFP	32	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25



PLASTIC QUAD FLATPACK



NOTES:

PowerPAD is a trademark of Texas Instruments.

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

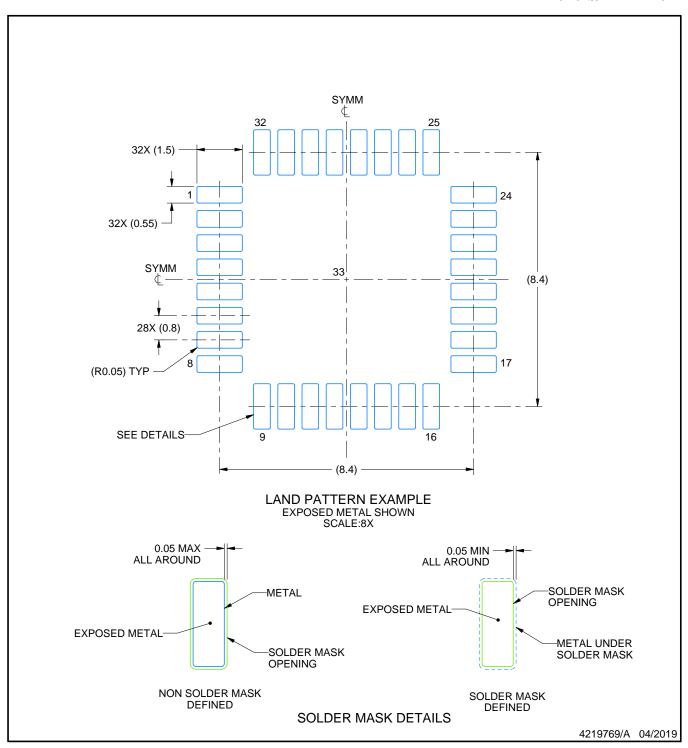
  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs.

- 4. Reference JEDEC registration MS-026.



PLASTIC QUAD FLATPACK



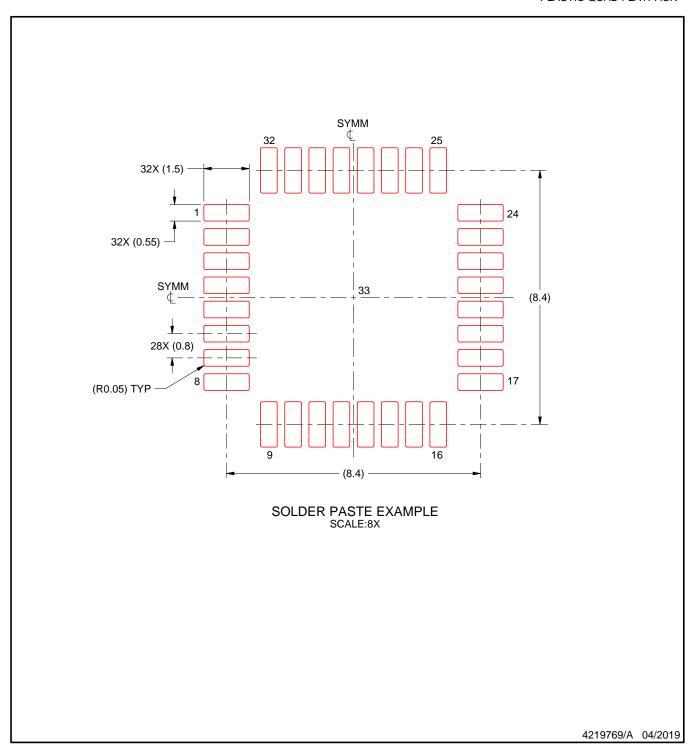
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



PLASTIC QUAD FLATPACK



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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