

CD74HCx4067-Q1 Automotive High-Speed CMOS Logic 16-Channel Analog **Mulitplexer and Demultiplexer**

1 Features

- Qualified for automotive applications
- AEC-Q100 test guidance with the following results:
 - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
 - Device HBM ESD Classification Level H1A
 - Device CDM ESD Classification Level C2
- Wide analog input voltage range
- Low ON resistance
 - 70 Ω typical (V_{CC} = 4.5V)
- Fast switching and propagation speeds
- Break-before-make switching
 - 6ns typical ($V_{CC} = 4.5V$)
- Fanout (over temperature range)
 - Standard outputs: 10 LSTTL loads
 - Bus driver outputs: 15 LSTTL loads
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL logic ICs
- 4.5V to 5.5V operation
- Direct LSTTL input logic compatibility: V_{IL} = 0.8V maximum, V_{IH} = 2V minimum
- CMOS input compatibility: I₁ ≤ 1µA at V_{OI} , V_{OH}

2 Applications

- **Automotive**
- Analog switch
- Analog multiplexer and demultiplexer

3 Description

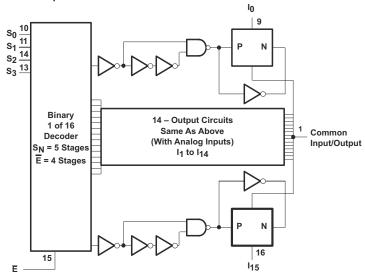
The CD74HCx4067-Q1 device is a digitally controlled analog switch that utilizes silicon-gate CMOS technology to achieve operating speeds similar to LSTTL, with the low power consumption of standard CMOS integrated circuits.

This analog multiplexer and demultiplexer controls analog voltages that may vary across the voltage supply range. It is a bidirectional switch, thus allowing any analog input to be used as an output and viceversa. The switch has low (on) resistance and low (off) leakages. In addition, the device has an enable control that, when high, disables all switches to their off state.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
CD74HCx4067QM96Q1	DW (SOIC, 24)	15.5mm × 10.3mm
CD74HCx4067QRGYRQ 1	RGY (QFN, 24)	5.5mm × 3.5mm
CD74HCx4067QDGSRQ 1	DGS (VSSOP, 24)	6.1mm × 3mm
CD74HCx4067QPWRQ1	PW (TSSOP, 24)	4.4mm × 7.8mm

- (1) For more information, see Section 18.
- The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)



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4 Pin Configuration and Functions

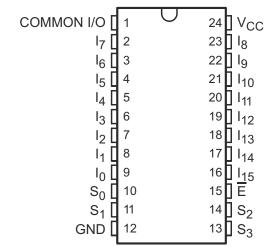


Figure 4-1. DW Package, 24-Pin SOIC (Top View)

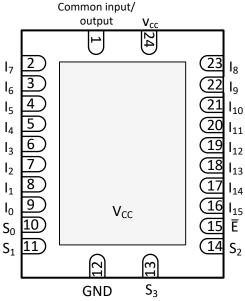


Figure 4-2. RGY Package, 24-Pin QFN (Top View) (Pad on Bottom)

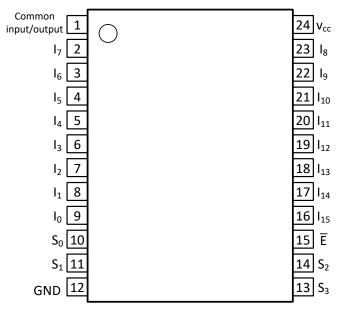


Figure 4-3. PW Package, 24-Pin TSSOP (Top View)

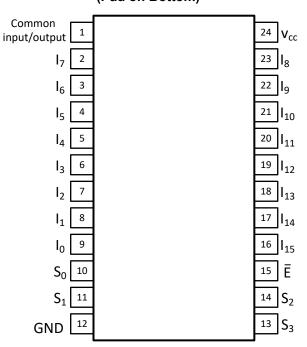


Figure 4-4. DGS Package, 24-Pin VSSOP (Top View)



PI	N	TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.	ITPE	DESCRIPTION
COMMON INPUT/ OUTPUT	1	Ю	Common input or output.
I ₇	2	Ю	Switch input/output
I ₆	3	Ю	Switch input/output
I ₅	4	Ю	Switch input/output
I ₄	5	Ю	Switch input/output
I ₃	6	Ю	Switch input/output
I ₂	7	10	Switch input/output
I ₁	8	10	Switch input/output
I ₀	9	10	Switch input/output
S ₀	10	I	Select/Address pin
S ₁	11	I	Select/Address pin
GND	12	Р	Ground pin
S ₃	13	I	Select/Address pin
S ₂	14	I	Select/Address pin
Ē	15	I	Enable for all switches ON/OFF
I ₁₅	16	10	Switch input/output
I ₁₄	17	10	Switch input/output
I ₁₃	18	10	Switch input/output
I ₁₂	19	10	Switch input/output
I ₁₁	20	10	Switch input/output
I ₁₀	21	10	Switch input/output
l ₉	22	Ю	Switch input/output
I ₈	23	10	Switch input/output
V _{CC}	24	Р	Power pin
Thermal Pac	t	-	The thermal pad is not electrically connected and can be floated, grounded or tied to V _{CC}

(1) I = input, O = output. P = power



5 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
V _{CC} HC	DC Supply voltage	DO Committee of		7	V
V _{CC} HCT	DC Supply voltage		-0.5	7	V
I _{IK}	DC input diode current	For V _I < -0.5V or V _I > V _{CC} + 0.5V	-20	20	mA
I _{OK}	DC output diode current	For V _O < -0.5V or V _O > V _{CC} + -0.5V	-20	20	mA
Icc	DC V _{CC} or ground current		-50	50	mA
DC Output Source or Sink Current per Output Pin, I _O	For V _O > -0.5V or V _O < V _{CC} + -0.5V		-25	25	mA
T _{JMAX}	Maximum junction temperature (Plastic Package)			150	°C
T _{stg}	Storage temperature		-65	150	°C

⁽¹⁾ Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6 ESD Ratings

V		Human body model (HBM), per AEC Q100-002, all pins ⁽¹⁾	400	V
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per AEC Q100-011, all pins	250	V

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

⁽²⁾ All voltages are with respect to ground, unless otherwise specified.



7 Thermal Information

		CD74HCx4067					
	THERMAL METRIC (1)	DW (SOIC)	RGY (QFN)	DGS (VSSOP)	PW (TSSOP)	UNIT	
		24 PINS	24 PINS	24 PINS	24 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	84.8	67.1	96.8	97.4	°C/W	
R _{θJC(top)}	Junction-to-case (top) thermal resistance	57.0	59.2	43.4	45.0	°C/W	
R _{θJB}	Junction-to-board thermal resistance	59.5	45.4	58.7	62.7	°C/W	
Ψ_{JT}	Junction-to-top characterization parameter	29.0	9.3	3.9	5.20	°C/W	
Ψ_{JB}	Junction-to-board characterization parameter	59.0	45.1	58.2	62.1	°C/W	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	34.7	N/A	N/A	°C/W	

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

8 Recommended Operating Conditions

			MIN	NOM MA	UNIT
V _{CC}	Supply voltage range (T _A = full package temperature range)	74HC types	2		6 V
V _{CC}	Supply voltage range (T _A = full package temperature range)	74HCT types	4.5	5.	5 V
V _{IS}	Analog switch I/O voltage		0	V _C	c V
T _A	Ambient temperature	Ambient temperature	-40	12	5 °C
		2V	0	100)
t _r , t _f	Input rise and fall times	4.5V	0	50) ns
		6V	0	40	D



9 Electrical Characteristics: HC Devices

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT									
Analog Switch																		
		V _{IS} (V)	V _I (V)	V _{CC} (V)	T _A													
				2		1.5												
High Level Input Voltage	V_{IH}			4.5		3.15			V									
				6	-40°C to 125°C	4.2												
				2	-40 C to 125 C			0.5										
Low Level Input Voltage	VIL			4.5				1.35	V									
				6				1.8										
				4.5	25°C		70	160										
		V or GND	V or CND	4.5	-40°C to 125°C			200										
		V _{CC} or GND	V _{CC} or GND	6	25°C		60	140										
ON" Resistance IO = 1mA	R _{ON}			6	-40°C to 125°C			175										
		V _{CC} to GND		4.5	25°C		90	180	12									
			V to GND V 1	V to CND	V to CND	V to CND	V to CND	V to CND	V to GND	V to CND	D V to CND	V _{CC} to GND V _{CC} to GND	4.5	-40°C to 125°C			225	
			V _{CC} to GND	6	25°C		80	160	4 1									
				6	-40°C to 125°C			200										
"ON" Resistance Between Any Two	ΛD			4.5	25°C		10		Ω									
Switches	ΔR_{ON}			6	25°C		8.5		12									
Off-Switch Leakage Current		E = V _{CC}	V or CND	6	25°C			±0.8										
On-Switch Leakage Current	IZ	E - V _{CC}	V _{CC} or GND	0	-40°C to 125°C			±8	μA									
Input Lockego Current (Any Control)			V _{CC} or	6	25°C			±0.1										
Input Leakage Current (Any Control)	IL		GND ⁽¹⁾	U	–40°C to 125°C			±1	μA									
Quiescent Device Current			V or CND	6	25°C			8										
	I _{CC}		V _{CC} or GND	U	-40°C to 125°C			160	μA									

⁽¹⁾ Any voltage between $V_{\mbox{\footnotesize CC}}$ and GND.



10 Electrical Characteristics: HCT Devices

Over operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
Analo	g Switch									
			V _{IS} (V)	V _I (V)	V _{CC} (V)	T _A				
High L	evel Input Voltage	V _{IH}			4.5	25°C	2			V
Low Le	evel Input Voltage	V_{IL}			4.5	–40°C to 125°C			0.8	V
			V _{CC} or GND	V _{CC} or GND		25°C		70	160	
"ON" F	Resistance IO = 1mA	В	ACC OL QIAD	ACC OL GIAD	4.5	–40°C to 125°C			200	Ω
ON F	ON Resistance to – IIIIA	R _{ON}	VCC to CND	VOO to OND	4.5	25°C		90	180	12
		VCC to GND VCC to GND	VCC to GND		–40°C to 125°C			225		
"ON" F Switch	Resistance Between Any Two es	ΔR _{ON}			4.5	25°C		10		Ω
O# C	iitala I a alka wa Ouwant		E - \/	V CND	F F	25°C			±0.8	
OII-SW	ritch Leakage Current	I _Z	$\overline{E} = V_{CC}$	V _{CC} or GND	5.5	–40°C to 125°C			±8	μA
Innut I	calcage Current (Any Central)			V or CND	<i>E E</i>	25°C			±0.1	
input L	.eakage Current (Any Control)	I _{IL}		V _{CC} or GND	5.5	–40°C to 125°C			±1	μA
Quieso	cent Device Current		N/	V or CND	5.5	25°C			8	
		I _{CC}		V _{CC} or GND	5.5	–40°C to 125°C			80	μA
	onal Quiescent Device Current	ΔI_{CC}				25°C		100	360	
Per Inp	Per Input Pin: 1 Unit Load			V _{CC} - 2.1	4.5 to 5.5	–40°C to 125°C			450	μA
						25°C			10	
CI	Control inputs					–55°C to 85°C			10	pF
						–55°C to 125°C			10	

⁽¹⁾ For dual-supply systems theoretical worst case (V_1 = 2.4V, V_{CC} = 5.5V) specification is 1.8mA



11 Switching Characteristics HC

over operating free-air temperature range (unless otherwise noted)

	Parameter	Test	Conditions	C _L (pF)	MIN NOM	MAX	UNIT	
	FROM (INPUT) TO (OUTPUT)	V _{CC} (V)	T _A					
		2	25°C			75		
			-40°C to 125°C			110	ns	
		4.5	25°C			15		
	I TO Common I/O		-40°C to 125°C	50		22	ns	
t _{pd}	I _n TO Common I/O	6	25°C			13		
			-40°C to 125°C			19	ns	
		5	25°C	15	6		ns	
		2	25°C			275		
			-40°C to 125°C			415	ns	
		4.5	25°C			55		
	= = 0	4.5	-40°C to 125°C	50		83	ns	
t _{en}	E TO Common I/O	6	25°C			47		
		O	-40°C to 125°C			71	ns	
I		5	25°C	15	23		ns	
		2	25°C			300		
		2	-40°C to 125°C	- 50		450	ns	
		4.5	25°C			60		
		4.5	-40°C to 125°C			90	ns	
t _{en}	S _n TO Common I/O	6	25°C			51		
		l o	-40°C to 125°C	15		76	ns	
		5	25°C		25		ns	
			25°C			275		
		2	-40°C to 125°C	-		415	ns	
			25°C			55		
		4.5	-40°C to 125°C	50		83	ns	
t_{dis}	Ē TO Common I/O		25°C	-		47		
		6	-40°C to 125°C			71	ns	
l		5	25°C	15	23	, ,	ns	
			25°C			200		
		2				290	ns	
			-40°C to 125°C			435		
		4.5	25°C	- 50		58	ns	
t_{dis}	S _n TO Common I/O		-40°C to 125°C			87		
		6	25°C			49	ns	
			-40°C to 125°C			74		
		5	25°C	15	21		ns	



over operating free-air temperature range (unless otherwise noted)

Parameter		Test Co	nditions	C _L (pF)	MIN	NOM	MAX	UNIT
C _{PD} Power dissipatio n capacitan ce(1)	C _{PD}	5	25°C			93		pF



12 Switching Characteristics HCT

over operating free-air temperature range (unless otherwise noted)

	Parameter	Test Co	nditions	C _L (pF)	MIN	NOM	MAX	UNIT
	FROM (INPUT) TO (OUTPUT)	V _{CC} (V)	T _A					
		5	25°C	15		6		
t _{pd}	I _n TO Common I/O	4.5	25°C	50			15	ns
			-40°C to 125°C	50			19	
	_	5	25°C	15		25		
t _{en}	E TO Common I/O	4.5	25°C	50			60	ns
			-40°C to 125°C	- 50			75	
t _{en}	S _n TO Common I/O	5	25°C	15		25		
		4.5	25°C	- 50			60	
			-40°C to 125°C	50			75	
	_	5	25°C	15		23		
t _{dis}	E TO Common I/O	4.5	25°C	50			55	4
			-40°C to 125°C	50			69	
		5	25°C	15		21		
t _{dis}	S _n TO Common I/O	4.5	25°C	50			58	ns
			-40°C to 125°C	50			73	
C _{PD} Power dissipatio n capacitan ce(1)	C _{PD}	5	25°C			96		pF

13 Analog Channel Specifications

over operating free-air temperature range (unless otherwise noted)

Parameter	Test Co	nditions	V _{CC} (V)	НС	НСТ	UNIT
Switch Frequency Response Bandwidth at -3dB			4.5	89	89	MHz
Total Harmonic Distortion	1kHz, V _{IS} = 4V _{PP}		4.5	0.051	0.051	%
Switch "OFF" signal feedthrough			4.5	-75	-75	dB
C _S Switch input capacitance				5	5	pF
C _{COM} Common Capacitance				50	50	pF



14 Parameter Measurement Information

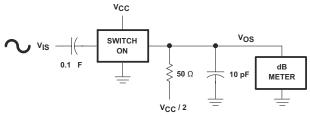


Figure 14-1. Frequency-Response Test Circuit

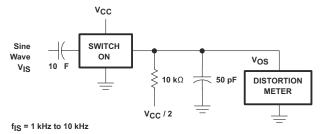


Figure 14-2. Sine-Wave Distortion Test Circuit

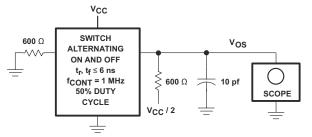


Figure 14-3. Control-to-Switch Feedthrough Noise Test Circuit

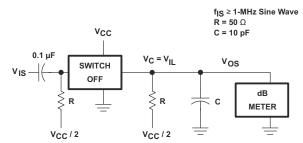
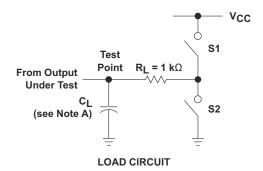
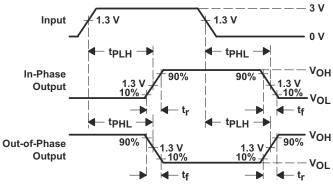


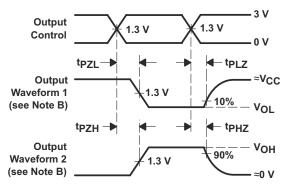
Figure 14-4. Switch OFF Signal Feedthrough Test Circuit





PARAMETER		S1	S2		
	tPZH	Open	Closed		
t _{en}	tpZL	Closed	Open		
t _{dis}	tPHZ	Open	Closed		
dis	tPLZ	Closed	Open		
t _{pd}		Open	Open		





VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

- NOTES: A. C_L includes probe and test-fixture capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_O = 50 Ω , t_r = 6 ns, t_f = 6 ns.
 - D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
 - E. The outputs are measured one at a time, with one input transition per measurement.
 - F. tpLZ and tpHZ are the same as tdis.
 - G. t_{PZL} and t_{PZH} are the same as t_{en} .
 - H. tpLH and tpHL are the same as tpd.

Figure 14-5. Load Circuit and Voltage Waveforms



15 Detailed Description

15.1 Functional Block Diagram

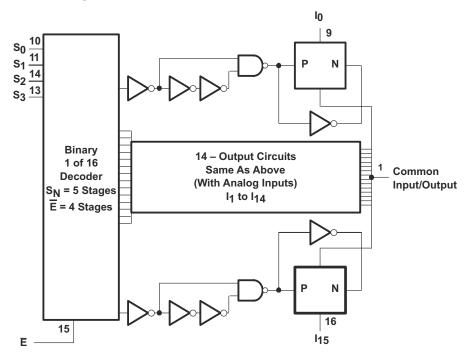


Figure 15-1. Logic Diagram (Positive Logic)

15.2 Device Functional Modes

Table 15-1. Function Table (1)

Table 16 111 diletteri 1able											
S0	S1	S2	S 3	Ē	SELECTED CHANNEL						
Х	X	X	X	Н	None						
L	L	L	L	L	0						
Н	L	L	L	L	1						
L	Н	L	L	L	2						
Н	Н	L	L	L	3						
L	L	Н	L	L	4						
Н	L	Н	L	L	5						
L	Н	Н	L	L	6						
Н	Н	Н	L	L	7						
L	L	L	Н	L	8						
Н	L	L	Н	L	9						
L	Н	L	Н	L	10						
Н	Н	L	Н	L	11						
L	L	Н	Н	L	12						
Н	L	Н	Н	L	13						
L	Н	Н	Н	L	14						
Н	Н	Н	Н	L	15						

⁽¹⁾ H = High level

L = Low level

X = Don't Care



16 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

16.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

16.2 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

16.3 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

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16.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

16.5 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

17 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

С	hanges from Revision C (February 2025) to Revision D (April 2025)	Page
•	Added CD74HC4067-Q1	1
С	hanges from Revision B (April 2008) to Revision C (February 2025)	Page
•	Updated the numbering format for tables, figures, and cross-references throughout the document	1
•	Updated Thermal parameters for DW package	6
•	Added RGY, DGS, and PW packages	6
•	Added HC Electrical characteristics	<mark>7</mark>
•	Added HC Switching characteristics	9
С	hanges from Revision A (April 2008) to Revision B (August 2012)	Page

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18 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

6-Sep-2025

www.ti.com

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
CD74HC4067QPWRQ1	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4067Q
CD74HC4067QPWRQ1.A	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4067Q
CD74HC4067QRGYRQ1	Active	Production	VQFN (RGY) 24	3000 LARGE T&R	Yes	FULL NIPDAU	Level-2-260C-1 YEAR	-55 to 125	HC4067Q
CD74HC4067QRGYRQ1.A	Active	Production	VQFN (RGY) 24	3000 LARGE T&R	Yes	FULL NIPDAU	Level-2-260C-1 YEAR	-55 to 125	HC4067Q
CD74HCT4067QM96Q1	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCT4067I
CD74HCT4067QM96Q1.A	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCT4067I
CD74HCT4067QPWRQ1	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCT4067Q
CD74HCT4067QPWRQ1.A	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCT4067Q
CD74HCT4067QRGYRQ1	Active	Production	VQFN (RGY) 24	3000 LARGE T&R	Yes	FULL NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HCT4067Q
CD74HCT4067QRGYRQ1.A	Active	Production	VQFN (RGY) 24	3000 LARGE T&R	Yes	FULL NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HCT4067Q
D24067IM96G4Q1	Obsolete	Production	SOIC (DW) 24	-	-	Call TI	Call TI	-40 to 85	HCT4067I

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

www.ti.com 6-Sep-2025

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OTHER QUALIFIED VERSIONS OF CD74HC4067-Q1, CD74HCT4067-Q1:

● Catalog: CD74HC4067, CD74HCT4067

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4067QPWRQ1	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
CD74HC4067QRGYRQ1	VQFN	RGY	24	3000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1
CD74HCT4067QM96Q1	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CD74HCT4067QPWRQ1	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
CD74HCT4067QRGYRQ1	VQFN	RGY	24	3000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1



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*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4067QPWRQ1	TSSOP	PW	24	2000	353.0	353.0	32.0
CD74HC4067QRGYRQ1	VQFN	RGY	24	3000	367.0	367.0	35.0
CD74HCT4067QM96Q1	SOIC	DW	24	2000	350.0	350.0	43.0
CD74HCT4067QPWRQ1	TSSOP	PW	24	2000	353.0	353.0	32.0
CD74HCT4067QRGYRQ1	VQFN	RGY	24	3000	367.0	367.0	35.0



SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



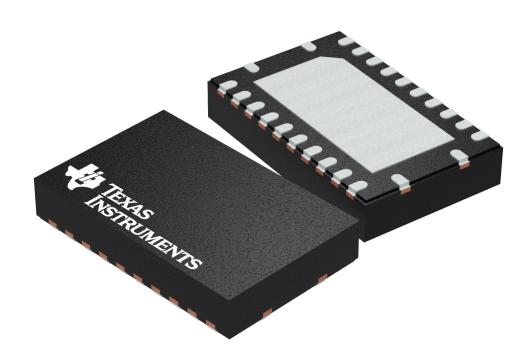
NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AD.



5.5 x 3.5 mm, 0.5 mm pitch

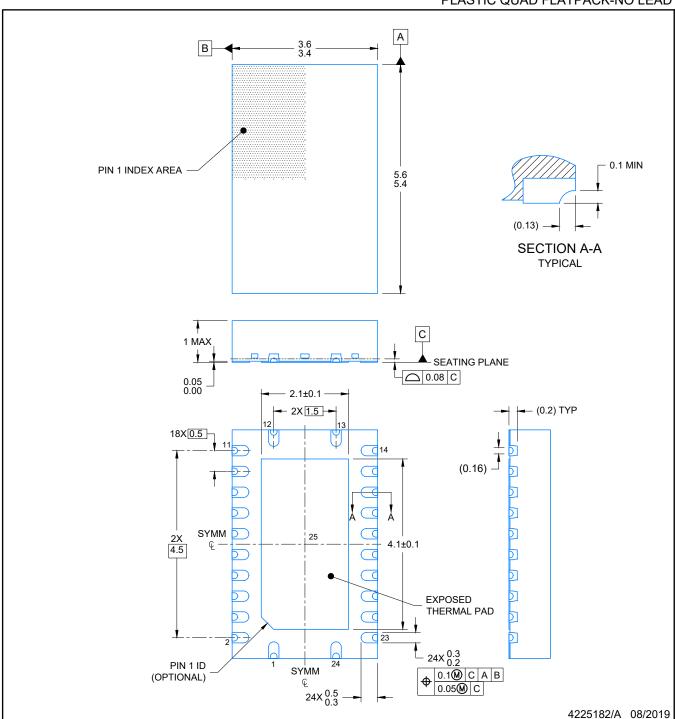
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



PLASTIC QUAD FLATPACK-NO LEAD

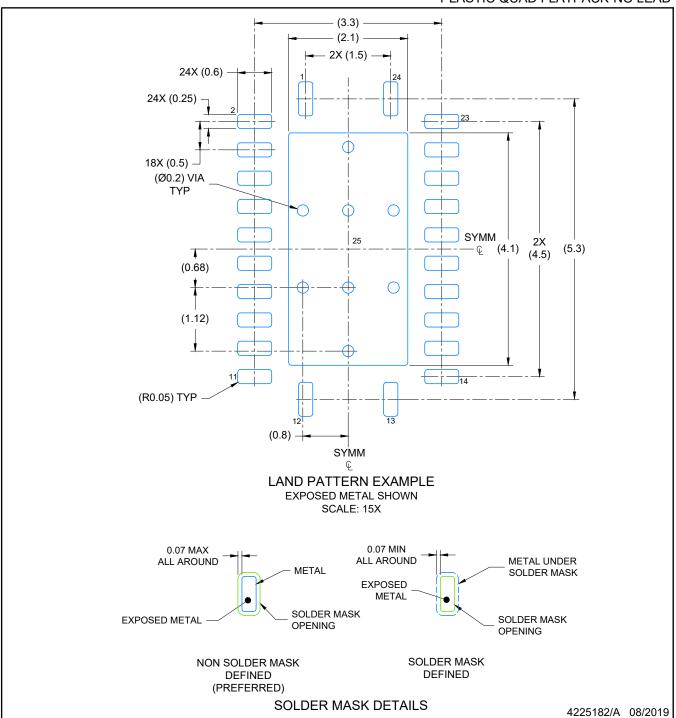


NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



PLASTIC QUAD FLATPACK-NO LEAD

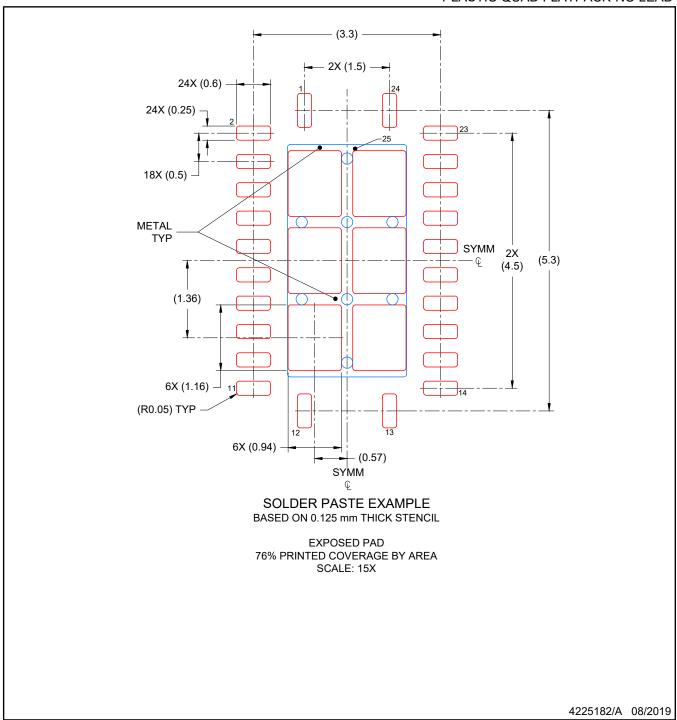


NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK-NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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