







CD54HC245, CD74HC245, CD54HCT245, CD74HCT245 SCHS119B - NOVEMBER 1998 - REVISED JULY 2022

CDx4HC(T)245 High-Speed CMOS Logic Octal-Bus Transceiver, Three-State, Non-**Inverting**

1 Features

- **Buffered** inputs
- Three-state outputs
- Bus line driving capability
- Typical propagation delay (A to B, B to A) 9ns at $V_{CC} = 5V, C_L = 15pF, T_A = 25^{\circ}C$
- Fanout (over temperature range)
 - Bus driver outputs :15 LSTTL loads
- Wide operating temperature range : -55°C to
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL logic ICs
- · HC types
 - 2 V to 6 V Operation
 - High Noise Immunity: $N_{II} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5 V$
- HCT types
 - 4.5 V to 5.5 V operation
 - Direct LSTTL input logic compatibility, V_{II} = 0.8 $V (Max), V_{IH} = 2 V (Min)$
 - − CMOS input compatibility, $I_I \le 1\mu A$ at V_{OL} , V_{OH}

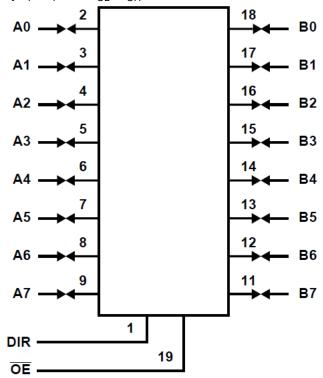
2 Description

The CDx4HC(T)245 is an octal bus transceiver with 3-state outputs. All eight channels are controlled by the direction (DIR) pin and output enable (\overline{OE}) pin.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
CD54HC245F	J (CDIP, 20)	26.92 mm × 6.92 mm
CD74HC245	N (PDIP, 20)	25.40 mm × 6.35 mm
	DW (SOIC, 20)	12.80 mm × 7.50 mm
CD54HCT245F	J (CDIP, 20)	26.92 mm × 6.92 mm
CD74HCT245	N (PDIP, 20)	25.40 mm × 6.35 mm
	DW (SOIC, 20)	12.80 mm × 7.50 mm

For all packages see the orderable addendum at the end of the data sheet.



Functional Block Diagram



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3 Revision History

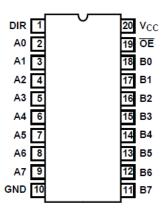
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2003) to Revision B (July 2022)

Page



4 Pin Configuration and Functions



J, N and DW Package 20-Pin CDIP, PDIP or SOIC **Top View**



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		-0.5	7	V
I _{IK}	Input diode current	For V _I < -0.5V or V _I > V _{CC} + 0.5V		±20	mA
I _{OK}	Output diode current	For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$		±20	mA
Io	Drain current, per output	For -0.5V < V _O < V _{CC} + 0.5V		±35	mA
I _O	Output source or sink current per output pin	For V _O > -0.5V or V _O < V _{CC} + 0.5V		±25	mA
	Continuous current through V _{CC} or G	GND		±50	mA
TJ	Junction temperature			150	°C
T _{stg}	Storage temperature range	Storage temperature range			
	Lead temperature (Soldering 10s)(Soldering 10s)	OIC - lead tips only)		300	°C

⁽¹⁾ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V	Supply voltage range	HC types	2	6	V
V _{CC}	Supply voltage range	HCT types	4.5	5.5	v
VI	Input voltage		0	V _{CC}	V
Vo	Output voltage		0	V _{CC}	V
		V _{CC} = 2V		1000	
t _t	Input rise and fall time	V _{CC} = 4.5V		500	ns
		V _{CC} = 6V		400	
T _A	Temperature range		-55	125	°C

5.3 Thermal Information

		DW (SOIC)	N (PDIP)	
THERMAL METRI	С	20 PINS	20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾	58	69	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.



5.4 Electrical Characteristics

	PARAMETER	TEST CONDITIONS ⁽¹⁾	V _{CC} (V)		25°C		-40°C to	85°C	-55°C 125°	UNIT	
		CONDITIONS	33, 7	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYP	PES										
			2	1.5			1.5		1.5		V
V_{IH}	High-level input voltage		4.5	3.15			3.15		3.15		V
			6	4.2			4.2		4.2		V
			2			0.5		0.5		0.5	V
V_{IL}	Low-level input voltage		4.5			1.35		1.35		1.35	V
			6			1.8		1.8		1.8	V
	High-level output voltage	I _{OH} = – 20 μA	2	1.9			1.9		1.9		V
	CMOS loads	I _{OH} = – 20 μA	4.5	4.4			4.4		4.4		V
V_{OH}		I _{OH} = – 20 μA	6	5.9			5.9		5.9		V
	High-level output voltage	I _{OH} = – 4 mA	4.5	3.98			3.84		3.7		V
	TTL loads	$I_{OH} = -5.2 \text{ mA}$	6	5.48			5.48		5.2		V
	Low-level output voltage	I _{OL} = 20 μA	2			0.1		0.1		0.1	V
	CMOS loads	I _{OL} = 20 μA	4.5			0.1		0.1		0.1	V
V_{OL}		I _{OL} = 20 μA	6			0.1		0.1		0.1	V
	Low-level output voltage	I _{OL} = 4 mA	4.5			0.26		0.33		0.4	V
	TTL	I _{OL} = 5.2 mA	6			0.26		0.33		0.4	V
l _l	Input leakage current	$V_I = V_{CC}$ or GND	6			±0.1		±1		±1	μΑ
I _{CC}	Quiescent device current	$V_I = V_{CC}$ or GND	6			8		80		160	μΑ
l _{oz}	Three-state leakage current	$V_O = V_{CC}$ or GND	6			±0.5		±5		±10	μΑ
HCT TY	PES .										
V _{IH}	High-level input voltage		4.5 to 5.5	2			2		2		V
V _{IL}	Low-level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
.,	High-level output voltage CMOS loads	I _{OH} = – 20 μA	4.5	4.4			4.4		4.4		٧
V _{OH}	High-level output voltage TTL	I _{OH} = – 4 mA	4.5	3.98			3.84		3.7		V
. ,	Low-level output voltage CMOS	I _{OL} = 20 μA	4.5			0.1		0.1		0.1	V
V _{OL}	Low-level output voltage	I _{OH} = 4 mA	4.5			0.26		0.33		0.4	V
l _l	Input leakage current	V _I = V _{CC} and GND	5.5			±0.1		±1		±1	μA
СС	Quiescent device current	V _I = V _{CC} and GND	5.5			8		80		160	μΑ
oz	Three-state leakage current	$V_O = V_{CC}$ or GND	6			±0.5		±5		±10	μΑ
		An or Bn input held at V _{CC} – 2.1 V	4.5 to 5.5		100	144		180		196	μA
ΔI _{CC} (1)	Additional quiescent device current per input pin	OE input held at V _{CC} – 2.1 V	4.5 to 5.5		100	540		675		735	μΑ
		DIR input held at V _{CC} – 2.1 V	4.5 to 5.5		100	324		405		441	μΑ

⁽¹⁾ For dual-supply systems theoretical worst case (VI = 2.4V, VCC = 5.5V) specification is 1.8mA



5.5 Switching Characteristics

Input t_t = 6ns. Unless otherwise specified, C_L = 50pF⁽²⁾

	DADAMETED	V 00		25°C		-40°C to	85°C	-55°C to 1	25°C	UNIT	
	PARAMETER	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII	
нс тү	PES								<u>'</u>		
		2			110		140		165		
t _{pd}	Propagation delay data to output	4.5			22		28		33	ns	
	J., p. 1	6			19		24		28		
		2			150		190		225		
t _{dis}	Output disable to output	4.5			30		38	-	45	ns	
		6			26		33		38		
		2			150		190		225		
t _{en}	Output enable to output	4.5			30		38		45	ns	
		6			26		33		38		
		2			60		75		90		
t _t	Output transition time	4.5			12		15		18	ns	
		6			10		13		15		
Ci	Input capacitance		10		10		10		10	pF	
C _{io}	Three-state output capacitance				20		20		20	pF	
C_{pd}	Power dissipation capacitance	5		53						pF	
нст т	YPES								<u>'</u>		
t _{pd}	Data to output	4.5			26		33		39	ns	
t _{dis}	Output disable to output	4.5			30		38		45	ns	
t _{en}	Output enable to output	4.5			32		40		48	ns	
t _t	Output transition time	4.5			12		15		18	ns	
C _i	Input capacitance		10		10		10		10	pF	
C _{io}	Three-state output capacitance				20		20		20	pF	
C _{pd}	Power dissipation capacitance ⁽¹⁾ (2)	5		55						pF	

⁽¹⁾ C_{PD} is used to determine the dynamic power consumption, per channel. (2) $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.



6 Parameter Measurement Information

 t_{pd} is the maximum between t_{PLH} and t_{PHL} t_{t} is the maximum between t_{TLH} and t_{THL}

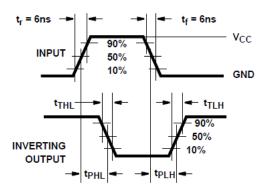


Figure 6-1. HC transition times and propagation delay times, combination logic

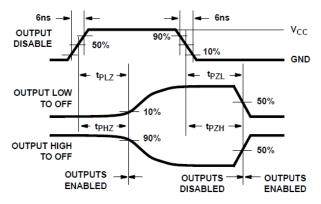


Figure 6-3. HC three-state propagation delay waveform

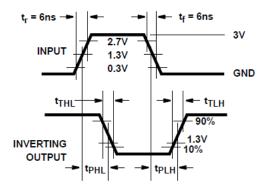


Figure 6-2. HCT transition times and propagation delay times, combination logic

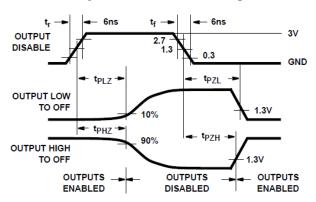


Figure 6-4. HCT three-state propagation delay waveform

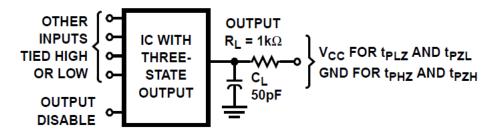


Figure 6-5. HC and HCT three-state propagation delay test circuit

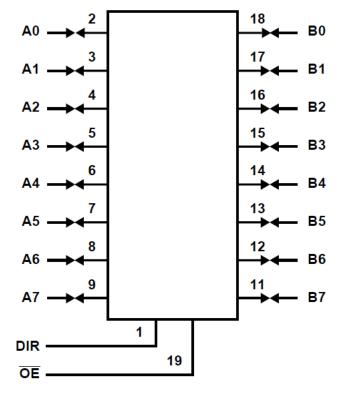
7 Detailed Description

7.1 Overview

The CD54HC245, CD54HCT245, and CD74HC245, CD74HCT245 are high-speed octal three-state bidirectional transceivers intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high-speed operation while driving large bus capacitances. They provide the low power consumption of standard CMOS circuits with speeds and drive capabilities comparable to that of LSTTL circuits.

The CD54HC245, CD54HCT245, CD74HC245 and CD74HCT245 allow data transmission of the B bus or from the B bus to the A bus. The logic level at the direction input (DIR) determines the direction. The output enable input (OE), when high, puts the I/O ports in the high-impedance state.

The HC/HCT245 is similar in operation to the HC/HCT640 and the HC/HCT643.



Functional Block Diagram

7.2 Device Functional Modes

Table 7-1. Truth Table

Control In	puts ⁽¹⁾	
ŌĒ	DIR	Operation
L	L	B Data to A Bus
L	Η	A Data to B Bus
Н	Х	Isolation

(1) H = High Level, L = Low Level, X = Irrelevant



8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
CD54HC245F	Active	Production	CDIP (J) 20	20 TUBE	No	(4) SNPB	N/A for Pkg Type	-55 to 125	CD54HC245F
				·					
CD54HC245F.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC245F
CD54HC245F3A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8408501RA CD54HC245F3A
CD54HC245F3A.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8408501RA CD54HC245F3A
CD54HCT245F	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT245F
CD54HCT245F.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT245F
CD54HCT245F3A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8550601RA CD54HCT245F3A
CD54HCT245F3A.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8550601RA CD54HCT245F3A
CD74HC245E	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC245E
CD74HC245E.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC245E
CD74HC245E.B	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC245E
CD74HC245M	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	-55 to 125	HC245M
CD74HC245M96	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC245M
CD74HC245M96.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC245M
CD74HCT245E	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT245E
CD74HCT245E.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT245E
CD74HCT245EE4	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT245E
CD74HCT245M	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	-55 to 125	HCT245M
CD74HCT245M96	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT245M
CD74HCT245M96.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT245M

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

PACKAGE OPTION ADDENDUM

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- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC245, CD54HCT245, CD74HC245, CD74HCT245:

Catalog: CD74HC245, CD74HCT245

Military: CD54HC245, CD54HCT245

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC245M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HC245M96	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
CD74HCT245M96	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
CD74HCT245M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC245M96	SOIC	DW	20	2000	356.0	356.0	45.0
CD74HC245M96	SOIC	DW	20	2000	356.0	356.0	45.0
CD74HCT245M96	SOIC	DW	20	2000	356.0	356.0	45.0
CD74HCT245M96	SOIC	DW	20	2000	356.0	356.0	45.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC245E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HC245E.A	N	PDIP	20	20	506	13.97	11230	4.32
CD74HC245E.B	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT245E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT245E.A	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT245EE4	N	PDIP	20	20	506	13.97	11230	4.32

14 LEADS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SOIC



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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