







CD54HC73, CD74HC73, CD74HCT73 SCHS134G - FEBRUARY 1998 - REVISED OCTOBER 2022

# CDx4HC73 CD74HCT73 Dual J-K Flip-Flop with Reset Negative-Edge Trigger

#### 1 Features

- Hysteresis on clock inputs for improved noise immunity and increased input rise and fall times
- Asynchronous reset
- Complementary outputs
- Buffered inputs
- Typical  $f_{MAX} = 60 \text{ MHz}$  at  $V_{CC} = 5 \text{ V}$ ,  $C_1 = 15 \text{ pF}, T_A = 25^{\circ}\text{C}$
- Fanout (over temperature range)
  - Standard outputs: 10 LSTTL loads
  - Bus driver outputs: 15 LSTTL loads
- Wide operating temperature range: -55°C to 125°C
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL Logic ICs
- · HC types
  - 2 V to 6V operation
  - $-\;$  High noise immunity:  $N_{IL}$  = 30%,  $N_{IH}$  = 30% of  $V_{CC}$  at  $V_{CC} = 5 V$
- HCT types
  - 4.5 V to 5.5 V operation
  - Direct LSTTL input logic compatibility,  $V_{IL} = 0.8 \text{ V (max)}, V_{IH} = 2 \text{ V (min)}$
  - CMOS input compatibility, I₁ ≤ 1 μA at V<sub>OI</sub>, V<sub>OH</sub>

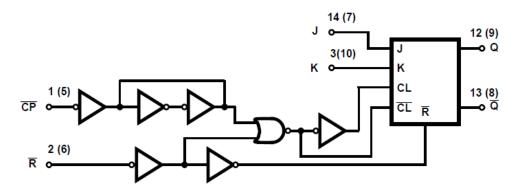
### 2 Description

The 'HC73 and CD74HCT73 utilize silicon gate CMOS technology to achieve operating speeds equivalent to LSTTL parts. They exhibit the low power consumption of standard CMOS integrated circuits, together with the ability to drive 10 LSTTL loads.

#### **Package Information**

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)				
CD74HC73M	SOIC (14)	8.65 mm × 3.90 mm				
CD74HCT73M	SOIC (14)	8.65 mm × 3.90 mm				
CD74HC73E	PDIP (14)	19.31 mm × 6.35 mm				
CD74HCT73E	PDIP (14)	19.31 mm × 6.35 mm				
CD54HC73F	CDIP (14)	19.55 mm × 6.71 mm				

For all available packages, see the orderable addendum at the end of the data sheet.



**Functional Block Diagram** 

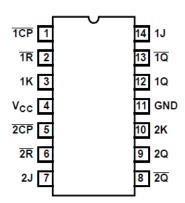


## **Table of Contents**

2 Description	7.2 Functional Block Diagram9
2 Description1	7.3 Device Functional Modes9
	8 Power Supply Recommendations10
4 Pin Configuration and Functions3	9 Layout10
5 Specifications4	9.1 Layout Guidelines10
5.1 Absolute Maximum Ratings <sup>(1)</sup> 4	10 Device and Documentation Support11
5.2 Recommended Operating Conditions4	10.1 Receiving Notification of Documentation Updates 11
5.3 Thermal Information4	10.2 Support Resources11
5.4 Electrical Specifications5	10.3 Trademarks11
5.5 Prerequisite for Switching Specifications6	10.4 Electrostatic Discharge Caution11
5.6 Switching Specifications7	10.5 Glossary11
6 Parameter Measurement Information8	11 Mechanical, Packaging, and Orderable
7 Detailed Description9	Information11
7.1 Overview9	
	rom page numbers in the current version.
Changes from Revision F (January 2022) to Revision	G (October 2022) Page
<ul> <li>Increased RθJA for packages: D (86 to 138.7); N (80</li> </ul>	to 91)4
Changes from Revision E (August 2003 ) to Revision	F (January 2022) Page
Updated the numbering, formatting, tables, figures, a modern data sheet standards	nd cross-references throughout the document to reflect



# **4 Pin Configuration and Functions**



J, N, or D package 14-Pin CDIP, PDIP, or SOIC Top View



## **5 Specifications**

## 5.1 Absolute Maximum Ratings<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		-0.5	7	V
I <sub>IK</sub>	Input diode current	For $V_1 < -0.5 \text{ V}$ or $V_1 > V_{CC} + 0.5 \text{ V}$		± 20	mA
Io	Drain current, per output	For –0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V		± 25	mA
I <sub>OK</sub>	Output diode current	For $V_O < -0.5 \text{ V}$ or $V_O > V_{CC} + 0.5 \text{ V}$		± 20	mA
Io	Output source or sink current per output pin	For $V_O > -0.5 \text{ V}$ or $V_O < V_{CC} + 0.5 \text{ V}$		± 25	mA
Icc	Continuous current through V <sub>CC</sub> or GND	·		± 50	mA
T <sub>J</sub>	Junction temperature			±150	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

<sup>(1)</sup> Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### **5.2 Recommended Operating Conditions**

			MIN	MAX	UNIT
V	Supply voltage range	HC types	2	6	V
V <sub>CC</sub>	Supply voltage range	HCT types	4.5	5.5	V
V <sub>I</sub> , V <sub>O</sub>	Input or output voltage		0	V <sub>CC</sub>	V
		2 V		1000	
t <sub>t</sub>	Input rise and fall time	4.5 V		500	ns
		6 V		400	
T <sub>A</sub>	Temperature range	·	-55	125	°C

#### 5.3 Thermal Information

		D (SOIC)	N (PDIP)	
THERMAL ME	ETRIC	14 PINS	14 PINS	UNIT
R <sub>0JA</sub>	Junction-to-ambient thermal resistance <sup>(1)</sup>	138.7	91	°C/W
R <sub>0JC(top)</sub>	Junction-to-case (top) thermal resistance	93.8	78.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	94.7	70.7	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	49.1	58.6	°C/W
ΨЈВ	Junction-to-board characterization parameter resistance	94.3	70.5	°C/W
R <sub>0JC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application report.



### 5.4 Electrical Specifications

	PARAMETER	TEST	V <sub>CC</sub>		25℃		–40℃ to	85℃	–55℃ to	125℃	UNIT
	PARAMETER	CONDITIONS(2)	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
НС ТҮР	ES										
			2	1.5			1.5		1.5		
$V_{IH}$	High level input voltage		4.5	3.15			3.15		3.15		V
			6	4.2			4.2		4.2		
			2			0.5		0.5		0.5	
$V_{IL}$	Low level input voltage		4.5			1.35		1.35		1.35	V
			6			1.8		1.8		1.8	
		I <sub>OH</sub> = – 20 μA	2	1.9			1.9		1.9		
	High level output voltage	$I_{OH} = -20 \mu A$	4.5	4.4			4.4		4.4		
V <sub>OH</sub>		$I_{OH} = -20 \mu A$	6	5.9			5.9		5.9		V
	High level output voltage	$I_{OH} = -4 \text{ mA}$	4.5	3.98			3.84		3.7		
		$I_{OH} = -5.2 \text{ mA}$	6	5.48			5.34		5.2		
		I <sub>OL</sub> = 20 μA	2			0.1	-	0.1		0.1	
	Low level output voltage	I <sub>OL</sub> = 20 μA	4.5			0.1		0.1		0.1	
V <sub>OL</sub>		I <sub>OL</sub> = 20 μA	6			0.1		0.1		0.1	V
	Low level output voltage	I <sub>OL</sub> = 4 mA	4.5			0.26		0.33		0.4	
	Low level output voltage	I <sub>OL</sub> = 5.2 mA	6			0.26		0.33		0.4	
l <sub>l</sub>	Input leakage current	$V_I = V_{CC}$ or GND	6			±0.1	-	±1		±1	mA
Icc	Supply current	$V_I = V_{CC}$ or GND	6			4		40		80	mA
HCT TY	PES					•				•	
V <sub>IH</sub>	High level input voltage		4.5 to 5.5	2			2		2		V
V <sub>IL</sub>	Low level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
	High level output voltage	I <sub>OH</sub> = – 20 μA	4.5	4.4			4.4		4.4		
V <sub>OH</sub>	High level output voltage	I <sub>OH</sub> = – 4 mA	4.5	3.98			3.84		3.7		V
	Low level output voltage	I <sub>OL</sub> = 20 μA	4.5			0.1		0.1		0.1	
V <sub>OL</sub>	Low level output voltage	I <sub>OL</sub> = 4 mA	4.5			0.26		0.33		0.4	V
lı	Input leakage current	V <sub>I</sub> = V <sub>CC</sub> and GND	5.5			±0.1		±1		±1	μA
СС	Supply current	V <sub>I</sub> = V <sub>CC</sub> and GND	5.5			4	,	40		80	μΑ
ΔI <sub>CC</sub> (1)	Additional supply current per input pin	All inputs held at $V_{CC}$ – 2.1	4.5 to 5.5		100	108		135		147	μΑ

 <sup>(1)</sup> For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4 V, V<sub>CC</sub> = 5.5 V) specification is 1.8 mA.
 (2) V<sub>I</sub> = V<sub>IH</sub> or V<sub>IL</sub>.



## 5.5 Prerequisite for Switching Specifications

	DADAMETED	TEST	V 00		25℃		–40°C to	85℃	–55℃ to	125℃	UNIT
	PARAMETER	CONDITIONS	V <sub>CC</sub> (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
нс тү	PES										
			2	80			100		120		
t <sub>w</sub>	CP pulse width	-C <sub>L</sub> = 50 pF	4.5	16			20		24		ns
			6	14			17		20		
			2	80			100		120		
t <sub>w</sub>	R pulse width	-C <sub>L</sub> = 50 pF	4.5	16			20		24		ns
			6	14			17		20		
			2	80	,		100		120		
t <sub>SU</sub>	Setup time, J, K to CP	C <sub>L</sub> = 50 pF	4.5	16			20		24		ns
			6	14			17		20		
			2	3			3		3		
t <sub>H</sub> Hold time, J, K to $\overline{CP}$	C <sub>L</sub> = 50 pF	4.5	3			3		3		ns	
			6	3			3		3		
			2	80			100		120		
t <sub>REM</sub>	Removal time	-C <sub>L</sub> = 50 pF	4.5	16			20		24		ns
			6	14			17		20		
		0 50 5	2	6			5		4		
	<del>00</del> (	C <sub>L</sub> = 50 pF	4.5	30			25		20		
$f_{MAX}$	CP frequency	C <sub>L</sub> = 15 pF	5	,	60		,				MHz
		C <sub>L</sub> = 50 pF	6	35			29		23		
нст т	YPES										
t <sub>w</sub>	CP pulse width	C <sub>L</sub> = 50 pF	4.5	16			20		24		ns
t <sub>w</sub>	R pulse width	C <sub>L</sub> = 50 pF	4.5	18			23		27		ns
t <sub>su</sub>	Setup time, J, K to CP	C <sub>L</sub> = 50 pF	4.5	16			20		24		ns
t <sub>H</sub>	Hold time, J, K to CP	C <sub>L</sub> = 50 pF	4.5	3			3		3		ns
t <sub>REM</sub>	Removal time	C <sub>L</sub> = 50 pF	4.5	12			15		18		ns
	<u>OD</u> 6	C <sub>L</sub> = 50 pF	4.5	30			25		20		
f <sub>MAX</sub>	CP frequency	C <sub>L</sub> = 15 pF	5		60						MHz



## 5.6 Switching Specifications

Input,  $t_r$ ,  $t_f = 6$  ns

	PARAMETER	TEST	V <sub>CC</sub> (V)		25℃		-40°C	to 85℃	−55° 125		UNIT	
		CONDITIONS	00 ( )	MIN	TYP	MAX	MIN	MAX	MIN	MAX		
HC TY	PES		1					'				
		C <sub>L</sub> = 50 pF	2			160		200		240		
t <sub>PLH</sub> ,	Propagation delay,	C <sub>L</sub> = 50 pr	4.5			32		40		48	20	
$t_{PHL}$	CP to Q	C <sub>L</sub> = 15 pF	5		13						ns	
		C <sub>L</sub> = 50 pF	6			28		34		41		
		C <sub>L</sub> = 50 pF	2			160		200		240		
t <sub>PLH</sub> ,	Propagation delay,	C <sub>L</sub> = 50 pr	4.5			32		40		48	20	
$t_{PHL}$	CP to Q	C <sub>L</sub> = 15 pF	5		13						ns	
		C <sub>L</sub> = 50 pF	6			28		34		41		
		C <sub>L</sub> = 50 pF	2			145		180		220		
t <sub>PLH</sub> ,	Propagation delay,	C <sub>L</sub> = 50 pr	4.5			29		36		44	20	
t <sub>PHL</sub>		C <sub>L</sub> = 15 pF	5		12						ns	
		C <sub>L</sub> = 50 pF	6			25		31		38		
			2			75		95	18	110		
t <sub>TLH</sub> , t <sub>THL</sub>	Output transition time	C <sub>L</sub> = 50 pF	4.5			15		19		22	ns	
THL			6			13		16		19		
Cı	Input capacitance					10		10		10	pF	
C <sub>PD</sub>	Power dissipation capacitance <sup>(1)</sup> (2)		5		28						pF	
нст т	YPES		'									
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation delay,  CP to Q	C <sub>L</sub> = 50 pF	4.5			38		48		57	ns	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation delay,  CP to Q	C <sub>L</sub> = 50 pF	4.5			36		45		54	ns	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation delay, R to Q, Q	C <sub>L</sub> = 50 pF	4.5			34		43		51	ns	
t <sub>TLH</sub> , t <sub>THL</sub>	Output transition time	C <sub>L</sub> = 50 pF	4.5			15		19		22	ns	
C <sub>I</sub>	Input capacitance					10		10		10	pF	
C <sub>PD</sub>	Power dissipation capacitance <sup>(1)</sup> (2)		5		28						pF	

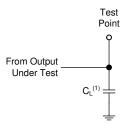
<sup>(1)</sup>  $C_{PD}$  is used to determine the dynamic power consumption, per flip-flop. (2)  $P_D = C_{PD} \ V_{CC} \ ^2 f_i + \sum C_L \ V_{CC} \ ^2 f_o$  where  $f_i$  = input frequency,  $f_o$  = output frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.

#### **6 Parameter Measurement Information**

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_t < 2.5 \text{ ns}$ .

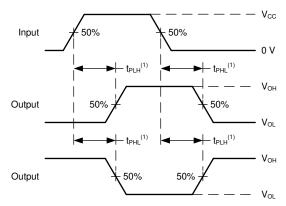
For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



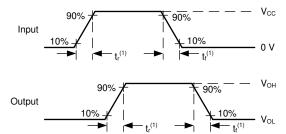
(1) C<sub>L</sub> includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs



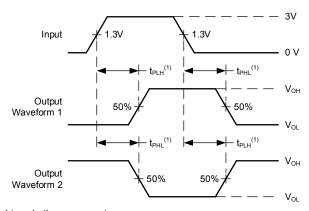
(1) The greater between  $t_{\text{PLH}}$  and  $t_{\text{PHL}}$  is the same as  $t_{\text{pd}}$ .

Figure 6-2. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs



(1) The greater between t<sub>r</sub> and t<sub>f</sub> is the same as t<sub>t</sub>.

Figure 6-3. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs



(1) The greater between  $t_{\text{PLH}}$  and  $t_{\text{PHL}}$  is the same as  $t_{\text{pd}}.$ 

Figure 6-4. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs



## 7 Detailed Description

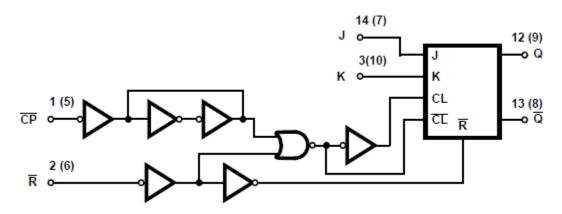
### 7.1 Overview

The 'HC73 and CD74HCT73 utilize silicon gate CMOS technology to achieve operating speeds equivalent to LSTTL parts. They exhibit the low power consumption of standard CMOS integrated circuits, together with the ability to drive 10 LSTTL loads

These flip-flops have independent J, K, Reset and Clock inputs and Q and  $\overline{\mathbb{Q}}$  outputs. They change state on the negative-going transition of the clock pulse. Reset is accomplished asynchronously by a low level input. This device is functionally identical to the HC/HCT107 but differs in terminal assignment and in some parametric limits.

The HCT logic family is functionally as well as pin compatible with the standard LS logic family

#### 7.2 Functional Block Diagram



#### 7.3 Device Functional Modes

Table 7-1. Truth Table<sup>(1)</sup>

	INP	UTS		OUTPUTS			
R	CP	J	K	Q	Q		
L	Х	Х	X	L	Н		
Н	<b>↓</b>	L	L	No change			
Н	<b>↓</b>	Н	L	Н	L		
Н	<b>↓</b>	L	Н	L	Н		
Н	<b>↓</b>	Н	Н	Toggle			
Н	Н	X	X	No change			

(1) H = high level (steady state), L = low level (steady state), X = irrelevant, ↓ = high-to-low transition



### 8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V<sub>CC</sub> terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

### 9 Layout

#### 9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.



### 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

#### 10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 10.2 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### 10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

#### 10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 10.5 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

### 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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31-Oct-2025

#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-8515301CA	Active	Production	CDIP (J)   14	25   TUBE	No	(4) SNPB	N/A for Pkg Type	-55 to 125	5962-8515301CA CD54HC73F3A
CD54HC73F	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC73F
CD54HC73F.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC73F
CD54HC73F3A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8515301CA CD54HC73F3A
CD54HC73F3A.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8515301CA CD54HC73F3A
CD74HC73E	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC73E
CD74HC73E.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC73E
CD74HC73M	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-55 to 125	HC73M
CD74HC73M96	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-55 to 125	HC73M
CD74HC73M96.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC73M
CD74HC73MT	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-55 to 125	HC73M
CD74HCT73E	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT73E
CD74HCT73E.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT73E
CD74HCT73M	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-55 to 125	HCT73M
CD74HCT73M96	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCT73M
CD74HCT73M96.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCT73M

 $<sup>^{\</sup>mbox{(1)}}$  Status: For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## **PACKAGE OPTION ADDENDUM**

www.ti.com 31-Oct-2025

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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#### OTHER QUALIFIED VERSIONS OF CD54HC73, CD74HC73:

Catalog: CD74HC73

Military: CD54HC73

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

# **PACKAGE MATERIALS INFORMATION**

www.ti.com 31-Oct-2025

### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC73M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HCT73M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

www.ti.com 31-Oct-2025



#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC73M96	SOIC	D	14	2500	353.0	353.0	32.0
CD74HCT73M96	SOIC	D	14	2500	353.0	353.0	32.0

# **PACKAGE MATERIALS INFORMATION**

www.ti.com 31-Oct-2025

### **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC73E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC73E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT73E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT73E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT73E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT73E.A	N	PDIP	14	25	506	13.97	11230	4.32

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4040083-5/G





CERAMIC DUAL IN LINE PACKAGE



#### NOTES:

- 1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This package is hermitically sealed with a ceramic lid using glass frit.
- His package is remitted by sealed with a ceramic its using glass mit.
   Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
   Falls within MIL-STD-1835 and GDIP1-T14.



CERAMIC DUAL IN LINE PACKAGE



# N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SMALL OUTLINE INTEGRATED CIRCUIT



#### NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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