CDx4HC173, CDx4HCT173 High-Speed CMOS Logic Quad D-Type Flip-Flop, Three-State

1 Features

- Three-state buffered outputs
- Gated input and output enables
- Fanout (over temperature range)
  - Standard outputs : 10 LSTTL loads
  - Bus driver outputs : 15 LSTTL loads
- Wide Operating Temperature Range : -55°C to 125°C
- Balanced propagation delay and transition times
- Significant power and reduction compared to LSTTL logic ICs
- HC types
  - 2 V to 6 V operation
  - High noise immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5 V
- HCT types
  - 4.5 V to 5.5 V Operation
  - Direct LSTTL input logic compatibility, V_{IL}= 0.8 V (Max), V_{IH} = 2 V (Min)
  - CMOS input compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}

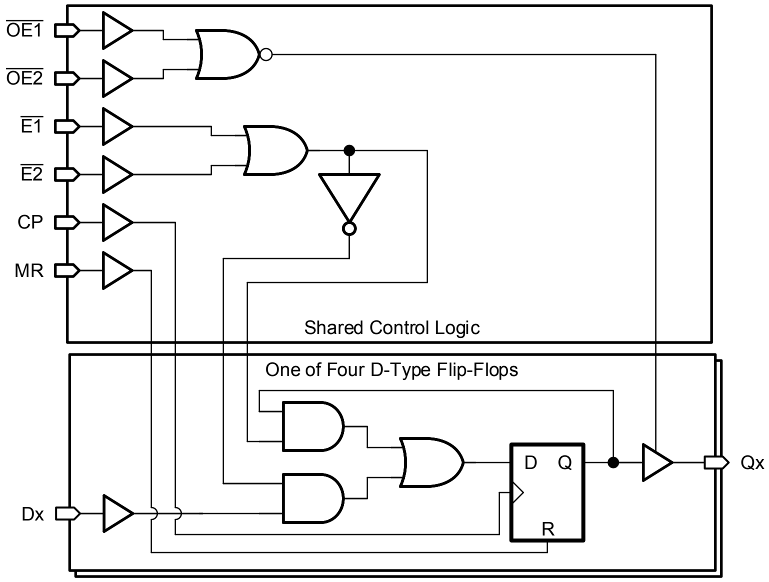
2 Description

The CDx4HC173 and CDx4HCT173 contains four independent D-type flip-flops with shared clock (CP), reset (MR), and data enable ($\overline{E1}$, $\overline{E2}$) pins.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
CD54HC173F	CDIP (16)	21.34 mm × 6.92 mm
CD54HCT173F3A	CDIP (16)	21.34 mm × 6.92 mm
CD74HC173E	PDIP (16)	19.31mm × 6.35 mm
CD74HCT173E	PDIP (16)	19.31mm × 6.35 mm
CD74HC173M	SOIC (16)	9.90 mm × 3.90 mm
CD74HCT173M	SOIC (16)	9.90 mm × 3.90 mm
CD74HC173PW	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all packages see the orderable addendum at the end of the data sheet..



Functional Block Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (October 2003) to Revision F (March 2022)	**Page**
• Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards	1

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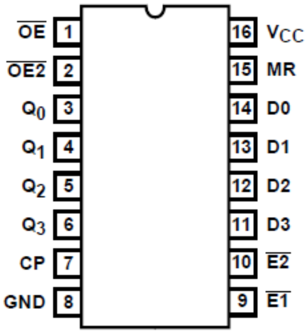
4 Pin Configuration and Functions



J, N, D, or PW Package
16-Pin CDIP, PDIP, SOIC, or TSSOP
Top View

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input diode current(2)	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V		±20	mA
I_{OK}	Output diode current(2)	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V		±20	mA
I_O	Output source or sink current per output pin	$V_O > –0.5$ V or $V_O < V_{CC} + 0.5$ V		±25	mA
	Continuous current through V_{CC} or GND			±70	mA
T_J	Junction temperature			150	°C
	Lead temperature (soldering 10s) (SOIC - lead tips only)			300	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage range	HC types	2	6	V
		HCT types	4.5	5.5	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
t_t	Input rise and fall time	V_{CC} = 2V		1000	ns
		V_{CC} = 4.5V		500	
		V_{CC} = 6V		400	
T_A	Temperature range		-55	125	°C

5.3 Thermal Information

THERMAL METRIC		N (PDIP)	D (SOIC)	NS (SOP)	PW (TSSOP)	UNIT
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	67	73	64	108	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report

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5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS(1)	V_{CC}	25°C			–40°C to 85°C		–55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V_{IH}	High-level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		V
			6	4.2			4.2		4.2		V
V_{IL}	Low-level input voltage		2			0.5		0.5		0.5	V
			4.5			1.35		1.35		1.35	V
			6			1.8		1.8		1.8	V
V_{OH}	High-level output voltage CMOS loads	I_{OH} = – 20μA	2	1.9			1.9		1.9		V
		I_{OH} = – 20μA	4.5	4.4			4.4		4.4		V
		I_{OH} = – 20μA	6	5.9			5.9		5.9		V
	High-level output voltage TTL loads	I_{OH} = – 6mA	4.5	3.98			3.84		3.7		V
		I_{OH} = – 7.8mA	6	5.48			5.34		5.2		V
V_{OL}	Low-level output voltage CMOS loads	I_{OL} = 20μA	2			0.1		0.1		0.1	V
		I_{OL} = 20μA	4.5			0.1		0.1		0.1	V
		I_{OL} = 20μA	6			0.1		0.1		0.1	V
	Low-level output voltage TTL loads	I_{OL} = 6mA	4.5			0.26		0.33		0.4	V
		I_{OL} = 7.8mA	6			0.26		0.33		0.4	V
I_I	Input leakage current	V_{CC} or GND	6			±0.1		±1		±1	μA
I_{CC}	Supply current	V_{CC} or GND	6			8		80		160	μA
I_{OZ}	Three-state leakage current		6			±0.5		±0.5		±10	μA
HCT TYPES											
V_{IH}	High-level input voltage		4.5 to 5.5	2			2		2		V
V_{IL}	Low-level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	High-level output voltage CMOS loads	I_{OH} = – 20μA	4.5	4.4			4.4		4.4		V
	High-level output voltage TTL loads	I_{OH} = – 6mA	4.5	3.98			3.84		3.7		V
V_{OL}	Low-level output voltage CMOS loads	I_{OL} = 20μA	4.5			0.1		0.1		0.1	V
	Low-level output voltage TTL loads	I_{OL} = 6mA	4.5			0.26		0.33		0.4	V
I_I	Input leakage current	V_{CC} and GND	5.5			±0.1		±1		±1	μA
I_{CC}	Supply Current	V_{CC} and GND	5.5			8		80		160	μA
ΔI_{CC} (2) (3)	Additional supply current per input pin	One of D0-D3	4.5 to 5.5		15	54		67.5		73.5	μA
		One of $\overline{E1}$ and $\overline{E2}$	4.5 to 5.5		15	54		67.5		73.5	μA
		CP	4.5 to 5.5		25	90		112.5		122.5	μA
		MR	4.5 to 5.5		20	72		90		98	μA
		One of $\overline{OE1}$ and $\overline{OE2}$	4.5 to 5.5		50	180		225		245	μA

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PARAMETER		TEST CONDITIONS(1)	V_{CC}	25°C			–40°C to 85°C		–55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
I_{OZ}	Three-state leakage current		5.5			±0.5		±5.0		±10	µA

(1) $V_I = V_{IH}$ or V_{IL}, unless otherwise noted.
(2) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.
(3) Inputs held at V_{CC} – 2.1.

5.5 Switching Characteristics

Input t_t = 6ns. Unless otherwise specified, C_L = 50pF

PARAMETER		V_{CC}(V)	25°C		-40°C to 85°C	-55°C to 125°C	UNIT
			TYP	MAX	MAX	MAX	
HC TYPES							
t_{pd}	Propagation delay, clock to output	2		200	250	300	ns
		4.5	17(1)	40	50	60	
		6		34	43	51	
t_{pd}	Propagation delay, MR to output	2		175	220	265	ns
		4.5	12(1)	35	44	53	
		6		30	37	45	
t_{pd}	Propagation delay output enable to Q (Figure 6)	2		150	190	225	ns
		4.5	12(1)	30	38	45	
		6		26	33	38	
t_t	Output transition times	2		60	75	90	ns
		4.5		12	15	18	
		6		10	13	15	
f_{MAX}	Maximum clock frequency	5	60(1)				MHz
C_i	Input capacitance			10	10	10	pF
C_O	Three-state output capacitance			10	10	10	pF
C_{pd} (2) (3)	Power dissipation capacitance	5	29				pF
HCT TYPES							
t_{pd}	Propagation delay, clock to output	4.5	17(1)	40	50	60	ns
t_{pd}	Propagation delay, MR to output	4.5	18(1)	44	55	66	ns
t_{pd}	Propagation delay output enable to Q (Figure 6)	2		150	190	225	ns
		4.5	14(1)	30	38	45	
		6		26	33	38	
t_t	Output transition times	4.5		15	19	22	ns
f_{MAX}	Maximum clock frequency	5	60(1)				MHz
C_i	Input capacitance			10	10	10	pF
C_{pd} (2) (3)	Power dissipation capacitance	5	34				pF

(1) Typical value tested at 5V, C_L = 15pF.
(2) C_{PD} is used to determine th edynamic power consumption, per package.
(3) $P_D = V_{CC}{}^{2}f_i + \Sigma (C_L V_{CC}{}^{2} + f_O)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

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5.6 Prerequisite For Switching Characteristics

PARAMETER		V_{CC}(V)	25°C		-40°C to 85°C		-55°C to 125°C		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
HC TYPES									
f_{MAX}	Maximum clock frequency	2	6		5		4		MHz
		4.5	30		24		20		
		6	35		28		24		
t_W	MR pulse width	2	80		100		120		ns
		4.5	16		20		24		
		6	14		17		20		
t_W	Clock pulse width	2	80		100		120		ns
		4.5	16		20		24		
		6	14		17		20		
t_{SU}	Set-up time, data to clock and $\overline{E}$ to clock	2	60		75		90		ns
		4.5	12		15		18		
		6	10		13		15		
t_H	Hold time, data to clock	2	3		3		3		ns
		4.5	3		3		3		
		6	3		3		3		
t_H	Hold time, $\overline{E}$ to clock	2	0		0		0		ns
		4.5	0		0		0		
		6	0		0		0		
t_{REM}	Removal time, MR to clock	2	60		75		90		ns
		4.5	12		15		18		
		6	10		13		15		
HCT TYPES									
f_{MAX}	Maximum clock frequency	4.5	20		16		13		MHz
t_Wt_W	MR pulse width	4.5	15		19		22		ns
t_W	Clock pulse width	4.5	25		31		38		ns
t_{SU}	Set-up Time, $\overline{E}$ to clock	4.5	12		15		18		ns
t_{SU}	Set-up time, data to clock	4.5	18		23		27		ns
t_H	Hold time, data to clock	4.5	0		0		0		ns
t_H	Hold time, $\overline{E}$ to clock	4.5	0		0		0		ns
t_{REM}	Removal time, MR to clock	4.5	12		15		18		ns

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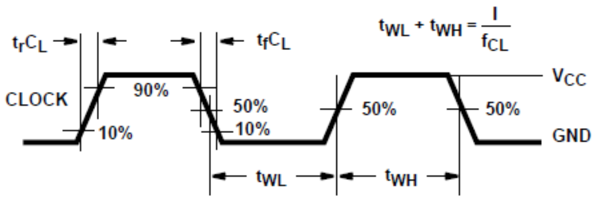
6 Parameter Measurement Information

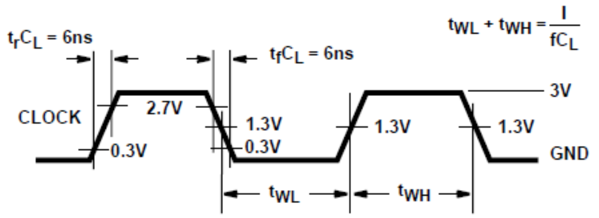
t_{PD} is the maximum between t_{PLH} and t_{PHL}

t_t is the maximum between t_{TLH} and t_{THL}



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX}, input duty cycle = 50%

Figure 6-1. HC clock pulse rise and fall times and pulse width



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. FOr f_{MAX}, input duty cycle = 50%

Figure 6-2. HCT clock pulse rise and fall times and pulse width

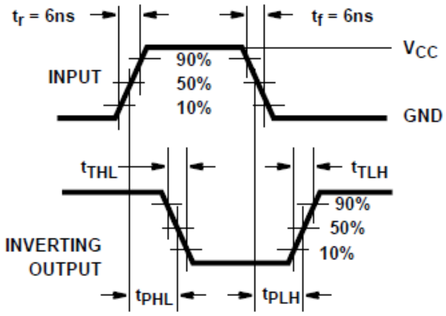


Figure 6-3. HC and HCU transition times and propagation delay times, combination logic

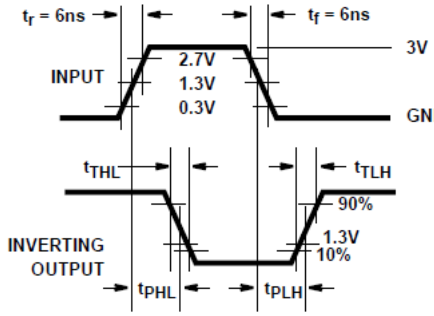


Figure 6-4. HCT transition times and propagation delay times, combination logic

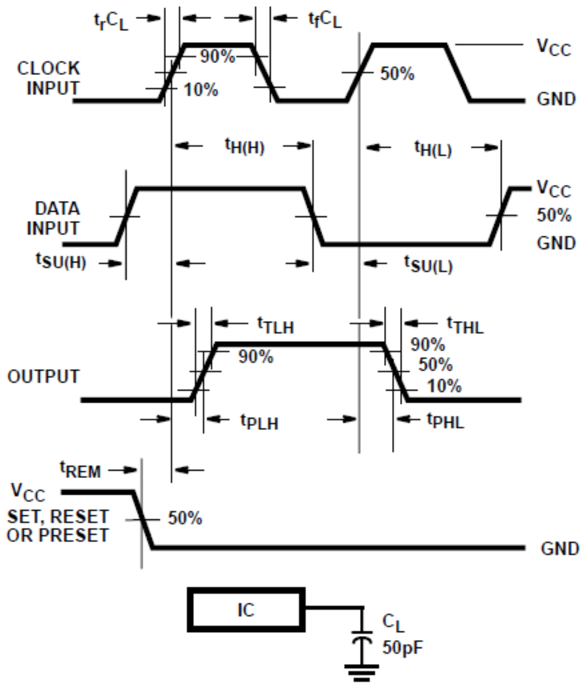


Figure 6-5. HC setup times, hold times, removal time, and propagation delay times for edge triggered sequential logic circuits

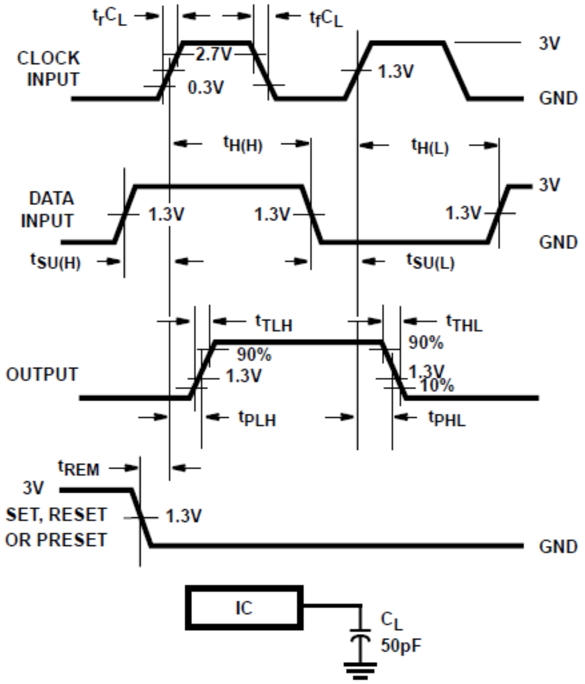


Figure 6-6. HCT setup times, hold times, removal time, and propagation delay times for edge triggered sequential logic circuits

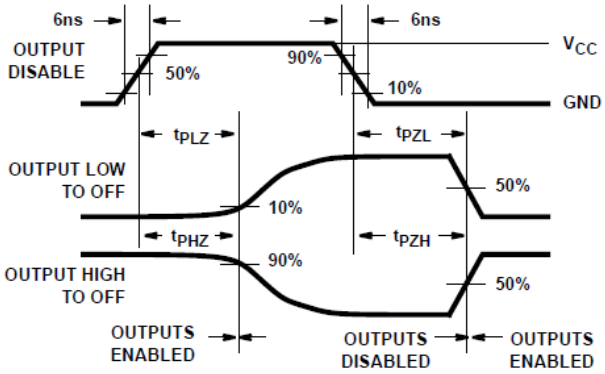


Figure 6-7. HC three-state propagation delay waveform

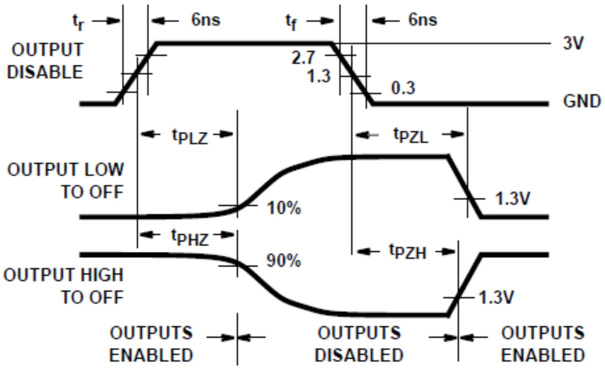
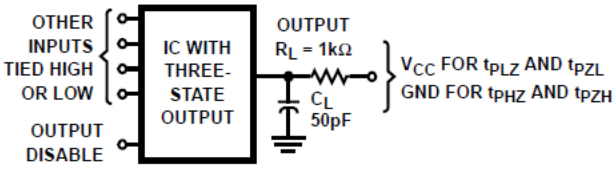


Figure 6-8. HCT three-state propagation delay waveform



NOTE: Opend drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output R_L = 1kΩ to V_{CC}, C_L = 50pF

Figure 6-9. HC and HCT three-state propagation delay test circuit

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7 Detailed Description

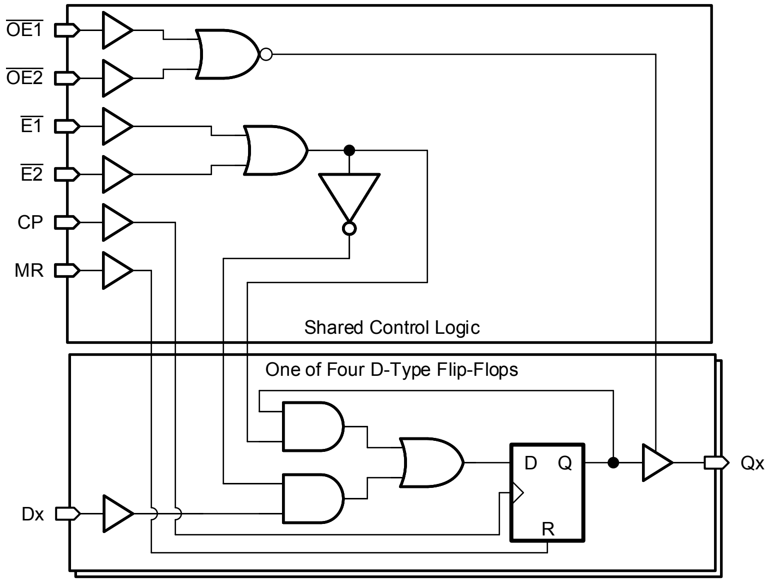
7.1 Overview

The CDx4HC173 or CDx4HCT173 high speed three-state quad Dtype flip-flops are fabricated with silicon gate CMOS technology. They possess the low power consumption of standard CMOS Integrated circuits, and can operate at speeds comparable to the equivalent low power Schottky devices. The buffered outputs can drive 15 LSTTL loads. The large output drive capability and three-state feature make these parts ideally suited for interfacing with bus lines in bus oriented systems

The four D-type flip-flops operate synchronously from a common clock. The outputs are in the three-state mode when either of the two output disable pins are at the logic “1” level. The input ENABLES allow the flip-flops to remain in their present states without having to disrupt the clock If either of the 2 input ENABLES are taken to a logic “1” level, the Q outputs are fed back to the inputs, forcing the flip-flops to remain in the same state. Reset is enabled by taking the RESET (MR) input to a logic “1” level. The data outputs change state on the positive going edge of the clock.

The ’HCT173 logic family is functionally, as well as pin compatible with the standard LS logic family.

7.2 Functional Block Diagram



7.3 Device Functional Modes

Table 7-1. Truth Table(1)(2)

INPUTS				DATA	OUTPUT
MR	CP	DATA ENABLE			
		$\overline{\text{E1}}$	$\overline{\text{E2}}$	D	Q_n
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

(1) H = High voltage level. L = Low voltage level. X = Irrelevant. ↑ = Transition from low to high level. Q_0 = Level before the indicated steady-state input conditions were established.

(2) When either OE1 or OE2 (or both) is (are) high, the output is disabled to the high-impedance stat, however, sequential operation of the flip-flops is not affected.

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8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

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10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8682501EA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8682501EA CD54HC173F3A
5962-8875901EA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8875901EA CD54HCT173F3A
CD54HC173F	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC173F
CD54HC173F.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC173F
CD54HC173F3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8682501EA CD54HC173F3A
CD54HC173F3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8682501EA CD54HC173F3A
CD54HCT173F3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8875901EA CD54HCT173F3A
CD54HCT173F3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8875901EA CD54HCT173F3A
CD74HC173E	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC173E
CD74HC173E.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC173E
CD74HC173M	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HC173M
CD74HC173M96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC173M
CD74HC173M96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC173M
CD74HC173PW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-55 to 125	HJ173
CD74HC173PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	HJ173
CD74HC173PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ173
CD74HCT173E	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT173E
CD74HCT173E.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT173E
CD74HCT173M	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HCT173M
CD74HCT173M96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT173M
CD74HCT173M96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT173M

(1) **Status:** For more details on status, see our product life cycle.

[2] **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC173, CD54HCT173, CD74HC173, CD74HCT173 :

- Catalog : CD74HC173, CD74HCT173

- Military : CD54HC173, CD54HCT173

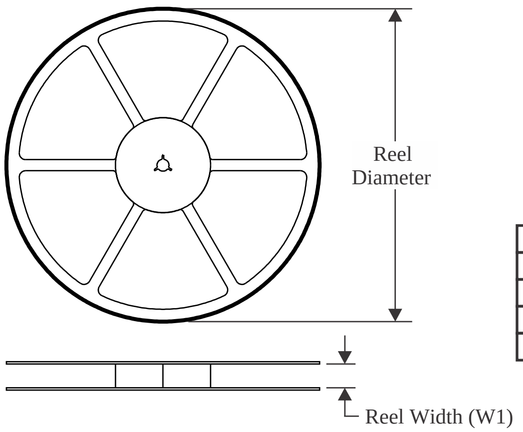
NOTE: Qualified Version Definitions:

  - Catalog - TI's standard catalog product

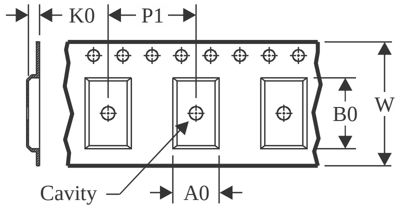
  - Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

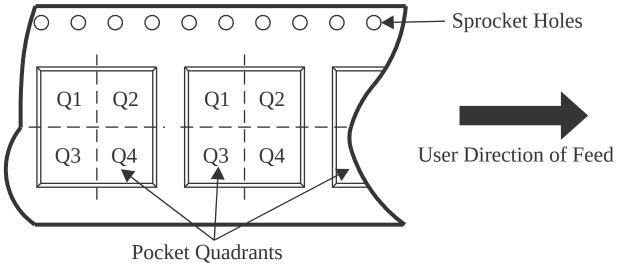


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

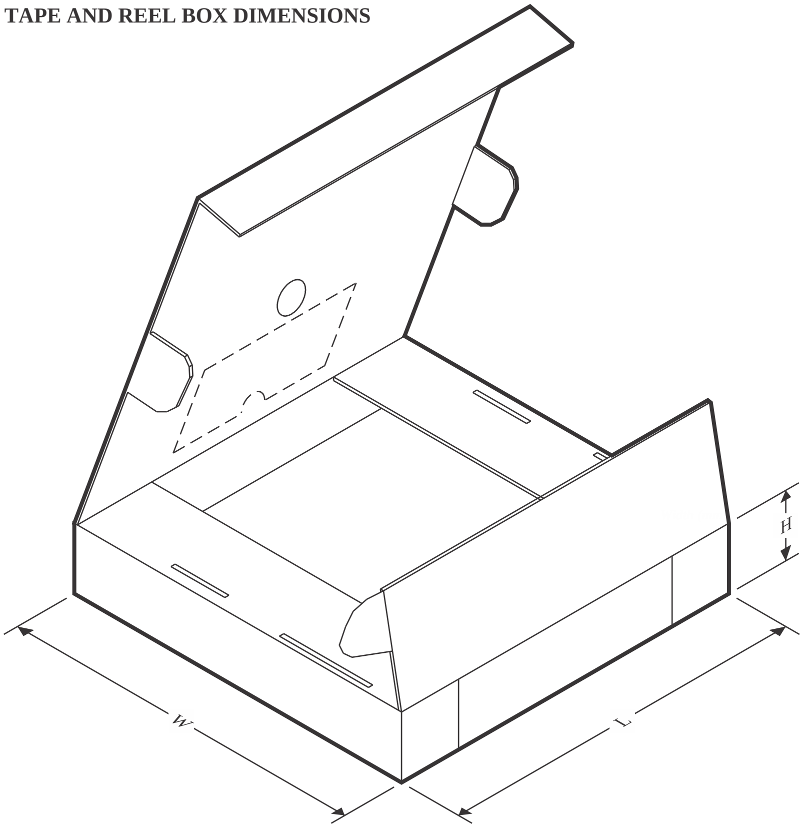
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC173M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC173PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HCT173M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

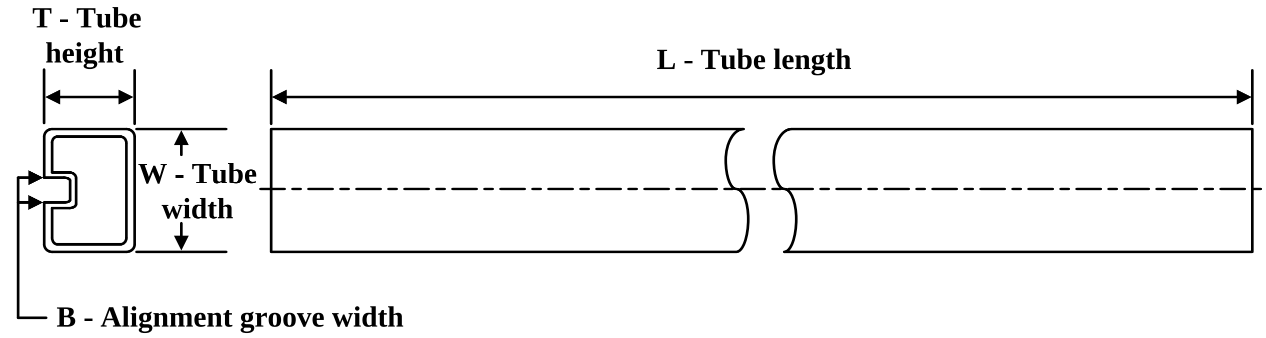
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC173M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74HC173PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
CD74HCT173M96	SOIC	D	16	2500	340.5	336.1	32.0

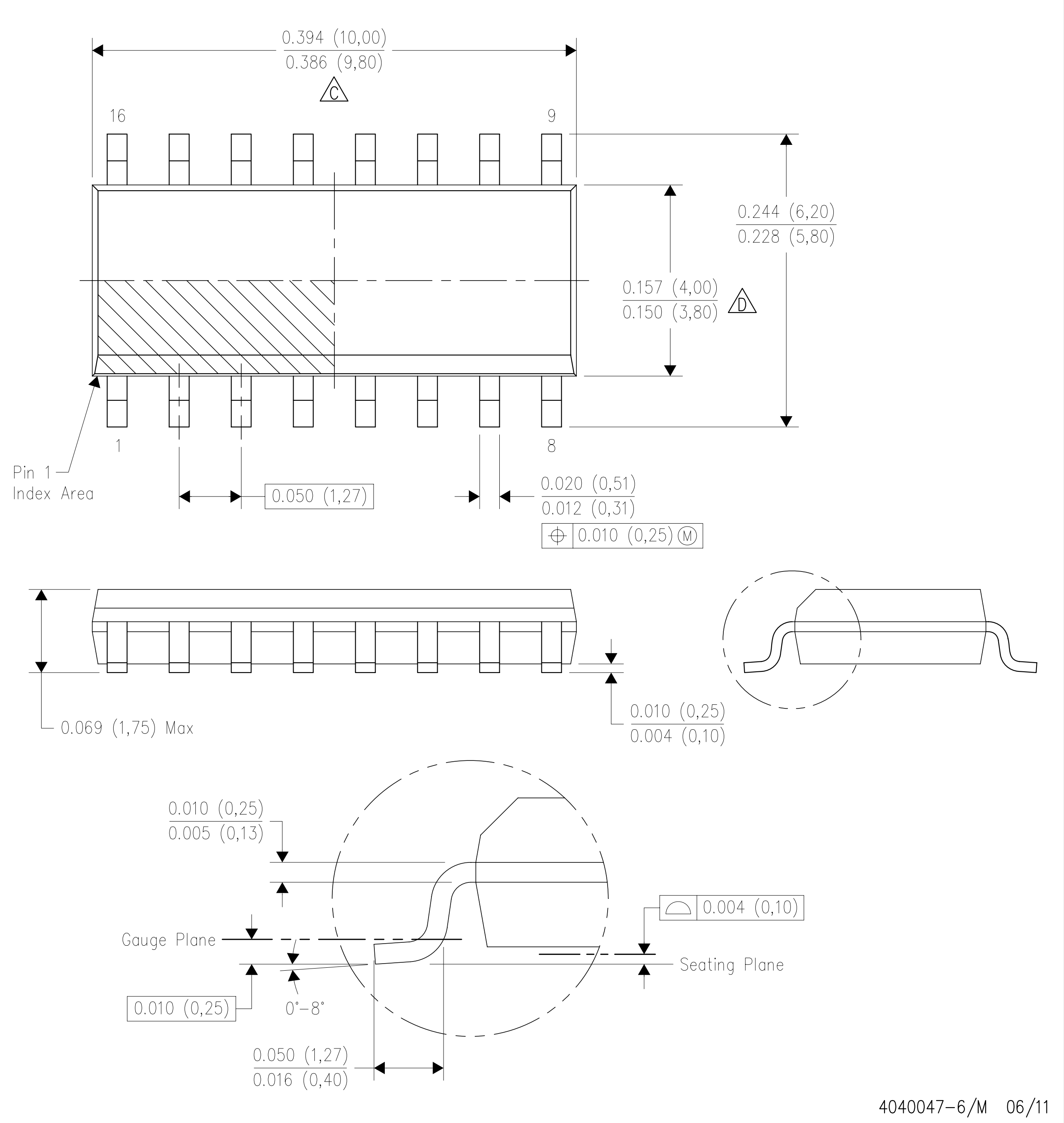
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC173E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC173E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC173E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC173E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT173E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT173E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT173E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT173E.A	N	PDIP	16	25	506	13.97	11230	4.32

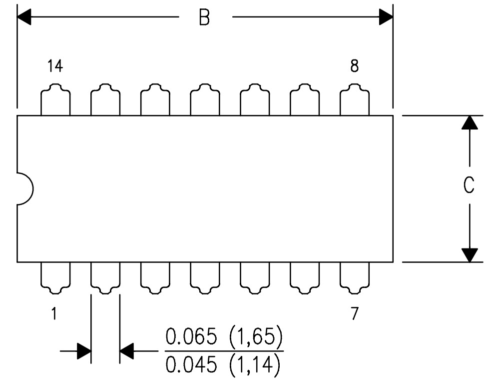
D (R–PDSO–G16) PLASTIC SMALL OUTLINE



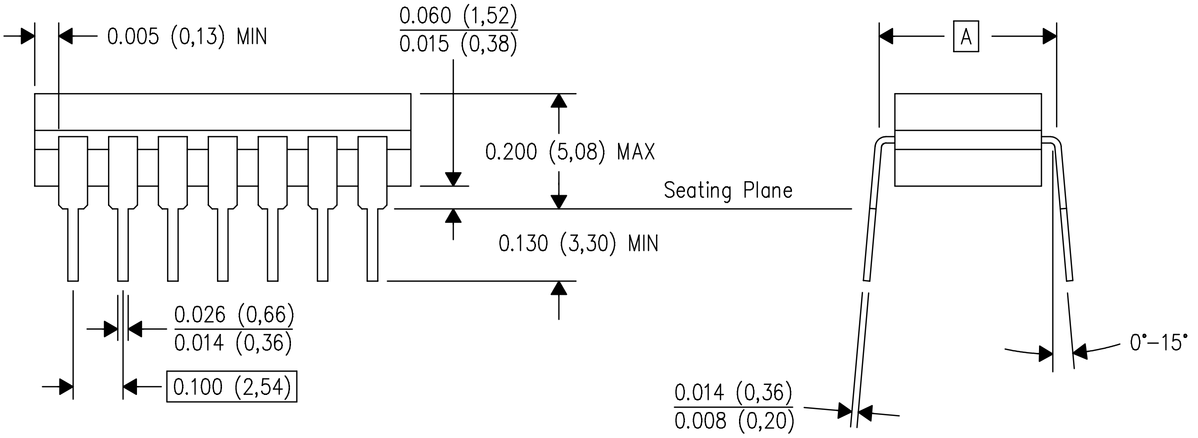
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

J (R-GDIP-T**) CERAMIC DUAL IN-LINE PACKAGE

14 LEADS SHOWN

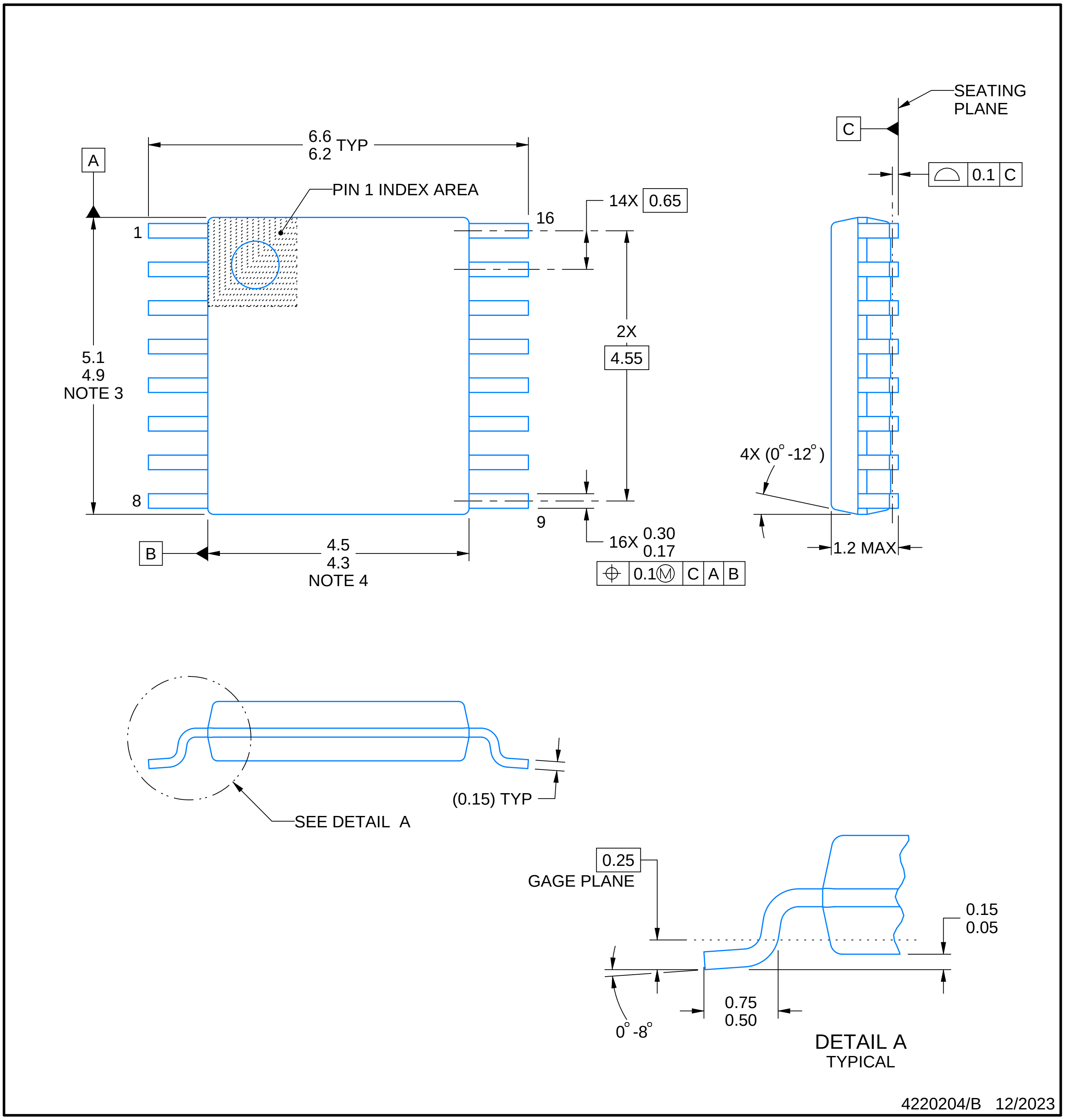


DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



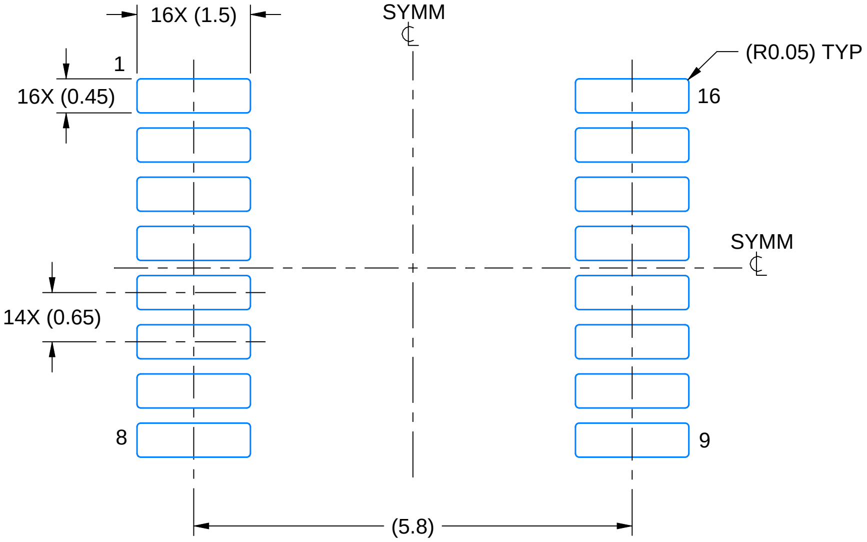
4040083/F 03/03

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

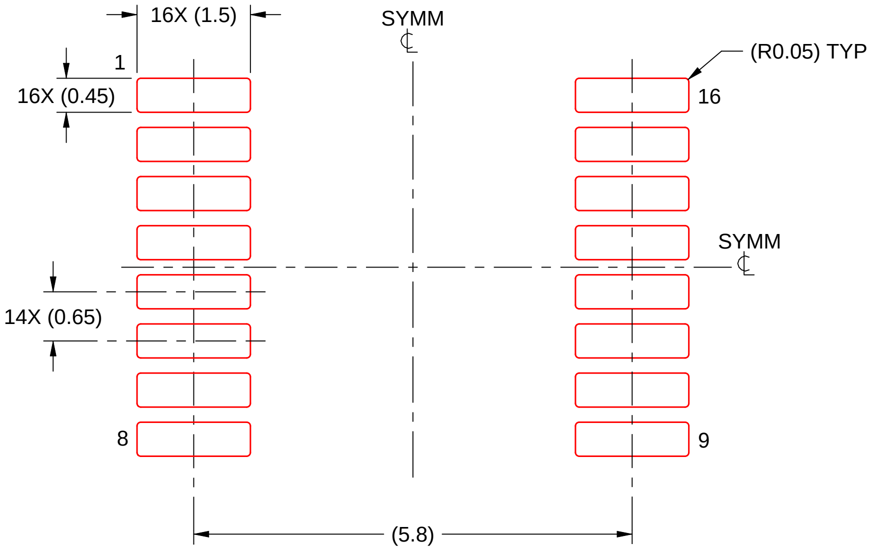
NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

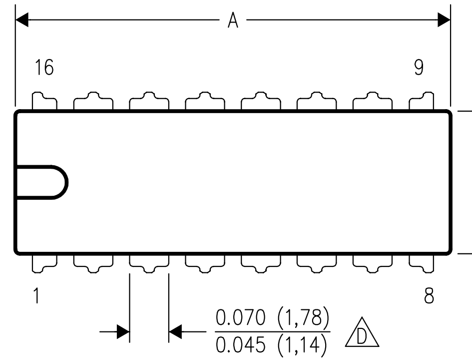
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

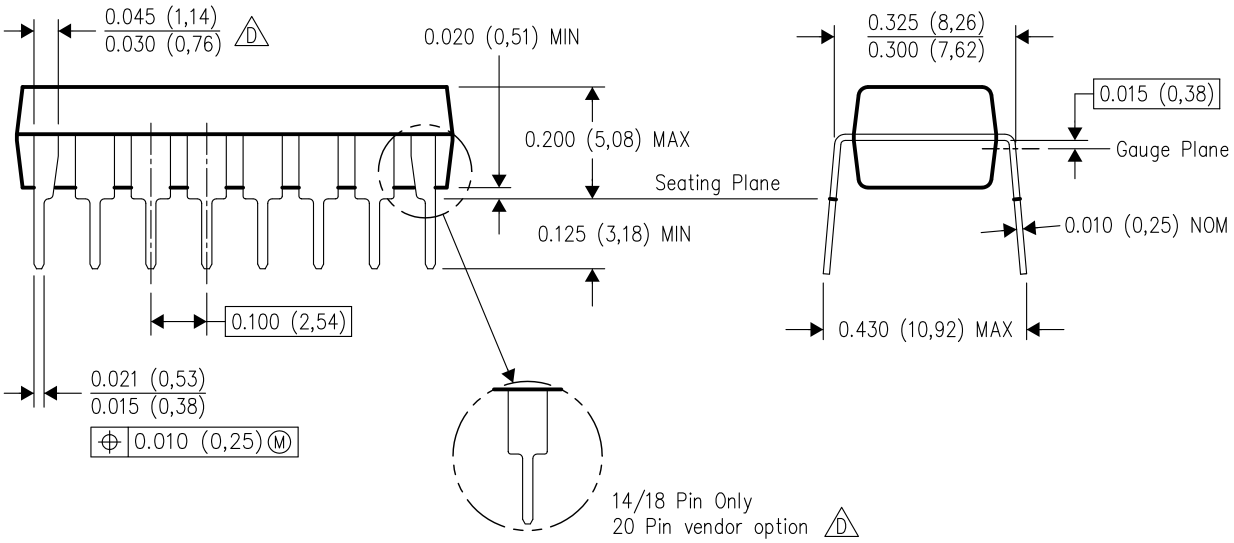
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
△C MS–001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
△C Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
△D The 20 pin end lead shoulder width is a vendor option, either half or full width.

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