

Data sheet acquired from Harris Semiconductor SCHS148D

CD54HC139, CD74HC139, CD54HCT139

High-Speed CMOS Logic Dual 2- to 4-Line Decoder/Demultiplexer

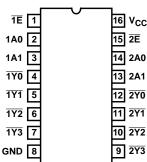
September 1997 - Revised October 2003

Features

- Multifunction Capability
 - Binary to 1 of 4 Decoders or 1 to 4 Line Demultiplexer
- Active Low Mutually Exclusive Outputs
- Fanout (Over Temperature Range)
 - Standard Outputs...... 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility,
 V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)
 - CMOS Input Compatibility, $I_I \leq 1 \mu \text{A}$ at $V_{\mbox{\scriptsize OL}},\,V_{\mbox{\scriptsize OH}}$
- Memory Decoding, Data Routing, Code Conversion

Pinout

CD54HC139, CD54HCT139 (CERDIP) CD74HC139, CD74HCT139 (PDIP, SOIC) TOP VIEW



Description

The 'HC139 and 'HCT139 devices contain two independent binary to one of four decoders each with a single active low enable input ($\overline{1E}$ or $\overline{2E}$). Data on the select inputs (1A0 and 1A1 or 2A0 and 2A1) cause one of the four normally high outputs to go low.

If the enable input is high all four outputs remain high. For demultiplexer operation the enable input is the data input. The enable input also functions as a chip select when these devices are cascaded. This device is functionally the same as the CD4556B and is pin compatible with it.

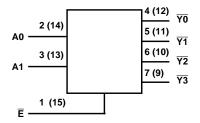
The outputs of these devices can drive 10 low power Schottky TTL equivalent loads. The HCT logic family is functionally as well as pin equivalent to the LS logic family.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC139F3A	-55 to 125	16 Ld CERDIP
CD54HCT139F3A	-55 to 125	16 Ld CERDIP
CD74HC139E	-55 to 125	16 Ld PDIP
CD74HC139M	-55 to 125	16 Ld SOIC
CD74HC139MT	-55 to 125	16 Ld SOIC
CD74HC139M96	-55 to 125	16 Ld SOIC
CD74HCT139E	-55 to 125	16 Ld PDIP
CD74HCT139M	-55 to 125	16 Ld SOIC
CD74HCT139MT	-55 to 125	16 Ld SOIC
CD74HCT139M96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

Functional Diagram

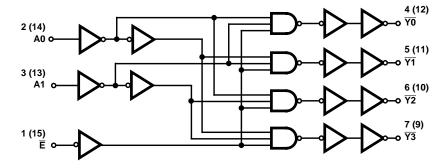


TRUTH TABLE

INPUTS	ENABLE	SELECT	OUTPUTS							
Ē	A1	Α0	<u></u> 73	Y2	<u>¥1</u>	<u></u> 70				
0	0	0	1	1	1	0				
0	0	1	1	1	0	1				
0	1	0	1	0	1	1				
0	1	1	0	1	1	1				
1	Х	Х	1	1	1	1				

X = Don't Care, Logic 1 = High, Logic 0 = Low

Logic Diagram



Absolute Maximum Ratings

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
E (PDIP) Package	67
M (SOIC) Package	73
Maximum Junction Temperature	150 ^o C
Maximum Storage Temperature Range	65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C
(SOIC - Lead Tips Only)	

Operating Conditions

Temperature Range (T _A)55 ⁰ C to 125 ⁰	C,
Supply Voltage Range, V _{CC}	
HC Types2V to 6	۷
HCT Types	ί۷
DC Input or Output Voltage, V _I , V _O 0V to V _C	СС
Input Rise and Fall Time	
2V	x)
4.5V 500ns (Ma	x)
6V	x)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

		TE: CONDI		V _{CC} 25°C -			-40°C 1	O 85°C	-55°C T	O 125°C	-	
PARAMETER	SYMBOL	V _I (V)	I _O (mA)	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES												
High Level Input	V _{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
Voltage				4.5	3.15	•	-	3.15	-	3.15	-	V
				6	4.2	•	-	4.2	-	4.2	-	V
Low Level Input	vel Input V _{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
Voltage				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output	V _{OH}	V _{IH} or V _{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
Voltage CMOS Loads			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
omeo Loado			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output	7		-	-	-	-	-	-	-	-	-	V
Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output	V _{OL}	OL VIH or VIL	0.02	2	-	-	0.1	-	0.1	-	0.1	V
Voltage CMOS Loads			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output	1		-	-	-	-	-	-	-	-	-	V
Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
TTE LOADS			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	II	V _{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	μΑ
Quiescent Device Current	Icc	V _{CC} or GND	0	6	-	-	8	-	80	-	160	μΑ

DC Electrical Specifications (Continued)

		TES CONDI		V _{CC}		25°C		-40°C 1	O 85°C	-55°C T	O 125°C	
PARAMETER	SYMBOL	V _I (V)	I _O (mA)	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HCT TYPES												
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	Voн	V _{IH} or V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	lį	V _{CC} and GND	0	5.5	-		±0.1	-	±1	-	±1	μА
Quiescent Device Current	Icc	V _{CC} or GND	0	5.5	-	-	8	-	80	-	160	μА
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI _{CC} (Note 2)	V _{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μА

NOTE:

HCT Input Loading Table

INPUT	UNIT LOADS
All	0.7

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360µA max at 25°C.

Switching Specifications Input t_r , $t_f = 6ns$

		TEST	V _{CC}	25°C			-40°C TO 85°C		-55°C TO 125°C		
PARAMETER	SYMBOL	CONDITIONS	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES	•										-
Propagation Delay	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	145	-	180	-	220	ns
A0, A1 to Outputs			4.5	-	-	29	-	36	-	44	ns
			6	-	-	25	-	31	-	38	ns
E to Outputs	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	135	-	170	-	205	ns
			4.5	-	-	27	-	34	-	41	ns
			6	-	-	23	-	29	-	35	ns
Select to Output	t _{PLH} , t _{PHL}	C _L = 15pF	5	-	12	-	-	-	-	-	ns
Enable to Output	t _{PLH} , t _{PHL}	C _L = 15pF	5	-	11	-	-	-	-	-	ns

^{2.} For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

Switching Specifications Input t_r , $t_f = 6ns$ (Continued)

	TEST V _{CC} 25°C				С ТО °С		C TO 5°C				
PARAMETER	SYMBOL	CONDITIONS	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
Output Transition Time (Figure 1)	t _{TLH} , t _{THL}	C _L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Power Dissipation Capacitance, (Notes 3, 4)	C _{PD}	-	5	-	55	-	-	-	-	-	pF
Input Capacitance	C _{IN}	=	-	-	-	10	-	10	-	10	pF
HCT TYPES	•										•
Propagation Delay											
A0, A1 to Outputs	t _{PLH} , t _{PHL}	C _L = 50pF	4.5	-	-	34	-	43	-	51	ns
E to Outputs	t _{PLH} , t _{PHL}	C _L = 50pF	4.5	-	-	34	-	43	-	51	ns
Select to Output	t _{PLH} , t _{PHL}	C _L = 15pF	5	-	14	-	-	-	-	-	ns
Enable to Output	t _{PLH} , t _{PHL}	C _L = 15pF	5	-	14	-	-	-	-	-	ns
Output Transition Time (Figure 2)	t _{TLH} , t _{THL}	C _L = 50pF	4.5	-	-	15	-	19	-	22	ns
Power Dissipation Capacitance, (Notes 3, 4)	C _{PD}	-	5	-	59	-	-	-	-	-	pF
Input Capacitance	C _{IN}	-	-	-	-	10	-	10	-	10	pF

NOTES:

- 3. $C_{\mbox{PD}}$ is used to determine the dynamic power consumption, per decoder/demux.
- 4. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where: $f_i = Input$ Frequency, $C_L = Output$ Load Capacitance, $V_{CC} = Supply$ Voltage.

Test Circuits and Waveforms

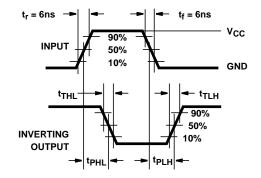


FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

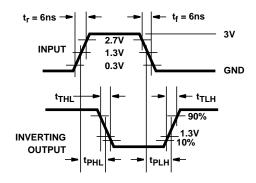


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
CD54HC139F	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC139F
CD54HC139F.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC139F
CD54HC139F3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8409201EA CD54HC139F3A
CD54HC139F3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8409201EA CD54HC139F3A
CD54HCT139F	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT139F
CD54HCT139F.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT139F
CD54HCT139F3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT139F3A
CD54HCT139F3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT139F3A
CD74HC139E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC139E
CD74HC139E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC139E
CD74HC139M	Obsolete	Production	SOIC (D) 16	-	=	Call TI	Call TI	-55 to 125	HC139M
CD74HC139M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC139M
CD74HC139M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC139M
CD74HCT139E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT139E
CD74HCT139E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT139E
CD74HCT139EE4	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT139E
CD74HCT139M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HCT139M
CD74HCT139M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT139M
CD74HCT139M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT139M

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

PACKAGE OPTION ADDENDUM

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(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF CD54HC139, CD54HC139, CD74HC139, CD74HC139:

Catalog: CD74HC139, CD74HCT139

Military: CD54HC139, CD54HCT139

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC139M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT139M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC139M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74HCT139M96	SOIC	D	16	2500	340.5	336.1	32.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC139E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC139E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC139E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC139E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT139E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT139E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT139E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT139E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT139EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT139EE4	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



14 LEADS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



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