# CD54/74HC123, CD54/74HCT123, CD74HC423, CD74HCT423

Data sheet acquired from Harris Semiconductor
SCHS142F

September 1997 - Revised October 2003

## High-Speed CMOS Logic Dual Retriggerable Monostable Multivibrators with Resets

### Features

- **Overriding Reset Terminates Output Pulse**
- **Triggering From the Leading or Trailing Edge**
- **Q and $\overline{Q}$ Buffered Outputs**
- **Separate Resets**
- **Wide Range of Output-Pulse Widths**
- **Schmitt Trigger on Both $\overline{A}$ and B Inputs**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55$^{o}$C to 125$^{o}$C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: $N_{IL}$ = 30%, $N_{IH}$ = 30%of $V_{CC}$ at $V_{CC}$ = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, $V_{IL}$= 0.8V (Max), $V_{IH}$ = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at $V_{OL}$, $V_{OH}$**

### Description

The ’HC123, ’HCT123, CD74HC423 and CD74HCT423 are dual monostable multivibrators with resets. They are all retriggerable and differ only in that the 123 types can be triggered by a negative to positive reset pulse; whereas the 423 types do not have this feature. An external resistor ($R_X$) and an external capacitor ($C_X$) control the timing and the accuracy for the circuit. Adjustment of Rx and $C_X$ provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. Pulse triggering on the $\overline{A}$ and B inputs occur at a particular voltage level and is not related to the rise and fall times of the trigger pulses.

Once triggered, the output pulse width may be extended by retriggering inputs $\overline{A}$ and B. The output pulse can be terminated by a LOW level on the Reset (R) pin. Trailing edge triggering ($\overline{A}$) and leading edge triggering (B) inputs are provided for triggering from either edge of the input pulse. If either Mono is not used each input on the unused device ($\overline{A}$, B, and $\overline{R}$) must be terminated high or low.

The minimum value of external resistance, Rx is typically 5kΩ. The minimum value external capacitance, CX, is 0pF. The calculation for the pulse width is $t_W$ = 0.45 $R_XC_X$ at $V_{CC}$ = 5V.

### Ordering Information

| PART NUMBER | TEMP. RANGE ($^{o}$C) | PACKAGE |
|---|---|---|
| CD54HC123F3A | -55 to 125 | 16 Ld CERDIP |
| CD54HCT123F3A | -55 to 125 | 16 Ld CERDIP |
| CD74HC123E | -55 to 125 | 16 Ld PDIP |
| CD74HC123M | -55 to 125 | 16 Ld SOIC |
| CD74HC123MT | -55 to 125 | 16 Ld SOIC |
| CD74HC123M96 | -55 to 125 | 16 Ld SOIC |
| CD74HC123NSR | -55 to 125 | 16 Ld SOP |
| CD74HC123PW | -55 to 125 | 16 Ld TSSOP |
| CD74HC123PWR | -55 to 125 | 16 Ld TSSOP |
| CD74HC123PWT | -55 to 125 | 16 Ld TSSOP |
| CD74HC423E | -55 to 125 | 16 Ld PDIP |
| CD74HC423M | -55 to 125 | 16 Ld SOIC |
| CD74HC423MT | -55 to 125 | 16 Ld SOIC |
| CD74HC423M96 | -55 to 125 | 16 Ld SOIC |
| CD74HC423NSR | -55 to 125 | 16 Ld SOP |
| CD74HCT123E | -55 to 125 | 16 Ld PDIP |
| CD74HCT123M | -55 to 125 | 16 Ld SOIC |
| CD74HCT123MT | -55 to 125 | 16 Ld SOIC |
| CD74HCT123M96 | -55 to 125 | 16 Ld SOIC |
| CD74HCT423E | -55 to 125 | 16 Ld PDIP |
| CD74HCT423MT | -55 to 125 | 16 Ld SOIC |
| CD74HCT423M96 | -55 to 125 | 16 Ld SOIC |

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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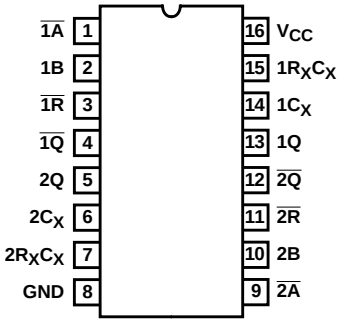
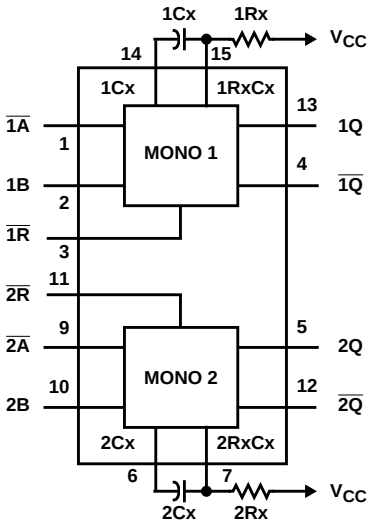
## Pinout

**CD54HC123, CD54HCT123**
**(CERDIP)**
**CD74HC123**
**(PDIP, SOIC, SOP, TSSOP)**
**CD74HC423**
**(PDIP, SOIC, SOP)**
**CD74HCT123, CD74HCT423**
**(PDIP, SOIC)**
TOP VIEW




## Functional Diagram




**TRUTH TABLE**

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| $\overline{A}$ | B | $\overline{R}$ | Q | $\overline{Q}$ |
| **CD74HC/HCT123** | | | | |
| H | X | H | L | H |
| X | L | H | L | H |
| L | ↑ | H | ⎍ | ⎏ |
| ↓ | H | H | ⎍ | ⎏ |
| X | X | L | L | H |
| L | H | ↑ | ⎍ | ⎏ |
| **CD74HC/HCT423** | | | | |
| H | X | H | L | H |
| X | L | H | L | H |
| L | ↑ | H | ⎍ | ⎏ |
| ↓ | H | H | ⎍ | ⎏ |
| X | X | L | L | H |

H = High Voltage Level, L = Low Voltage Level,
X = Don't Care.

## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ . . . . . -0.5V to 7V
DC Input Diode Current, $I_{IK}$
For $V_I$ < -0.5V or $V_I$ > $V_{CC}$ + 0.5V . . . . . ±20mA
DC Output Diode Current, $I_{OK}$
For $V_O$ < -0.5V or $V_O$ > $V_{CC}$ + 0.5V . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, $I_O$
For $V_O$ > -0.5V or $V_O$ < $V_{CC}$ + 0.5V . . . . . ±25mA
DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$ . . . . . ±50mA

## Operating Conditions

Temperature Range ($T_A$) . . . . . -55°C to 125°C
Supply Voltage Range, $V_{CC}$
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, $V_I$, $V_O$ . . . . . 0V to $V_{CC}$
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)

## Thermal Information

Package Thermal Impedance, $\theta_{JA}$ (see Note 1):
E (PDIP) Package . . . . . 67°C/W
M (SOIC) Package. . . . . 73°C/W
NS (SOP) Package . . . . . 64°C/W
PW (TSSOP) Package . . . . . 108°C/W
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS $V_I$ (V) | TEST CONDITIONS $I_O$ (mA) | $V_{CC}$ (V) | 25°C MIN | 25°C TYP | 25°C MAX | -40°C TO 85°C MIN | -40°C TO 85°C MAX | -55°C TO 125°C MIN | -55°C TO 125°C MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **HC TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 2 | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | | | 4.5 | 3.15 | - | - | 3.15 | - | 3.15 | - | V |
| | | | | 6 | 4.2 | - | - | 4.2 | - | 4.2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 2 | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | | | 4.5 | - | - | 1.35 | - | 1.35 | - | 1.35 | V |
| | | | | 6 | - | - | 1.8 | - | 1.8 | - | 1.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 2 | 1.9 | - | - | 1.9 | - | 1.9 | - | V |
| | | | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| | | | -0.02 | 6 | 5.9 | - | - | 5.9 | - | 5.9 | - | V |
| High Level Output Voltage TTL Loads | | | - | - | - | - | - | - | - | - | - | V |
| | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| | | | -5.2 | 6 | 5.48 | - | - | 5.34 | - | 5.2 | - | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 2 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 6 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | - | - | - | - | - | - | - | - | - | V |
| | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| | | | 5.2 | 6 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ or GND | - | 6 | - | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 6 | - | - | 8 | - | 80 | - | 160 | µA |

## DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS $V_I$ (V) | TEST CONDITIONS $I_O$ (mA) | $V_{CC}$ (V) | 25°C MIN | 25°C TYP | 25°C MAX | -40°C TO 85°C MIN | -40°C TO 85°C MAX | -55°C TO 125°C MIN | -55°C TO 125°C MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **HCT TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 4.5 to 5.5 | 2 | - | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 4.5 to 5.5 | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| High Level Output Voltage TTL Loads | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ and GND | 0 | 5.5 | - | | ±0.1 | - | ±1 | - | ±1 | µA |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 5.5 | - | - | 8 | - | 80 | - | 160 | µA |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | $\Delta I_{CC}$ (Note 2) | $V_{CC}$ -2.1 | - | 4.5 to 5.5 | - | 100 | 360 | - | 450 | - | 490 | µA |

NOTE:

2. For dual-supply systems theoretical worst case ($V_I$ = 2.4V, $V_{CC}$ = 5.5V) specification is 1.8mA.

## HCT Input Loading Table

| INPUT | UNIT LOADS |
|---|---|
| All | 0.35 |

NOTE: Unit Load is $\Delta I_{CC}$ limit specified in DC Electrical Table, e.g. 360µA max at 25°C.

## Prerequisite for Switching Specifications

| PARAMETER | SYMBOL | $V_{CC}$ (V) | 25°C MIN | 25°C TYP | 25°C MAX | -40°C TO 85°C MIN | -40°C TO 85°C TYP | -40°C TO 85°C MAX | -55°C TO 125°C MIN | -55°C TO 125°C TYP | -55°C TO 125°C MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **HC TYPES** | | | | | | | | | | | | |
| Minimum Input, Pulse Width $\overline{A}$ | $t_{WL}$ | 2 | 100 | - | - | 125 | - | - | 150 | - | - | ns |
| | | 4.5 | 20 | - | - | 25 | - | - | 30 | - | - | ns |
| | | 6 | 17 | - | - | 21 | - | - | 26 | - | - | ns |
| B | $t_{WH}$ | 2 | 100 | - | - | 125 | - | - | 150 | - | - | ns |
| | | 4.5 | 20 | - | - | 25 | - | - | 30 | - | - | ns |
| | | 6 | 17 | - | - | 21 | - | - | 26 | - | - | ns |

**Prerequisite for Switching Specifications** **(Continued)**

| PARAMETER | SYMBOL | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | | -55°C TO 125°C | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $\overline{R}$ | $t_{WL}$ | 2 | 100 | - | - | 125 | - | - | 150 | - | 150 | ns |
| | | 4.5 | 20 | - | - | 25 | - | - | 30 | - | 30 | ns |
| | | 6 | 17 | - | - | 21 | - | - | 26 | - | 26 | ns |
| $\overline{A}$ and B Hold Time | $t_H$ | 2 | 50 | - | - | 65 | - | - | 75 | - | 75 | ns |
| | | 4.5 | 10 | - | - | 13 | - | - | 15 | - | 15 | ns |
| | | 6 | 9 | - | - | 11 | - | - | 13 | - | 13 | ns |
| Reset Removal Time | $t_{REM}$ | 2 | 50 | - | - | 65 | - | - | 75 | - | 75 | ns |
| | | 4.5 | 10 | - | - | 13 | - | - | 15 | - | 15 | ns |
| | | 6 | 9 | - | - | 11 | - | - | 13 | - | 13 | ns |
| Retrigger Time Number | $t_{rT}$ | 5 | - | - | - | - | - | - | - | - | - | ns |
| $R_X$ = 10KΩ, $C_X$ = 0 | | | - | 50 | - | - | 63 | - | - | 76 | - | ns |
| Output Pulse Width Q or $\overline{Q}$ $R_X$ = 10KΩ, $C_X$ = 10nF | $t_W$ | 5 | 40 | - | 50 | 38.7 | - | 51.3 | 38.2 | - | 51.8 | µs |
| **HCT TYPES** | | | | | | | | | | | | |
| Minimum Input, Pulse Width $\overline{A}$ | $t_{WL}$ | 5 | 20 | - | - | 25 | - | - | 30 | - | - | - ns |
| B | $t_{WH}$ | | 20 | - | - | 25 | - | - | 30 | - | - | ns |
| $\overline{R}$ | $t_{WL}$ | | 20 | - | - | 25 | - | - | 30 | - | - | ns |
| $\overline{A}$ and B Hold Time | $t_H$ | 5 | 10 | - | - | 13 | - | - | 15 | - | - | ns |
| Reset Removal Time | $t_{REM}$ | 5 | 10 | - | - | 13 | - | - | 15 | | - | ns |
| Retrigger Time Number (Note 3) $R_X$ = 10KΩ, $C_X$ = 0 | $t_{rT}$ | 5 | - | 50 | - | - | 63 | - | - | 76 | - | ns |
| Output Pulse Width Q or Q $R_X$ = 10KΩ, $C_X$ = 10nF | $t_W$ | 5 | 40 | - | 50 | 38.7 | - | 51.3 | 38.2 | - | 51.8 | µs |

NOTE:

3. Time to trigger depends on the values of $R_X$ and $C_X$. The output pulse width can only be extended when the time between the active-going edges of the trigger input pulses meet the minimum retrigger time requirement.

**Switching Specifications** Input $t_r$, $t_f$ = 6ns, $R_X$ = 10KΩ, $C_X$ = 0

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | | |
| Trigger Propagation Delay $\overline{A}$, B, $\overline{R}$ to Q | $t_{PLH}$ | $C_L$ = 50pF | 2 | - | - | 300 | - | 375 | - | 450 | ns |
| | | | 4.5 | - | - | 60 | - | 75 | - | 90 | ns |
| | | $C_L$ = 15pF | 5 | - | 25 | - | - | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | - | 51 | - | 64 | - | 76 | ns |
| $\overline{A}$, B, $\overline{R}$ to $\overline{Q}$ | $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 320 | - | 400 | - | 480 | ns |
| | | | 4.5 | - | - | 64 | - | 80 | - | 96 | ns |
| | | $C_L$ = 15pF | 5 | - | 26 | - | - | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | - | 54 | - | 68 | - | 82 | ns |
| Reset Propagation Delay $\overline{R}$ to Q or $\overline{Q}$ | $t_{PHL}$, $t_{PLH}$ | $C_L$ = 50pF | 2 | - | - | 215 | - | 270 | - | 325 | ns |
| | | | 4.5 | - | - | 43 | - | 54 | - | 65 | ns |
| | | | 6 | - | - | 37 | - | 46 | - | 55 | ns |
| Output Transition Time | $t_{THL}$, $t_{TLH}$ | $C_L$ = 50pF | 2 | - | - | 75 | - | 95 | - | 110 | ns |
| | | | 4.5 | - | - | 15 | - | 19 | - | 22 | ns |
| | | | 6 | - | - | 13 | - | 16 | - | 19 | ns |
| Output Pulse Width $R_X$ = 10KΩ, $C_X$ = 10nF | - | - | 5 | - | 45 | - | - | - | - | - | µs |
| Pulse Width Match Between Circuits In the Same Package $R_X$ = 10KΩ, $C_X$ = 10pF | - | - | 5 | - | ±2 | - | - | - | - | - | % |
| Power Dissipation Capacitance (Note 4) | $C_{PD}$ | $C_L$ = 15pF | 5 | - | - | - | - | - | - | - | pF |
| Input Capacitance | $C_{IN}$ | $C_L$ = 50pF | - | 10 | - | 10 | - | 10 | - | 10 | pF |
| **HCT TYPES** | | | | | | | | | | | |
| Trigger Propagation Delay $\overline{A}$, B, $\overline{R}$ to $\overline{Q}$ | $t_{PLH}$ | $C_L$ = 50pF | 4.5 | - | - | 60 | - | 75 | - | 90 | ns |
| | | $C_L$ = 15pF | 5 | - | 25 | - | - | - | - | - | ns |
| $\overline{A}$, B, $\overline{R}$ to $\overline{Q}$ | $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 68 | - | 85 | - | 102 | ns |
| | | $C_L$ =15pF | 5 | - | 27 | - | - | - | - | - | ns |
| Reset Propagation Delay $\overline{R}$ to Q or $\overline{Q}$ | $t_{PHL}$, $t_{PLH}$ | $C_L$ = 50pF | 4.5 | - | - | 48 | - | 60 | - | 72 | ns |
| Output Transition Time | $t_{THL}$, $t_{TLH}$ | $C_L$ = 50pF | 4.5 | - | - | 15 | - | 19 | - | 22 | ns |
| Output Pulse Width $R_X$ = 10KΩ, $C_X$ = 10nF | - | - | 5 | - | 45 | - | - | - | - | - | µs |

**Switching Specifications** Input $t_r$, $t_f$ = 6ns, $R_X$ = 10KΩ, $C_X$ = 0 **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| Pulse Width Match Between Circuits In the Same Package $R_X$ = 10KΩ, $C_X$ = 10pF | - | - | 5 | | ±2 | - | - | - | - | - | % |
| Input Capacitance | $C_{IN}$ | $C_L$ = 50pF | - | - | - | 10 | - | 10 | - | 10 | pF |

NOTE:

4. $C_{PD}$ is used to determine the dynamic power consumption, per multivibrator.
   $P_D = (C_{PD} + C_X) V_{CC}^2 f_i \Sigma(C_L V_{CC}^2 f_O)$
   Where
   $f_i$ = input frequency
   $f_O$ = Output Frequency
   $C_L$ = Output Load Capacitance
   $C_X$ = External Capacitance
   $V_{CC}$ = Supply Voltage,
   assuming $f_i \ll \frac{1}{t_W}$

## *Test Circuits and Waveforms*

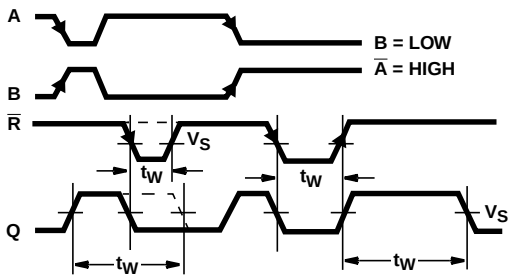



FIGURE 1. OUTPUT PULSE CONTROL USING RESET INPUT ($\overline{R}$) PULSE FOR 123

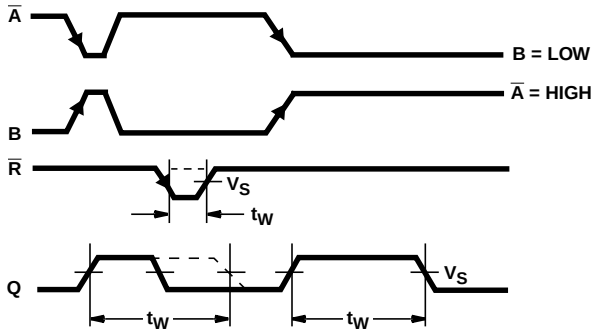
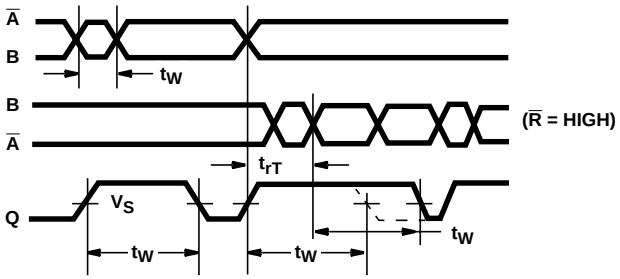



FIGURE 2. OUTPUT PULSE CONTROL USING RESET INPUT ($\overline{R}$) FOR 423




NOTE: Output pulse control using retrigger pulse for 123 and 423.

FIGURE 3. TRIGGERING OF ONE SHOT BY INPUT $\overline{A}$ OR INPUT B FOR A PERIOD $t_W$

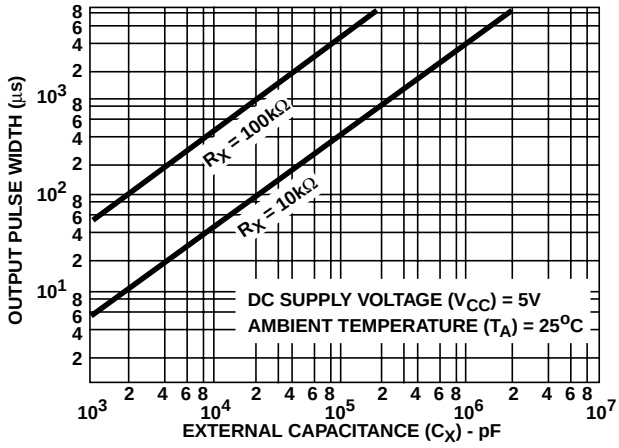



FIGURE 4. TYPICAL OUTPUT PULSE WIDTH AS A FUNCTION OF $C_X$ FOR $R_X$ = 10kΩ AND 100kΩ

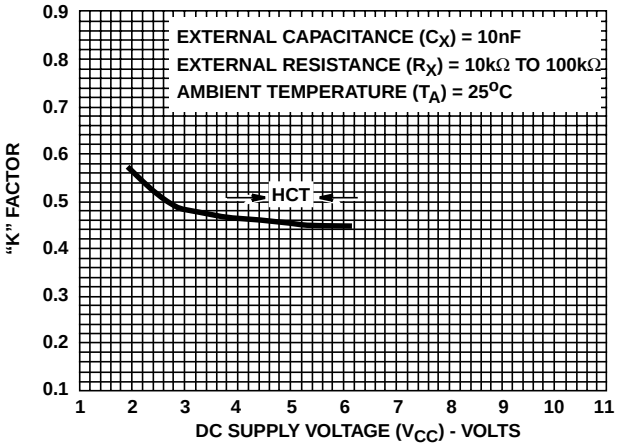



FIGURE 5. TYPICAL "K" FACTOR AS A FUNCTION OF $V_{CC}$

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-8684701EA | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8684701EA CD54HC123F3A |
| 5962-8970001EA | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8970001EA CD54HCT123F3A |
| CD54HC123F | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | CD54HC123F |
| CD54HC123F.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | CD54HC123F |
| CD54HC123F3A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8684701EA CD54HC123F3A |
| CD54HC123F3A.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8684701EA CD54HC123F3A |
| CD54HCT123F3A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8970001EA CD54HCT123F3A |
| CD54HCT123F3A.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8970001EA CD54HCT123F3A |
| CD74HC123E | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HC123E |
| CD74HC123E.A | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HC123E |
| CD74HC123EE4 | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HC123E |
| CD74HC123M | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | -55 to 125 | HC123M |
| CD74HC123M96 | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -55 to 125 | HC123M |
| CD74HC123M96.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC123M |
| CD74HC123M96E4 | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC123M |
| CD74HC123M96G4 | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC123M |
| CD74HC123M96G4.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC123M |
| CD74HC123NSR | Active | Production | SOP (NS) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC123M |
| CD74HC123NSR.A | Active | Production | SOP (NS) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC123M |
| CD74HC123PW | Obsolete | Production | TSSOP (PW) \| 16 | - | - | Call TI | Call TI | -55 to 125 | HJ123 |
| CD74HC123PWR | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -55 to 125 | HJ123 |
| CD74HC123PWR.A | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HJ123 |
| CD74HC123PWRG4 | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HJ123 |
| CD74HC123PWRG4.A | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HJ123 |
| CD74HC123PWT | Obsolete | Production | TSSOP (PW) \| 16 | - | - | Call TI | Call TI | -55 to 125 | HJ123 |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| CD74HC423E | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HC423E |
| CD74HC423E.A | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HC423E |
| CD74HC423M | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | -55 to 125 | HC423M |
| CD74HC423M96 | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC423M |
| CD74HC423M96.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC423M |
| CD74HC423M96G4 | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC423M |
| CD74HC423NSR | Active | Production | SOP (NS) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC423M |
| CD74HC423NSR.A | Active | Production | SOP (NS) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC423M |
| CD74HCT123E | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HCT123E |
| CD74HCT123E.A | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HCT123E |
| CD74HCT123M | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | -55 to 125 | HCT123M |
| CD74HCT123M96 | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT123M |
| CD74HCT123M96.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT123M |
| CD74HCT123MT | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | -55 to 125 | HCT123M |
| CD74HCT423E | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HCT423E |
| CD74HCT423E.A | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HCT423E |
| CD74HCT423M96 | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT423M |
| CD74HCT423M96.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT423M |
| CD74HCT423M96G4 | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT423M |
| CD74HCT423MT | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | -55 to 125 | HCT423M |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54HC123, CD54HCT123, CD74HC123, CD74HCT123 :**

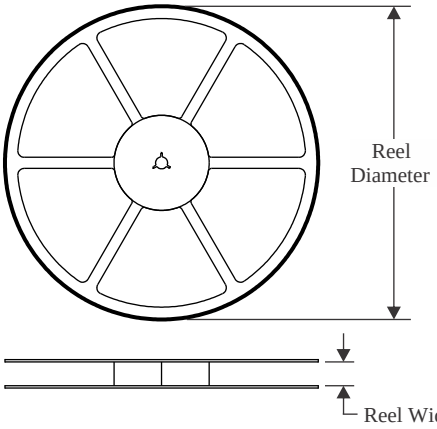
- Catalog : CD74HC123, CD74HCT123
- Military : CD54HC123, CD54HCT123

NOTE: Qualified Version Definitions:

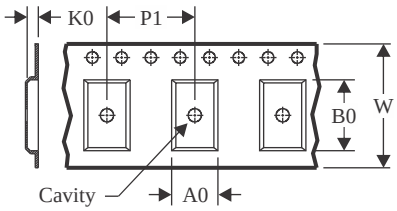
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

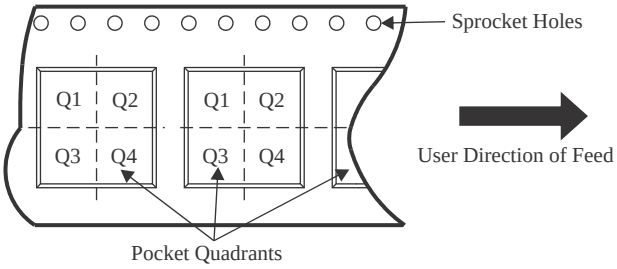



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

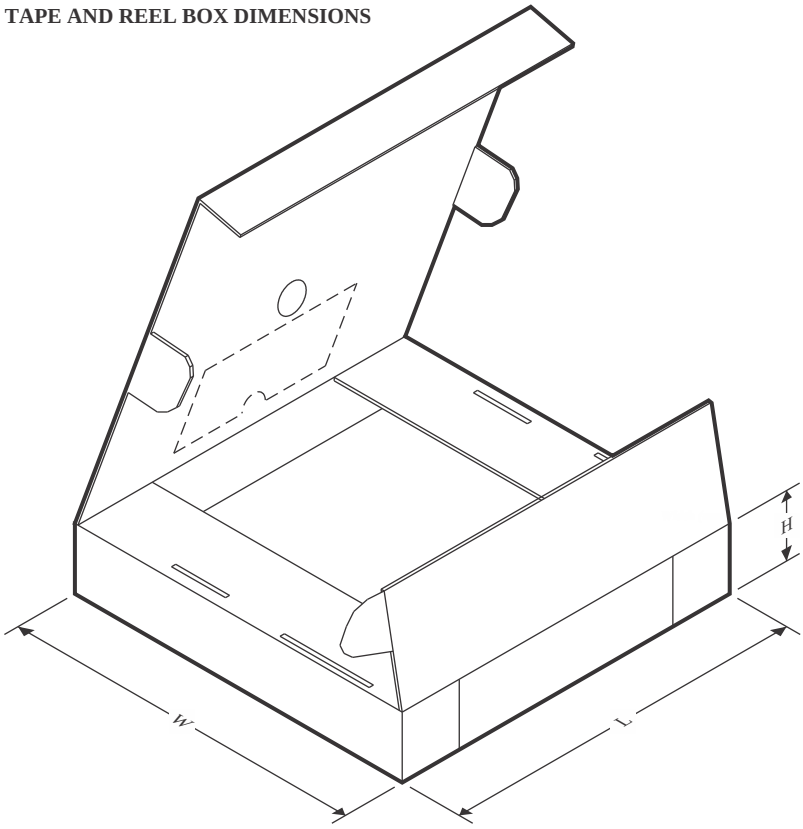
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74HC123M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HC123M96G4 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HC123NSR | SOP | NS | 16 | 2000 | 330.0 | 16.4 | 8.1 | 10.4 | 2.5 | 12.0 | 16.0 | Q1 |
| CD74HC123PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| CD74HC123PWRG4 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| CD74HC423M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HC423NSR | SOP | NS | 16 | 2000 | 330.0 | 16.4 | 8.1 | 10.4 | 2.5 | 12.0 | 16.0 | Q1 |
| CD74HCT123M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HCT423M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

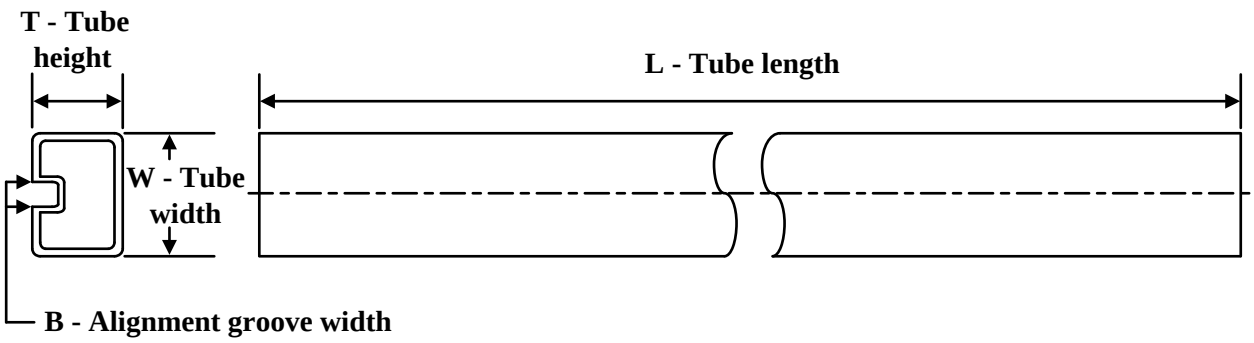
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

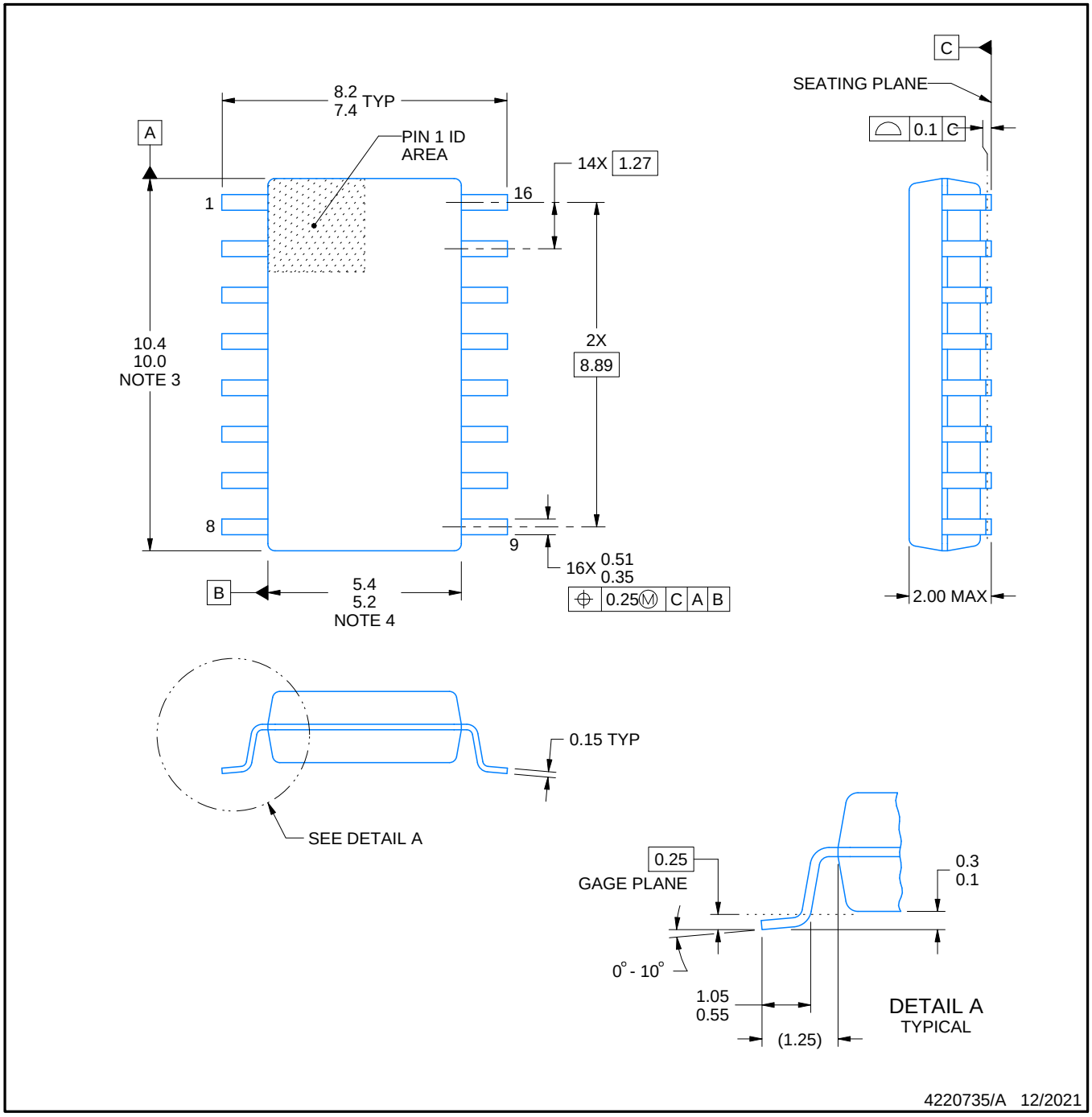
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD74HC123M96 | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| CD74HC123M96G4 | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| CD74HC123NSR | SOP | NS | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| CD74HC123PWR | TSSOP | PW | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| CD74HC123PWRG4 | TSSOP | PW | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| CD74HC423M96 | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| CD74HC423NSR | SOP | NS | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| CD74HCT123M96 | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| CD74HCT423M96 | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |

## TUBE



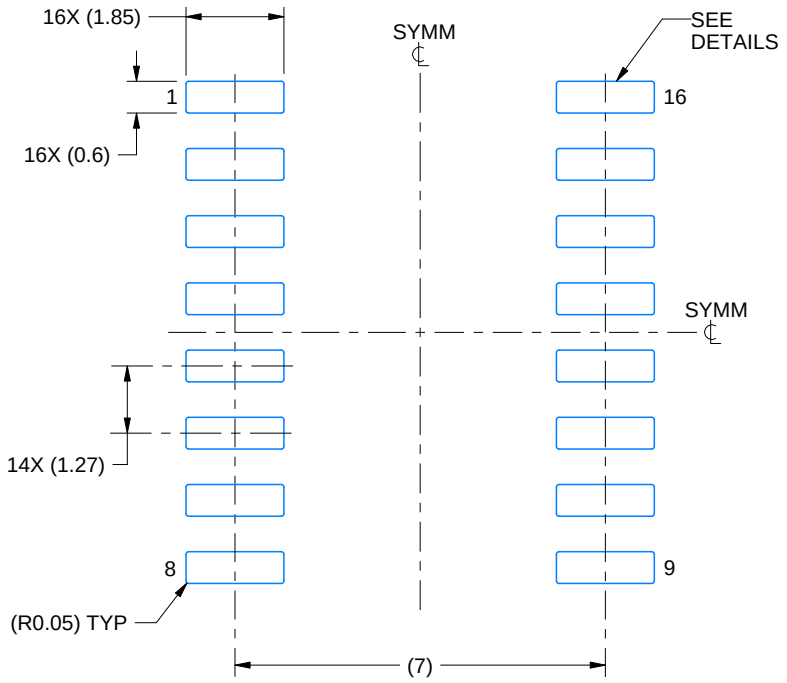

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| CD74HC123E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC123E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC123E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC123E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC123EE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC123EE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC423E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC423E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC423E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC423E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT123E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT123E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT123E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT123E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT423E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT423E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT423E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT423E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |

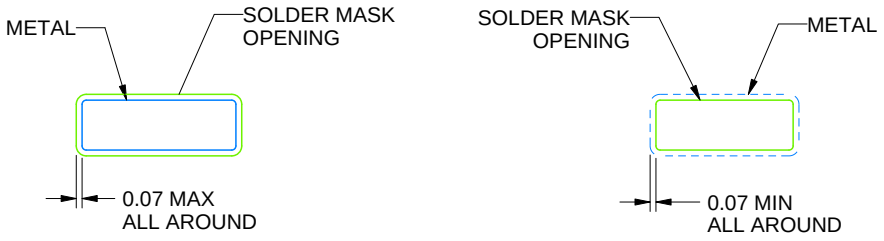



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.




LAND PATTERN EXAMPLE
SCALE:7X




NON SOLDER MASK DEFINED

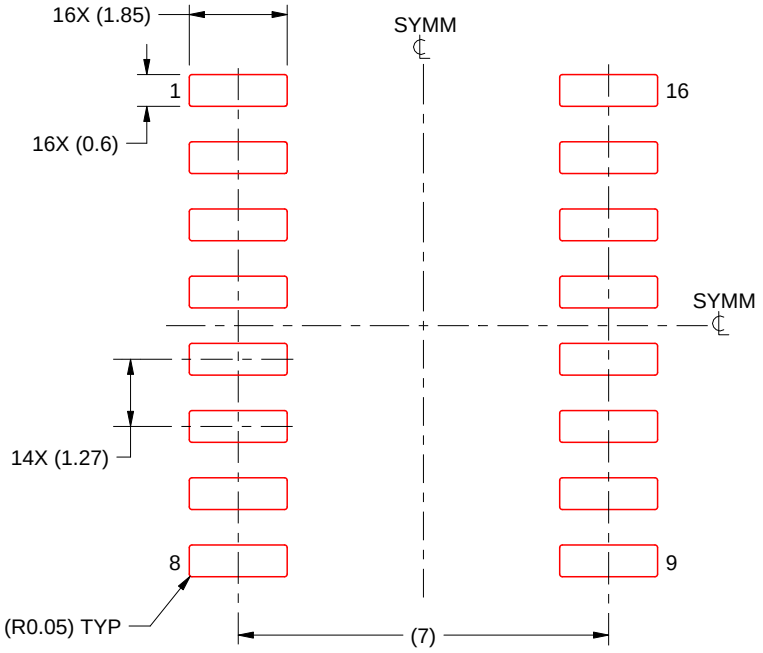
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



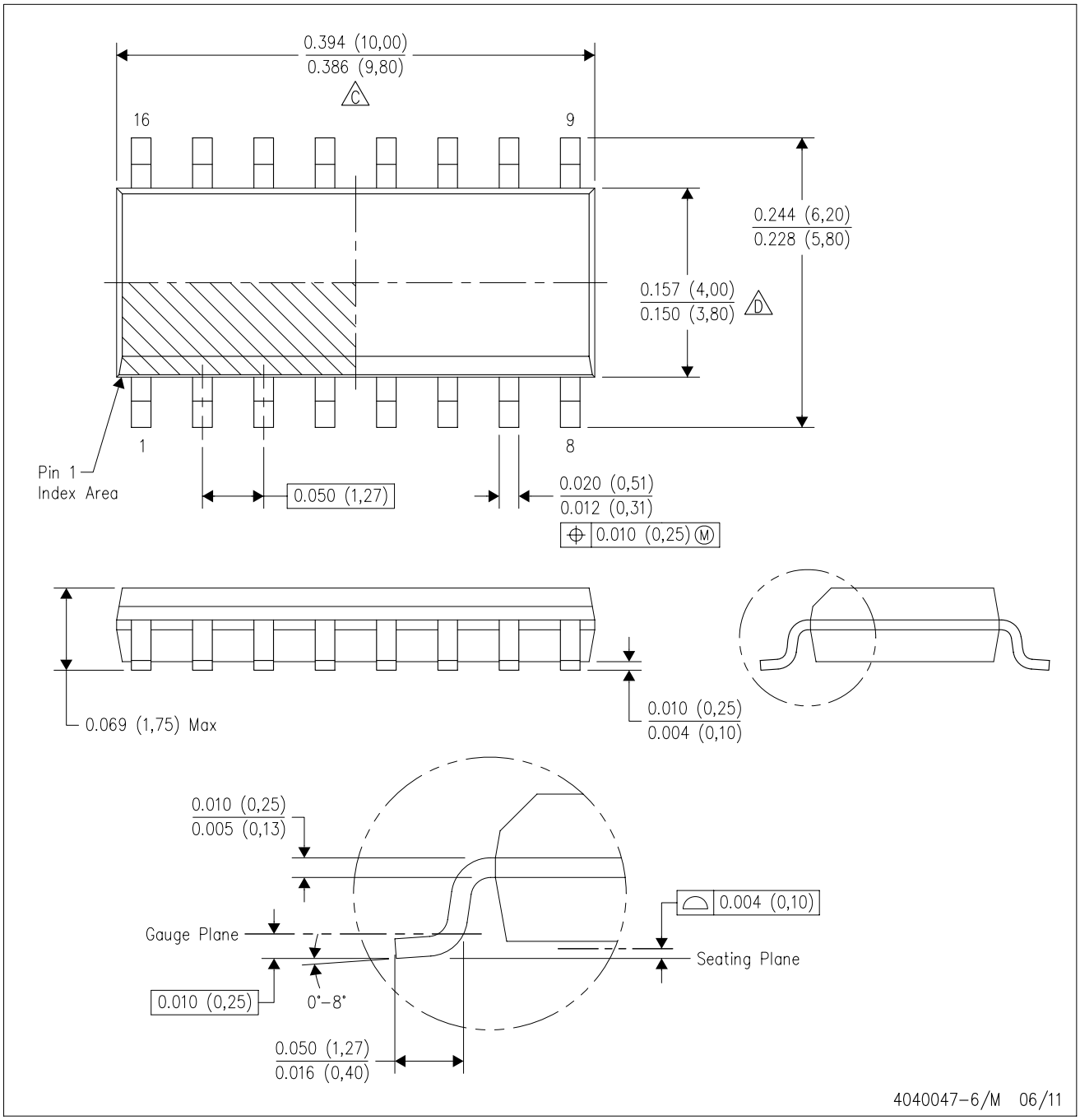

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

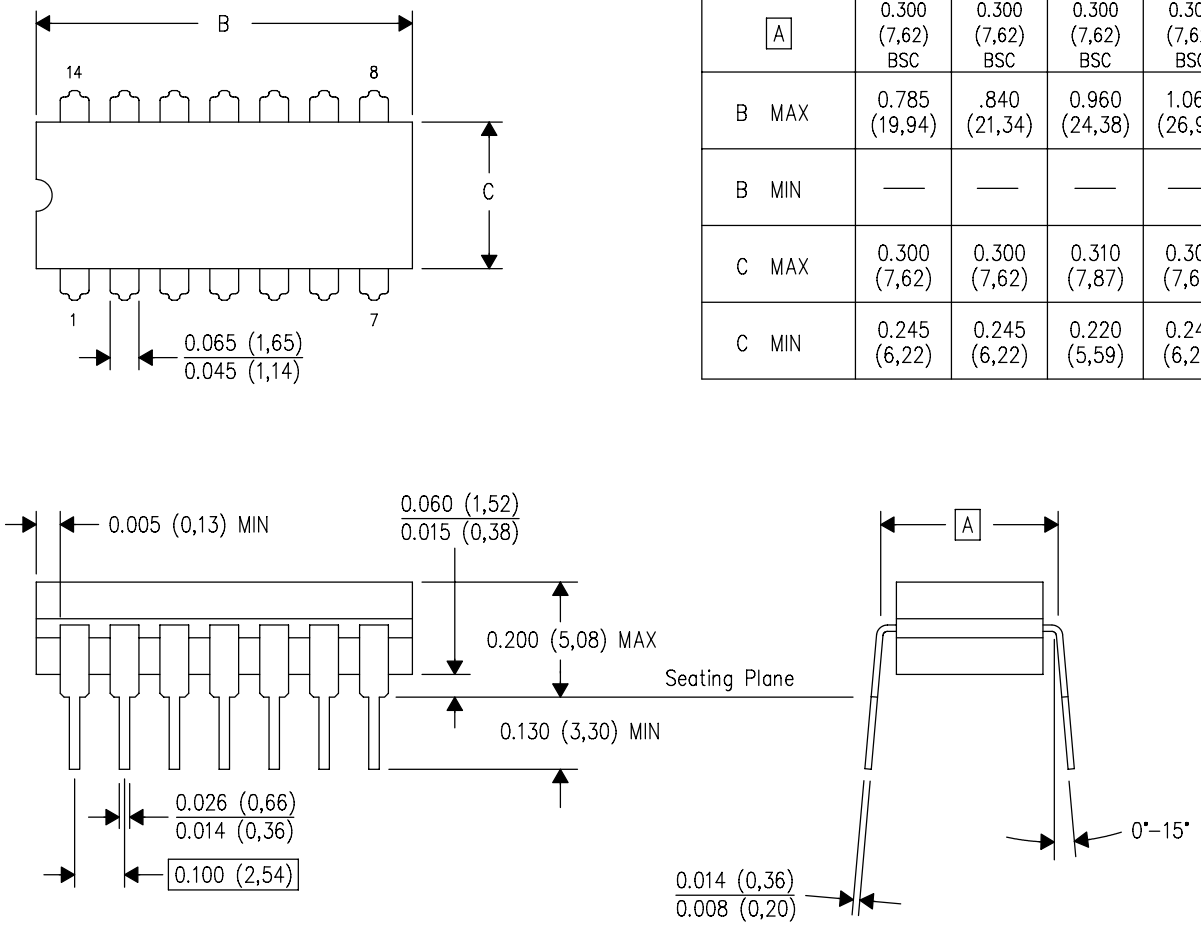
D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

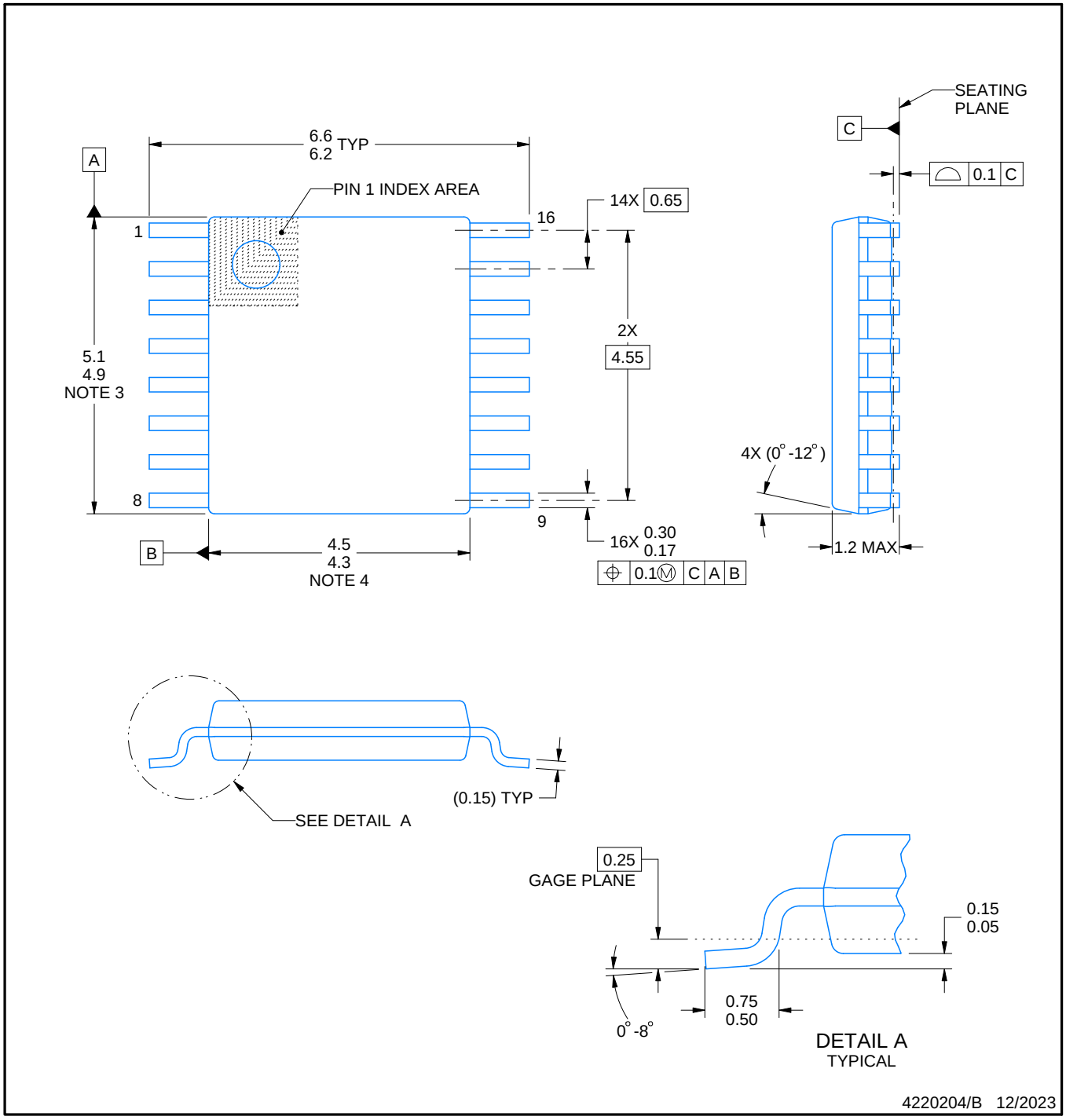
14 LEADS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

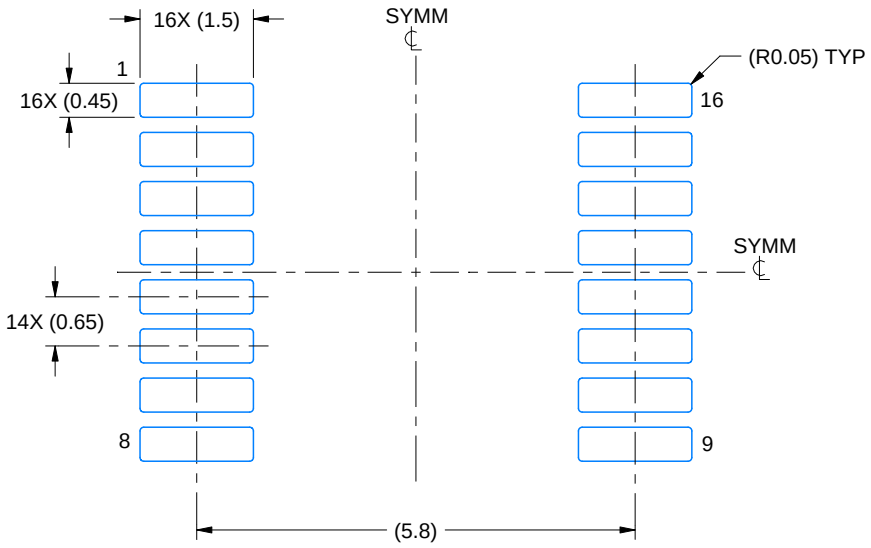
4040083/F 03/03

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

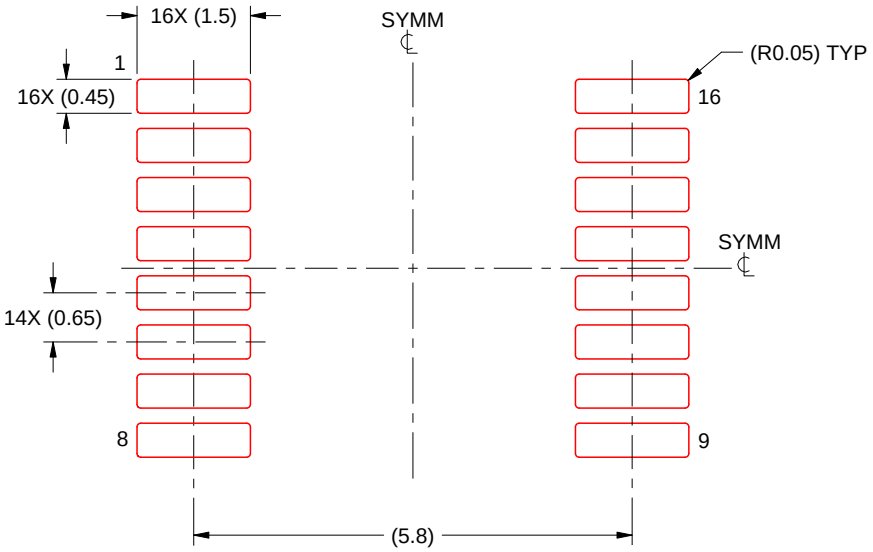
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

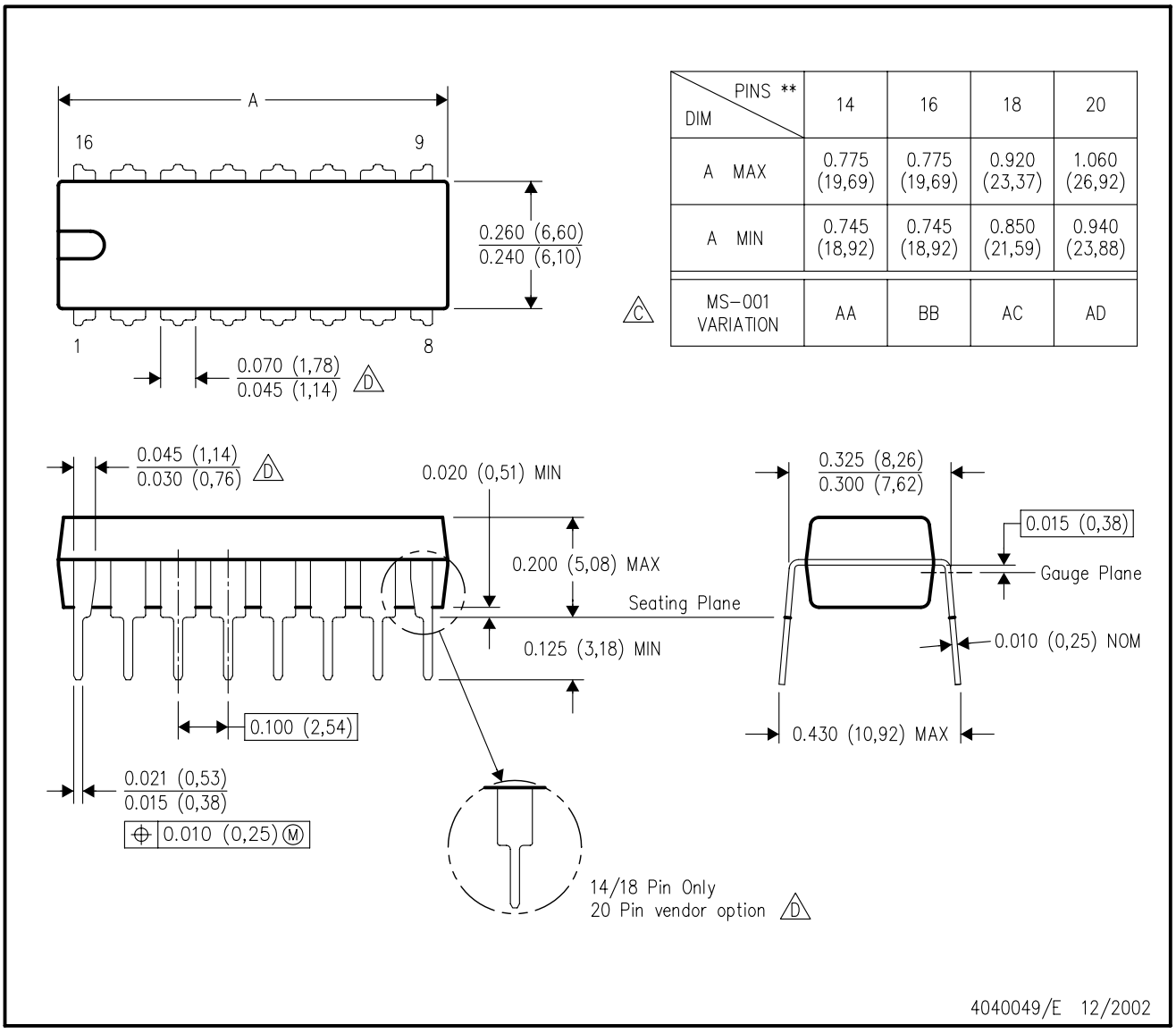
4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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