# CDx4ACT151 8-Line to 1-Line Data Selectors/Multiplexers

#### 1 Features

- Inputs are TTL-voltage compatible
- 8-line to 1-line multiplexers can perform as:
  - Boolean function generators
  - Parallel-to-serial converters
  - Data source selectors
- Speed of bipolar F, AS, and S, with significantly reduced power consumption
- Balanced propagation delays
- ±24mA output drive current
  - Fanout to 15 F devices
- SCR-latchup-resistant CMOS process and circuit
- Exceeds 2kV ESD protection per MIL-STD-883, method 3015

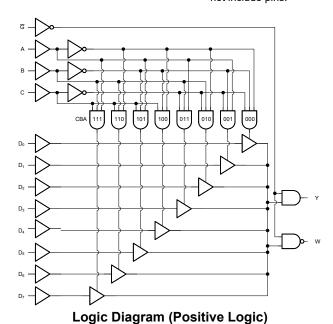
## 2 Description

These data selectors/multiplexers provide full binary decoding to select one of eight data sources. The strobe (G) input must be at a low logic level to enable the inputs. A high level at the strobe terminal forces the W output high and the Y output low.

#### **Device Information**

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>	BODY SIZE(3)
	D (SOIC, 16)	8.65mm × 6mm	8.65mm × 3.9mm
CDx4ACT151	J (CDIP , 16)	19.55mm × 7.9mm	19.55 mm × 6.7mm
CDX4ACT151	PW (TSSOP, 16)	5mm × 6.4mm	5mm × 4.4mm
	BQB (WQFN, 16)	3.5mm × 2.5mm	3.5mm × 2.5mm

- For more information, see Mechanical, Packaging, and Orderable Information.
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.





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# 3 Pin Configuration and Functions

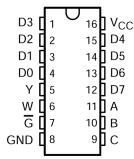


Figure 3-1. CD54ACT151 J Package; CD74ACT151 J, D, or PW Package; 16-Pin CDIP, SOIC or TSSOP (Top View)

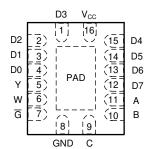


Figure 3-2. CD74ACT151 BQB Package, 16-Pin WQFN (Transparent Top View)

#### **Pin Functions**

P	IN	I/O <sup>(1)</sup>	DESCRIPTION
NO.	NAME	1/0(-/	DESCRIPTION
1	D3	I	Data input 3
2	D2	I	Data input 2
3	D1	I	Data input 1
4	D0	I	Data input 0
5	Y	0	Data output
6	W	0	Data output, inverted
7	G	I	Output strobe, active low
8	GND	_	Ground
9	С	I	Address select C
10	В	I	Address select B
11	Α	I	Address select A
12	D7	I	Data input 7
13	D6	I	Data input 6
14	D5	I	Data input 5
15	D4	I	Data input 4
16	V <sub>CC</sub>	_	Positive supply
Thermal Pad <sup>(2)</sup>		_	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply

- (1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power
- (2) BQB package only



## 4 Specifications

## 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		-0.5	6	V
I <sub>IK</sub> (2)	Input clamp current	(V <sub>I</sub> < 0 V or V <sub>I</sub> > V <sub>CC</sub> )		±20	mA
I <sub>OK</sub> (2)	Output clamp current	(V <sub>O</sub> < 0 V or V <sub>O</sub> > V <sub>CC</sub> )		±50	mA
Io	Continuous output current	$(V_O > 0 \text{ V or } V_O < V_{CC})$		±50	mA
	Continuous current through V <sub>CC</sub> or GND	·		±100	mA
T <sub>stg</sub>	Storage temperature range		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 4.2 ESD Ratings

			VALUE	UNIT
V <sub>(</sub>	Electrostatic  ESD) discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V

<sup>(1)</sup> JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.

## 4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		T <sub>A</sub> = 25°C -55°C to 125°C		-40°C to	UNIT			
		MIN	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>CC</sub>	Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8		0.8	V
VI	Input voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	0	$V_{CC}$	V
Vo	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		-24		-24		-24	mA
I <sub>OL</sub>	Low-level output current		24		24		24	mA
Δt/Δν	Input transition rise or fall rate		10		10		10	ns/V

<sup>(1)</sup> All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

#### 4.4 Thermal Information

			CD74ACT151		
	THERMAL METRIC <sup>(1)</sup>	D (SOIC)	BQB (WQFN)	PW (TSSOP)	UNIT
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	119.9	98.6	139.5	°C/W

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

<sup>(2)</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.



#### 4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V	T <sub>A</sub> = 2	5°C	-55°C to 125°C		-40°C to 85°C		UNIT
PARAMETER	TEST CON	DITIONS	V <sub>CC</sub>	MIN	MAX	MIN	MAX	X MIN MA	MAX	UNII
		I <sub>OH</sub> = -50 μA	4.5 V	4.4		4.4		4.4		
		I <sub>OH</sub> = -24 mA	4.5 V	3.94		3.7		3.8		
V <sub>OH</sub>	$V_I = V_{IH}$ or $V_{IL}$	I <sub>OH</sub> = -50 mA	5.5 V			3.85				V
		I <sub>OH</sub> = -75 mA	5.5 V					3.85		
		I <sub>OL</sub> = 50 μA	4.5 V	,	0.1		0.1		0.1	V
\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	\\ -\\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	I <sub>OL</sub> = 24 mA	4.5 V		0.36		0.5		0.44	
V <sub>OL</sub>	$V_I = V_{IH}$ or $V_{IL}$	I <sub>OL</sub> = 50 mA <sup>(1)</sup>	5.5 V				1.65			v
		I <sub>OL</sub> = 75 mA <sup>(1)</sup>	5.5 V						1.65	
I <sub>I</sub>	$V_I = V_{CC}$ or GND		5.5 V		±0.1		±1		±1	μA
I <sub>CC</sub>	$V_I = V_{CC}$ or GND,	I <sub>O</sub> = 0	5.5 V		8		160		80	μA
ΔI <sub>CC</sub> <sup>(2)</sup>	V <sub>I</sub> = V <sub>CC</sub> - 2.1 V		4.5 V to 5.5 V		2.4		3		2.8	mA
C <sub>i</sub>					10		10		10	pF

<sup>(1)</sup> Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

Table 4-1. Act Input Load
Table

INPUT	UNIT LOAD(1)
D	1
G	1
A, B, or C	1

Unit Load is ΔI<sub>CC</sub> limit specified in electrical characteristics table (e.g., 2.4 mA at 25°C).

## 4.6 Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC}$  = 5 V ± 0.5 V,  $C_L$  = 50 pF (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	EDOM (INDUT)	TO (OUTPUT)	-55°C to	-55°C to 125°C		-40°C to 85°C	
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	MIN	MAX	UNIT
t <sub>PLH</sub>	D	Y	3.9	15.5	4	14.1	
t <sub>PHL</sub>	D	Ť	3.9	15.5	4	14.1	ns
t <sub>PLH</sub>	D	W	4.2	16.9	4.4	15.4	
t <sub>PHL</sub>	D	VV	4.2	16.9	4.4	15.4	ns
t <sub>PLH</sub>	4.5.	Y	5.1	20.2	5.2	18.4	20
t <sub>PHL</sub>	A, B, or C	I	5.1	20.2	5.2	18.4	ns
t <sub>PLH</sub>	A. P. or C	W	5.4	21.6	5.6	19.6	ns
t <sub>PHL</sub>	A, B, or C	VV	5.4	21.6	5.6	19.6	115
t <sub>PLH</sub>	G	Y	3	12.1	3.1	11	20
t <sub>PHL</sub>	G	ř	3	12.1	3.1	11	ns

<sup>(2)</sup> Additional quiescent supply current per input pin, TTL inputs high, 1 unit load



over recommended operating free-air temperature range,  $V_{CC}$  = 5 V ± 0.5 V,  $C_L$  = 50 pF (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	METER FROM (INPUT) TO (OUTPUT)		-55°C to	125°C	-40°C to	85°C	UNIT
PARAMETER	PROW (INPUT)	10 (001701)	MIN	MAX	MIN	MAX	ONII
t <sub>PLH</sub>	<u></u>	10/	3.4	13.5	3.5	12.3	no
t <sub>PHL</sub>	G	W	3.4	13.5	3.5	12.3	ns

## **4.7 Operating Characteristics**

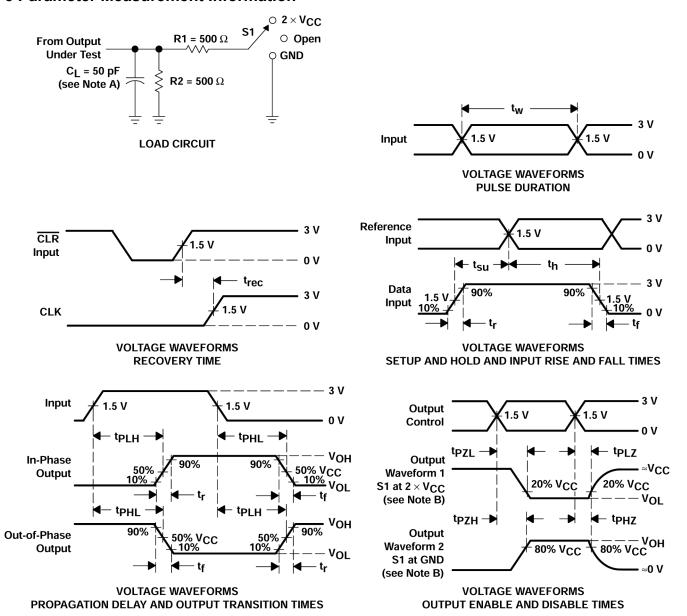
 $V_{CC} = 5 \text{ V}, T_{A} = 25^{\circ}\text{C}$ 

PARAMETER	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	120	pF

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#### **5 Parameter Measurement Information**



- A. C<sub>L</sub> includes probe and test-fixture capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_0 = 50 \Omega$ ,  $t_r = 3$  ns. Phase relationships between waveforms are arbitrary.
- D. For clock inputs,  $f_{\text{max}}$  is measured with the input duty cycle at 50%.
- E. The outputs are measured one at a time with one input transition per measurement.
- F.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- G.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- H. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
- I. All parameters and waveforms are not applicable to all devices.

Figure 5-1. Load Circuit and Voltage Waveforms



TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	2 × V <sub>CC</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND



## **6 Detailed Description**

#### **6.1 Overview**

The CDx4ACT151 is a high speed silicon gate CMOS multiplexer well suited to multiplexing and data routing applications. It contains a single 8:1 multiplexer.

The CDx4ACT151 operates asynchronously, with the Y output being equal to the input selected by the address inputs (A, B, C). The W output is always the inverse of the Y output.

The strobe  $(\overline{G})$  input forces the Y output low, and the W output high, regardless of the state of other inputs.

## 6.2 Functional Block Diagram

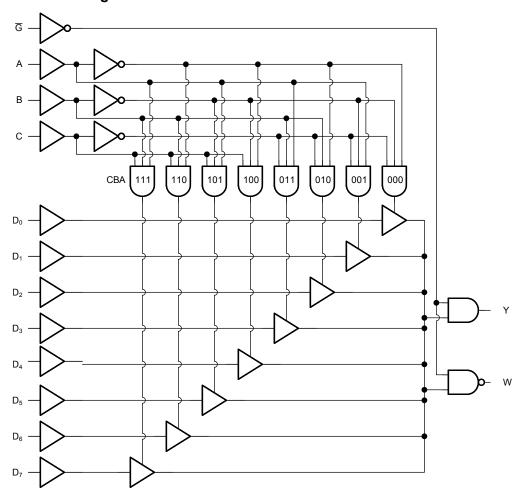


Figure 6-1. Logic Diagram (Positive Logic) for CDx4ACT151



#### 6.3 Feature Description

#### 6.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important to limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

#### 6.3.2 TTL-Compatible CMOS Inputs

This device includes TTL-compatible CMOS inputs. These inputs are specifically designed to interface with TTL logic devices by having a reduced input voltage threshold.

TTL-compatible CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law  $(R = V \div I)$ .

TTL-compatible CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the *Implications of Slow or Floating CMOS Inputs* application report.

Do not leave TTL-compatible CMOS inputs floating at any time during operation. Unused inputs must be terminated at  $V_{CC}$  or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a  $10k\Omega$  resistor is recommended and typically will meet all requirements.

#### 6.3.3 Clamp Diode Structure

As shown in Figure 6-2, the inputs and outputs to this device have both positive and negative clamping diodes.

## **CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

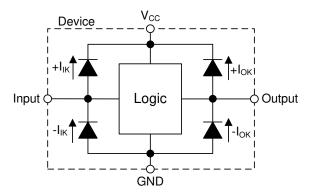


Figure 6-2. Electrical Placement of Clamping Diodes for Each Input and Output



#### **6.4 Device Functional Modes**

Function Table lists the functional modes of the CDx4ACT151.

**Table 6-1. Function Table** 

	INPU	OUTP	UTS <sup>(2)</sup>		
	SELECT		STROBE	Υ	w
С	В	Α	G	ı	vv
Х	X	Χ	Н	L	Н
L	L	L	L	D0	D0
L	L	Н	L	D1	D1
L	Н	L	L	D2	D2
L	Н	Н	L	D3	D3
Н	L	L	L	D4	D4
Н	L	Н	L	D5	D5
Н	Н	L	L	D6	<del>D</del> 6
Н	Н	Н	L	D7	D7

<sup>(1)</sup> 

H = High Voltage Level, L = Low Voltage Level, X = Don't Care H = Driving High, L = Driving Low, Dx = Driving same value as Dx input,  $\overline{Dx}$  = Driving inverted value from Dx input



## 7 Application and Implementation

#### **Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 7.1 Application Information

The CDx4ACT151 is an 8-to-1 data selector/multiplexer. This application shows an example of using the device with all required connections.

## 7.2 Typical Application

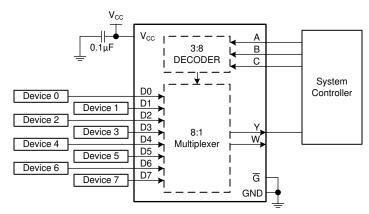


Figure 7-1. Typical Application Block Diagram

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#### 7.2.1 Design Requirements

#### 7.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the CDx4ACT151 plus the maximum static supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through  $V_{CC}$  listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the CDx4ACT151 plus the maximum supply current, I<sub>CC</sub>, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The CDx4ACT151 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The CDx4ACT151 can drive a load with total resistance described by  $R_L \ge V_O / I_O$ , with the output voltage and current defined in the *Electrical Characteristics* table with  $V_{OH}$  and  $V_{OL}$ . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the  $V_{CC}$  pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear* and Logic (SLL) Packages and Devices.

#### **CAUTION**

The maximum junction temperature,  $T_{J(max)}$  listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.



#### 7.2.1.2 Input Considerations

Input signals must cross  $V_{IL(max)}$  to be considered a logic LOW, and  $V_{IH(min)}$  to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either  $V_{CC}$  or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the CDx4ACT151 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A  $10k\Omega$  resistor value is often used due to these factors.

The CDx4ACT151 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the Feature Description section for additional information regarding the inputs for this device.

#### 7.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the  $V_{OH}$  specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OL}$  specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V<sub>CC</sub> or ground.

Refer to the Feature Description section for additional information regarding the outputs for this device.

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## 7.2.2 Detailed Design Procedure

- Add a decoupling capacitor from V<sub>CC</sub> to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V<sub>CC</sub> and GND pins. An example layout is shown in the *Layout* section.
- 2. Ensure the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the CDx4ACT151 to one or more of the receiving devices.
- 3. Ensure the resistive load at the output is larger than  $(V_{CC} / I_{O(max)})\Omega$ . Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in M $\Omega$ ; much larger than the minimum calculated previously.
- 4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

#### 7.2.3 Application Curve

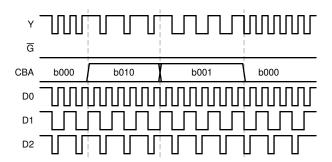


Figure 7-2. Application Timing Diagram



### 7.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A  $0.1\mu F$  capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The  $0.1\mu F$  and  $1\mu F$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

#### 7.4 Layout

#### 7.4.1 Layout Guidelines

- · Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - Parallel traces must be separated by at least 3x dielectric thickness
  - For traces longer than 12cm
    - · Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - · Avoid branches; buffer each signal that must branch separately

#### 7.4.2 Layout Example

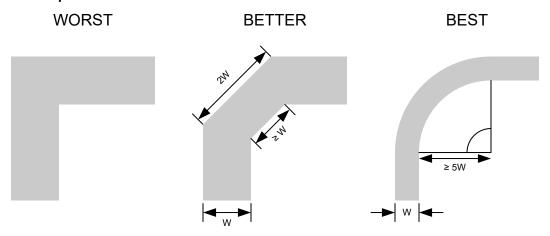


Figure 7-3. Example Trace Corners for Improved Signal Integrity



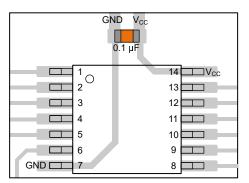


Figure 7-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

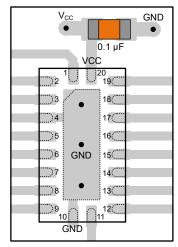


Figure 7-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

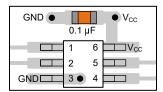


Figure 7-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages



Figure 7-7. Example Damping Resistor Placement for Improved Signal Integrity



## 8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 8.1 Documentation Support

#### 8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, CMOS Power Consumption and Cpd Calculation application report
- Texas Instruments, *Designing With Logic* application report
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application report

## 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.3 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### 8.4 Trademarks

TI E2E<sup>™</sup> is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

#### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 8.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

### 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

С	hanges from Revision A (August 2024) to Revision B (May 2025)	Page
•	Changed the key graphic on the first page of the data sheet	1
•	Added Overview section, Feature Description section, Application Information section, and Typical Application section.	1
•	Added BQB and PW packages to Pin Configuration and Functions	
	Added BQB and PW packages to Thermal Information	

Submit Document Feedback



Changes from Revision * (March 2003) to Revision A (August 2024)
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Page

•	Added Device Information table, Pin Functions table, ESD Ratings table, Thermal Information table, Device	
	Functional Modes, Application and Implementation section, Device and Documentation Support section, and	b
	Mechanical, Packaging, and Orderable Information section	. 1
	Undated RAJA values: D = 73 to 119.9, all values in °C/W	4

# 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
	(-)	(=)			(-)	(4)	(5)		(-)
CD54ACT151F3A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54ACT151F3A
CD54ACT151F3A.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54ACT151F3A
CD74ACT151BQBR	Active	Production	WQFN (BQB)   16	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AD151
CD74ACT151M96	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT151M
CD74ACT151M96.A	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT151M
CD74ACT151PWR	Active	Production	TSSOP (PW)   16	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-55 to 125	AD151

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

## PACKAGE OPTION ADDENDUM

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#### OTHER QUALIFIED VERSIONS OF CD54ACT151, CD74ACT151:

Military : CD54ACT151

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

• Military - QML certified for Military and Defense Applications

# **PACKAGE MATERIALS INFORMATION**

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## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74ACT151BQBR	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
CD74ACT151M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74ACT151PWR	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1



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## \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74ACT151BQBR	WQFN	BQB	16	3000	210.0	185.0	35.0
CD74ACT151M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74ACT151PWR	TSSOP	PW	16	3000	353.0	353.0	32.0

# D (R-PDS0-G16)

## PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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PLASTIC QUAD FLAT PACK-NO LEAD



#### NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



PLASTIC QUAD FLAT PACK-NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLAT PACK-NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



#### 14 LEADS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



SMALL OUTLINE PACKAGE



#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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