







CD54ACT138, CD74ACT138 SCHS329C - JANUARY 2003 - REVISED JULY 2024

CDx4ACT138 3-Line to 8-Line Decoders/Demultiplexers

1 Features

- Inputs are TTL-voltage compatible
- Speed of bipolar F, AS, and S, with significantly reduced power consumption
- Designed specifically for high-speed memory decoders and data-transmission systems
- Incorporate three enable inputs to simplify cascading and/or data reception
- Balanced propagation delays
- ±24mA output drive current
 - Fanout to 15 F devices
- SCR-latchup-resistant CMOS process and circuit
- Exceeds 2kV ESD protection per MIL-STD-883, method 3015

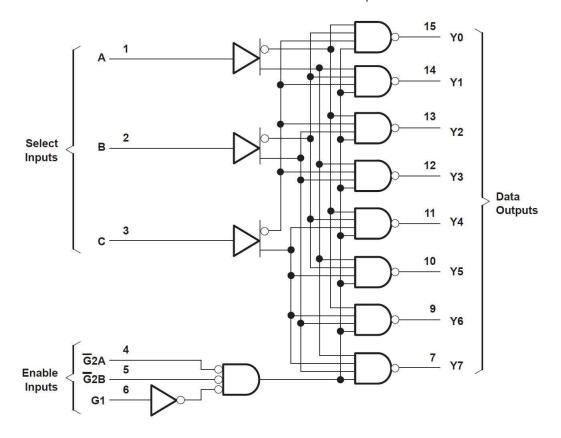
2 Description

The 'ACT138 decoders/demultiplexers are designed for high-performance memory-decoding and dataapplications that require short propagation-delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding.

Device Information

PART NUMBER	BER PACKAGE ⁽¹⁾ PACKAGE SIZE ⁽²⁾		BODY SIZE(3)
	BQB (WQFN, 16)	3.5mm × 2.5mm	3.5mm × 2.5mm
CDx4ACT138	D (SOIC, 16)	9.9mm × 6mm	9.9mm × 3.9mm
	N (PDIP, 16)	19.3mm × 9.4mm	19.3mm × 6.35mm
	PW (TSSOP, 16)	5.00mm × 6.4mm	5.00mm × 4.40mm

- For more information, see Section 10.
- The package size (length × width) is a nominal value and includes pins, where applicable.
- (3)The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)



Table of Contents

1 Features	1	6.3 Device Functional Modes	8
2 Description	1	7 Application and Implementation	10
3 Pin Configuration and Functions		7.1 Application Information	10
4 Specifications		7.2 Power Supply Recommendations	12
4.1 Absolute Maximum Ratings		7.3 Layout	
4.2 ESD Ratings		8 Device and Documentation Support	13
4.3 Recommended Operating Conditions	4	8.1 Documentation Support (Analog)	
4.4 Thermal Information	4	8.2 Receiving Notification of Documentation Updates	13
4.5 Electrical Characteristics	5	8.3 Support Resources	13
4.6 Switching Characteristics	5	8.4 Trademarks	13
4.7 Operating Characteristics	5	8.5 Electrostatic Discharge Caution	13
5 Parameter Measurement Information		8.6 Glossary	
6 Detailed Description		9 Revision History	
6.1 Overview	8	10 Mechanical, Packaging, and Orderable	
6.2 Functional Block Diagram	8	Information	14
-			



3 Pin Configuration and Functions

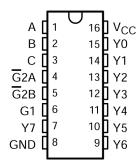


Figure 3-1. CD54ACT138 J Package; CD74ACT138 D, N, or PW Package; 16-Pin CDIP, SOIC, PDIP, or TSSOP (Top View)

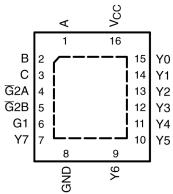


Figure 3-2. CD74ACT138 BQB Package, 16-Pin WQFN (Top View)

Table 3-1. Pin Functions

	PIN TYPE ⁽¹⁾		DESCRIPTION			
NAME	NO.	ITPE	DESCRIPTION			
A	1	I	Input A			
В	2	I	Input B			
С	3	I	Input C			
G2A	4	I	Strobe Input 2A, active low			
G2B	5	1	Strobe Input 2B, active low			
G1	6	I	Strobe Input			
Y7	7	0	Output 7			
GND	8	G	Ground			
Y6	9	0	Output 6			
Y5	10	0	Output 5			
Y4	11	0	Output 4			
Y3	12	0	Output 3			
Y2	13	0	Output 2			
Y1	14	0	Output 1			
Y0	15	0	Output 0			
V _{CC}	16	Р	Positive Supply			

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.



4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	6	V
I _{IK} (2)	Input clamp current	$(V_I < 0 \text{ V or } V_I > V_{CC})$		±20	mA
I _{OK} (2)	Output clamp current	$(V_O < 0 \text{ V or } V_O > V_{CC})$		±50	mA
Io	Continuous output current	$(V_O > 0 \text{ V or } V_O < V_{CC})$		±50	mA
	Continuous current through V _{CC} or GND			±100	mA
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		T _A =	T _A = 25°C		-55°C to 125°C		-40°C to 85°C	
		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		2		V
V _{IL}	Low-level input voltage		0.8		8.0		0.8	V
VI	Input voltage	0	V _{CC}	0	V _{CC}	0	V _{CC}	V
Vo	Output voltage	0	V _{CC}	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		-24		-24		-24	mA
I _{OL}	Low-level output current		24		24		24	mA
Δt/Δν	Input transition rise or fall rate		10		10		10	ns/V

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

4.4 Thermal Information

THERMAL METRIC(1)			CD74ACT138				
		BQB (WQFN)	D (SOIC)	N (PDIP)	PW (TSSOP)	UNIT	
		16 PINS	16 PINS	16 PINS	16 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.9	106.6	67	126.2	°C/W	

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

Submit Document Feedback

Copyright © 2024 Texas Instruments Incorporated

²⁾ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.



4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	R TEST CONDITIONS		V	TA = 2	5 °C	-55°C to	125°C	-40°C to	85°C	UNIT
PARAMETER	1231 00	NDITIONS	V _{CC}	MIN	MAX	MIN	MAX	MIN	MAX	UNII
		Ι _{ΟΗ} = -50 μΑ	4.5 V	4.4		4.4		4.4		
\ <u>\</u>	$V_I = V_{IH}$ or V_{IL}	I _{OH} = -24 mA	4.5 V	3.94		3.7		3.8		V
V _{OH}	VI - VIH OI VIL	$I_{OH} = -50 \text{ mA}^{(1)}$	5.5 V			3.85				v
		$I_{OH} = -75 \text{ mA}^{(1)}$	5.5 V					3.85		
		I _{OL} = 50 μA	4.5 V		0.1		0.1		0.1	
\ <u>\</u>	V V 27V	I _{OL} = 24 mA	4.5 V		0.36		0.5		0.44	
V _{OL}	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 50 \text{ mA}^{(1)}$	5.5 V				1.65			v
		$I_{OL} = 75 \text{ mA}^{(1)}$	5.5 V						1.65	
I _I	V _I = V _{CC} or GND		5.5 V		±0.1		±1		±1	μA
I _{cc}	$V_I = V_{CC}$ or GND,	I _O = 0	5.5 V		8		160		80	μA
ΔI _{CC} (2)	V _I = V _{CC} - 2.1 V		4.5 V to 5.5 V		2.4		3		2.8	mA
C _i					10		10		10	PF

⁽¹⁾ Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

(2) Additional quiescent supply current per input pin, TTL inputs high, 1 unit load

Table 4-1. Act Input Load Table

INPUT	UNIT LOAD
A, B, or C	0.83
G2A or G2B	1
G1	0.42

4.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5V ± 0.5V, C_L = 50pF (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	EDOM (INDLIT)	TO (OUTPUT)	-55°C to	125°C	-40°C to 8	5°C	UNIT
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	MIN	MAX	ONII
t _{PLH}	A, B, C	Any V	3	12	3.1	10.9	no
t _{PHL}	А, Б, С	Any Y	3	12	3.1	10.9	ns
t _{PLH}	G1	Any V	2.8	11	2.8	10	no
t _{PHL}	91	Any Y	2.8	11	2.8	10	ns
t _{PLH}	G2A, G2B	Any V	2.6	10.5	2.7	9.5	no
t _{PHL}	G2A, G2B	Any Y	2.6	10.5	2.7	9.5	ns

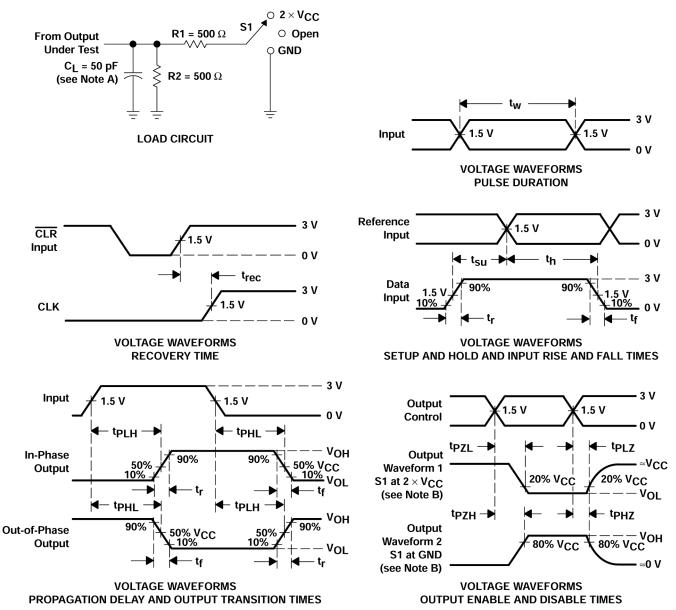
4.7 Operating Characteristics

 $V_{CC} = 5V, T_A = 25^{\circ}C$

PARAMETER			UNIT
C _{pd}	Power dissipation capacitance	110	pF



5 Parameter Measurement Information



- A. C_L includes probe and test-fixture capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_r = 3$ ns, $t_f = 3$ ns. Phase relationships between waveforms are arbitrary.
- D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
- E. The outputs are measured one at a time with one input transition per measurement.
- F. t_{PLH} and t_{PHL} are the same as t_{pd} .
- G. t_{PZL} and t_{PZH} are the same as t_{en} .
- H. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- I. All parameters and waveforms are not applicable to all devices.

Figure 5-1. Load Circuit and Voltage Waveforms



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	2 × V _{CC}
t _{PHZ} /t _{PZH}	GND

6 Detailed Description

6.1 Overview

When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications (see Application Information).

6.2 Functional Block Diagram

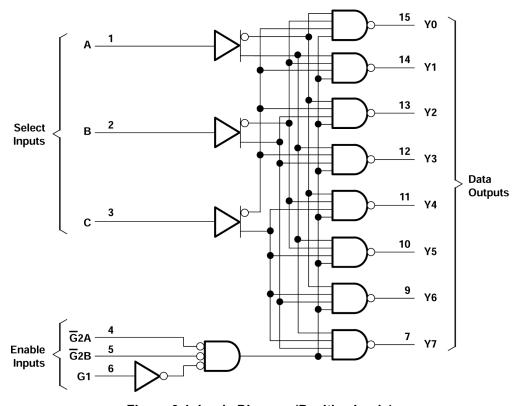


Figure 6-1. Logic Diagram (Positive Logic)

6.3 Device Functional Modes

Table 6-1. Function Table

ENABLE INPUTS SELECT INPUTS							OUTPUTS								
G1	G2A	G2B	С	В	Α	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7		
X	Н	X	Х	Х	Х	Н	Н	Н	Н	Н	Н	Н	Н		
Х	X	Н	Х	Х	X	Н	Н	Н	Н	Н	Н	Н	Н		
L	Х	X	Х	Х	Х	Н	Н	Н	Н	Н	Н	Н	Н		
Н	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н		
Н	L	L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н		
Н	L	L	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н		
Н	L	L	L	Н	Н	Н	Н	Н	L	Н	Н	Н	Н		
Н	L	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н		
Н	L	L	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н		



Table 6-1. Function Table (continued)

	ENABLE IN	PUTS	5	ELECT	INPUTS				OUT	PUTS			
G1	G2A	G2B	С	В	Α	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
Н	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н
Н	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L



7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

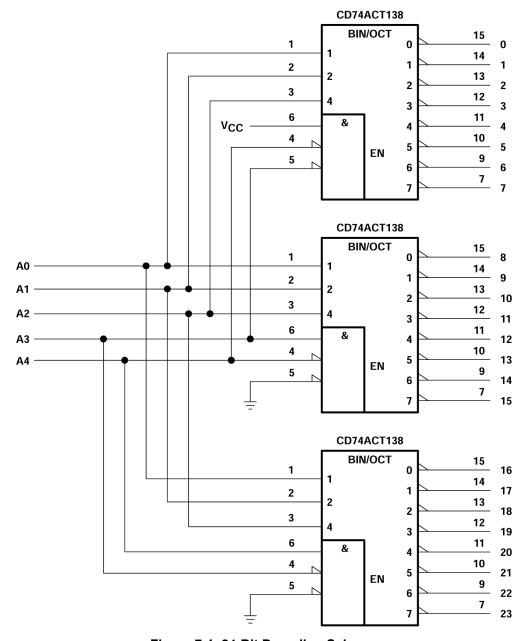


Figure 7-1. 24-Bit Decoding Scheme



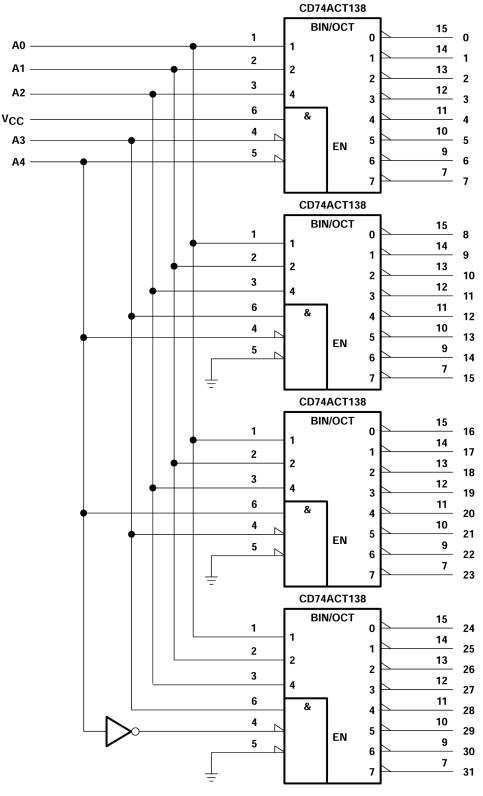


Figure 7-2. 32-Bit Decoding Scheme

7.2 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A $0.1\mu F$ capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The $0.1\mu F$ and $1\mu F$ capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

7.3 Layout

7.3.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

7.3.2 Layout Example

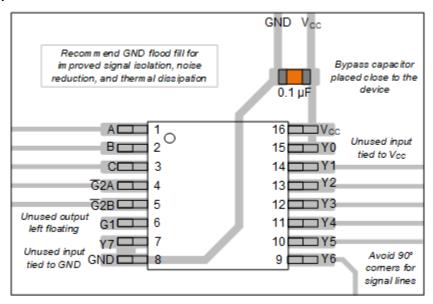


Figure 7-3. Example Layout for the CD74ACT138



8 Device and Documentation Support

8.1 Documentation Support (Analog)

8.1.1 Related Documentation

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY	
CD54ACT138	Click here	Click here	Click here	Click here	Click here	
CD74ACT138	Click here	Click here	Click here	Click here	Click here	

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

Changes from Revision B (April 2024) to Revision C (July 2024)

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

9 Revision History



10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

www.ti.com 31-Oct-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
CD54ACT138F3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54ACT138F3A
CD54ACT138F3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54ACT138F3A
CD74ACT138BQBR	Active	Production	WQFN (BQB) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AD138
CD74ACT138BQBR.A	Active	Production	WQFN (BQB) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AD138
CD74ACT138E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74ACT138E
CD74ACT138E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74ACT138E
CD74ACT138M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	ACT138M
CD74ACT138M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT138M
CD74ACT138M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT138M
CD74ACT138M96G4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT138M
CD74ACT138PWR	Active	Production	TSSOP (PW) 16	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	AD138
CD74ACT138PWR.A	Active	Production	TSSOP (PW) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AD138

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

www.ti.com 31-Oct-2025

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54ACT138, CD74ACT138:

Catalog: CD74ACT138

Military: CD54ACT138

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

www.ti.com 6-Nov-2025

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74ACT138BQBR	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
CD74ACT138M96	SOIC	D	16	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
CD74ACT138M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74ACT138PWR	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

www.ti.com 6-Nov-2025



*All dimensions are nominal

7 till dillitoriolorio di o riorriiridi							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74ACT138BQBR	WQFN	BQB	16	3000	210.0	185.0	35.0
CD74ACT138M96	SOIC	D	16	2500	340.5	336.1	32.0
CD74ACT138M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74ACT138PWR	TSSOP	PW	16	3000	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

www.ti.com 6-Nov-2025

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74ACT138E	N	PDIP	16	25	506	13.97	11230	4.32
CD74ACT138E	N	PDIP	16	25	506	13.97	11230	4.32
CD74ACT138E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74ACT138E.A	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



INSTRUMENTS www.ti.com

PLASTIC QUAD FLAT PACK-NO LEAD



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



PLASTIC QUAD FLAT PACK-NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLAT PACK-NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



14 LEADS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025