CD54ACT112, CD74ACT112 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

SCHS323 - JANUARY 2003

- Inputs Are TTL-Voltage Compatible
- Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption
- Balanced Propagation Delays
- ±24-mA Output Drive Current
 - Fanout to 15 F Devices
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015

CD54ACT112...F PACKAGE CD74ACT112 . . . M PACKAGE (TOP VIEW) 16 VCC 1CLK [1K **∏** 15 1 1 CLR 1J [14 2 2 CLR 1PRE [4 13 2CLK 1Q 🛮 5 12 2K 1Q 11 **∏** 2J $2\overline{Q}$ 10 2PRE 9 2Q GND [

description/ordering information

The 'ACT112 devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset (\overline{PRE}) or clear (\overline{CLR}) inputs sets or resets the outputs, regardless of the levels of the other inputs. When \overline{PRE} and \overline{CLR} are inactive (high), data at the J and K inputs meeting the setup-time requirements is transferred to the outputs on the negative-going edge of the clock pulse (CLK). Clock triggering occurs at a voltage level and is not directly related to the fall time of the clock pulse. Following the hold-time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

ORDERING INFORMATION

TA	PACKA	GE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	SOIC – M	Tube	CD74ACT112M	ACT112M
–55°C to 125°C	SOIC - IVI	Tape and reel	CD74ACT112M96	ACTITZIVI
	CDIP – F	Tube	CD54ACT112F3A	CD54ACT112F3A

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each flip-flop)

		OUTI	OUTPUTS			
PRE	CLR	CLK	J	K	Q	Q
L	Н	Х	Х	Х	Н	L
Н	L	X	Χ	X	L	Н
L	L	X	Χ	X	н‡	н‡
Н	Н	\downarrow	L	L	Q_0	\overline{Q}_0
Н	Н	\downarrow	Н	L	н	L
Н	Н	\downarrow	L	Н	L	Н
Н	Н	\downarrow	Н	Н	Тод	gle
Н	Н	Н	Χ	Χ	Q_0	\overline{Q}_0

Output states are unpredictable if PRE and CLR go high simultaneously after both being low at the same time.



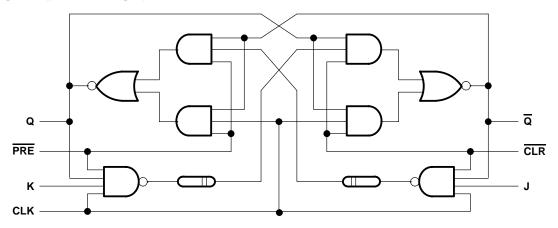
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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}	0.5 V to 6 V
Input clamp current, I _{IK} (V _I < 0 V or V _I > V _{CC}) (see Note 1)	±20 mA
Output clamp current, I _{OK} (V _O < 0 V or V _O > V _{CC}) (see Note 1)	±50 mA
Continuous output current, I_O ($V_O > 0$ V or $V_O < V_{CC}$)	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 2)	73°C/W
Storage temperature range, T _{stq}	. –65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		T _A = 1	T _A = 25°C		–55°C to 125°C		–40°C to 85°C	
		MIN	MAX	MIN	MAX	MIN	MAX	
Vcc	Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	2		2		2		V
VIL	Low-level input voltage		0.8		0.8		0.8	V
VI	Input voltage	0	VCC	0	VCC	0	VCC	V
VO	Output voltage	0	VCC	0	VCC	0	VCC	V
IOH	High-level output current		-24		-24		-24	mA
l _{OL}	Low-level output current		24		24		24	mA
Δt/Δν	Input transition rise or fall rate		10		10		10	ns/V

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST COND	Vcc	T _A = 25°C		–55°C to 125°C		–40°C to 85°C		UNIT		
			MIN	MAX	MIN	MAX	MIN	MAX			
		I _{OH} = -50 μA	4.5 V	4.4		4.4		4.4			
Vou	VI = VIH or VIL	$I_{OH} = -24 \text{ mA}$	4.5 V	3.94		3.7		3.8		V	
VOH	v = v H or v L	$I_{OH} = -50 \text{ mA}^{\dagger}$	5.5 V			3.85				V	
		$I_{OH} = -75 \text{ mA}^{\dagger}$	5.5 V					3.85			
	VI = VIH or VIL	I _{OL} = 50 μA	4.5 V		0.1		0.1		0.1	.1	
\/a.		I _{OL} = 24 mA	4.5 V		0.36		0.5		0.44	٧	
VOL		$I_{OL} = 50 \text{ mA}^{\dagger}$	5.5 V				1.65				
		$I_{OL} = 75 \text{ mA}^{\dagger}$	5.5 V						1.65		
lį	$V_I = V_{CC}$ or GND		5.5 V		±0.1		±1		±1	μΑ	
ICC	$V_I = V_{CC}$ or GND,	IO = 0	5.5 V		4		80		40	μΑ	
ΔlCC	$V_I = V_{CC} - 2.1 \text{ V}$		4.5 V to 5.5 V		2.4		3		2.8	mA	
C _i					10		10		10	pF	

[†] Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

ACT INPUT LOAD TABLE

INPUT	UNIT LOAD
J or CLK	1
К	0.53
CLR or PRE	0.58

Unit Load is ΔI_{CC} limit specified in electrical characteristics table (e.g., 2.4 mA at 25°C).

timing requirements over recommended operating conditions (unless otherwise noted)

				–55°C to 125°C		–40°C to 85°C		
			MIN	MAX	MIN	MAX		
fclock	Clock frequency			100		114	MHz	
	Pulse duration	CLK high or low	5		4.4		ns	
t _W	ruise duration	CLR or PRE low	5.5		4.8		115	
t _{su}	Setup time, before CLK↓	J or K	4		3.5		ns	
t _h	Hold time, after CLK↓	J or K	1		1		ns	
t _{rec}	Recovery time, before CLK↓	CLR↑ or PRE↑	2.5		2.2		ns	

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–55°(125		–40°C to 85°C		UNIT
	(111 01)	(6611 61)	MIN	MAX	MIN	MAX	
f _{max}			100		114		MHz
+ =	CLK	2.6	10.3	2.7	9.4	no	
^t PLH	CLR or PRE	Q or Q	3.1	12.2	3.2	11.1	ns
CLK TPHL CLR or PRE	Q or \overline{Q}	2.6	10.3	2.7	9.4		
	CLR or PRE	3013	3.1	12.2	3.2	11.1	ns

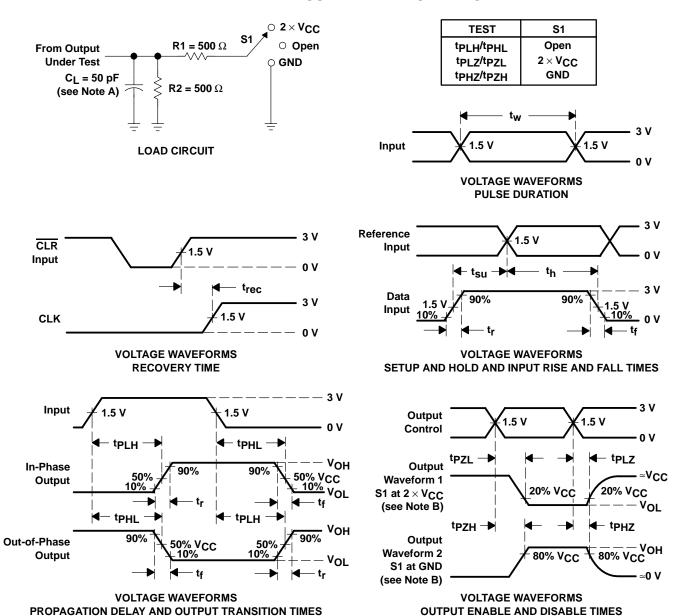
operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER T				
C _{pd}	Power dissipation capacitance	56	pF		



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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \ \Omega$, $t_f = 3 \ ns$, $t_f = 3 \ ns$. Phase relationships between waveforms are arbitrary.
- D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
- E. The outputs are measured one at a time with one input transition per measurement.
- F. tpLH and tpHL are the same as tpd.
- G. t_{PZL} and t_{PZH} are the same as t_{en} .
- H. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- I. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)			(6)
						(4)	(5)		
CD54ACT112F3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54ACT112F3A
CD54ACT112F3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54ACT112F3A
CD74ACT112M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	ACT112M
CD74ACT112M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT112M
CD74ACT112M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT112M

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

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OTHER QUALIFIED VERSIONS OF CD54ACT112, CD74ACT112:

Military: CD54ACT112

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

• Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74ACT112M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

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*All dimensions are nominal

	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ı	CD74ACT112M96	SOIC	D	16	2500	340.5	336.1	32.0

D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



14 LEADS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

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