

# **CDx4ACT05 Hex Inverters With Open-Drain Outputs**

#### 1 Features

- Inputs are TTL-voltage compatible
- Speed of bipolar F, AS, and S, with significantly reduced power consumption
- Fanout to 15 F devices
- SCR-latchup-resistant CMOS process and circuit
- Exceeds 2kV ESD protection per MIL-STD-883, method 3015

# 2 Description

The 'ACT05 devices independent contain inverters.

#### **Device Information**

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE(2)	BODY SIZE(3)
CD54ACT05 J (CDIP, 14)		19.55mm x 7.9mm	19.55 mm x 6.7mm
	BQA (WQFN, 14)	3mm × 2.5mm	3mm × 2.5mm
CD74ACT05	D (SOIC, 14)	8.65mm × 6mm	8.65mm × 3.9mm
CD74AC103	N (PDIP, 14)	19.3mm × 9.4mm 19.3mm × 6.3	
	PW (TSSOP, 14)	5mm × 6.4mm	5mm × 4.4mm

- For more information, see Section 10.
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.





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# 3 Pin Configuration and Functions

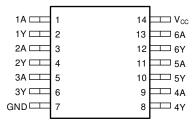


Figure 3-1. CD54ACT05 J Package, 14-Pin CDIP; CD74ACT05 D, N, or PW Package; 14-Pin SOIC, PDIP, or TSSOP (Top View)

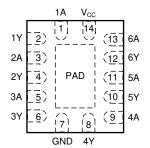


Figure 3-2. CD74ACT05 BQA Package, 14-Pin WQFN

Table 3-1. Pin Functions

PIN				
NAME	CD74ACT05	CD54ACT05	I/O <sup>(1)</sup>	DESCRIPTION
NAME	BQA, D, N, PW	J		
1A	1	1	I	1A Input
1Y	2	2	0	1Y Output
2A	3	3	I	2A Input
2Y	4	4	0	2Y Output
3A	5	5	I	3A Input
3Y	6	6	0	3Y Output
GND	7	7	_	Ground Pin
4Y	8	8	0	4Y Output
4A	9	9	I	4A Input
5Y	10	10	I	5Y Output
5A	11	11	I	5A Input
6Y	12	12	0	6Y Output
6A	13	13	I	6A Input
V <sub>CC</sub>	14	14	_	Power Pin
NC	_	_	_	No Connection
Thermal pad			_	Connect the GND pin to the exposed thermal pad for correct operation. Connect the thermal pad to any internal PCB ground plane using multiple vias for good thermal performance.

(1) I = input, O = output, P = power, FB = feedback, GND = ground, N/A = not applicable



# 4 Specifications

## 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		·	MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		-0.5	6	V
I <sub>IK</sub>	Input clamp current <sup>(2)</sup>	< 0 or V <sub>I</sub> > V <sub>CC</sub>		±20	mA
I <sub>OK</sub>	Output clamp current <sup>(2)</sup>	0 < 0		-50	mA
I <sub>O</sub>	Continuous current			±50	mA
T <sub>stg</sub>	Storage temperature range		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 4.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V

<sup>(1)</sup> JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		T <sub>A</sub> =	T <sub>A</sub> = 25°C		TO C	–55°C TO 125°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		2		V
V <sub>IL</sub>	Low-level input voltage		8.0		0.8		0.8	V
VI	Input voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
Vo	Output voltage	0	5.5	0	5.5	0	5.5	V
I <sub>OL</sub>	Low-level output current		24		24		24	mA
Δt/Δν	Input transition rise or fall rate		10		10		10	ns/V

<sup>(1)</sup> All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

#### 4.4 Thermal Information

			CD74ACT05				
THERMAL METRIC(1)		BQA (WQFN)	D (SOIC)	N (PDIP)	PW (TSSOP)	UNIT	
			14	PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	85.4	89.9	80	132.2	°C/W	

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

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<sup>(2)</sup> The input and output negative voltage ratings may be exceeded if the input and output current ratings are observed.

#### 4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>cc</sub>	T <sub>A</sub> = 2	5°C	–40°C 85°	_	–55°C 125°	-	UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
		I <sub>OL</sub> = 50 mA	4.5 V		0.1		0.1		0.1	
N/	$V_{I} = V_{IH}$ or $V_{IL}$	I <sub>OL</sub> = 24 mA	4.5 V		0.36		0.44		0.5	v
$V_{OL}$ $V_{I} =$	AI - AIH OI AIF	$I_{OL} = 50 \text{ mA}^{(1)}$	5.5 V						1.65	v
		$I_{OL} = 75 \text{ mA}^{(1)}$	5.5 V				1.65			
I <sub>I</sub>	$V_I = V_{CC}$ or GND		5.5 V		±0.1		±1		±1	μA
Icc	$V_I = V_{CC}$ or GND,	I <sub>O</sub> = 0	5.5 V		4		40		80	μA
ΔI <sub>CC</sub>	$V_{I} = V_{CC} - 2.1 \text{ V}$		4.5 V to 5.5 V		2.4		2.8		3	mA
C <sub>i</sub>					10		10		10	pF

# Table 4-1. ACT INPUT LOAD TABLE (1)

Input	Unit Load
Α	0.18

 Unit load is ΔI<sub>CC</sub> limit specified in electrical characteristics table (e.g., 2.4 mA at 25°C).

# 4.6 Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC}$  = 5 V ± 0.5 V,  $C_L$  = 50 pF (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C 85°C	-	–55°C 125°	-	UNIT
	(INFOT)	(001701)	MIN	MAX	MIN	MAX	
t <sub>PZL</sub>	A or P	V	2.4	8.5	2.3	9.3	no
t <sub>PLZ</sub>	A or B	Ť	2.8	9.8	2.7	10.8	ns

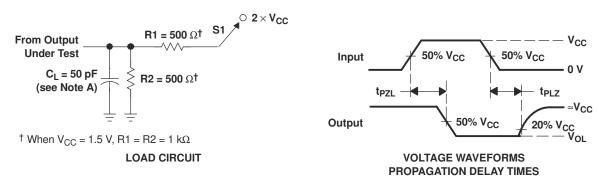
## 4.7 Operating Characteristics

 $V_{CC}$  = 5 V,  $T_A$  = 25°C

	PARAMETER	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	105	pF



## **5 Parameter Measurement Information**



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \ \Omega$ ,  $t_r \leq$  3 ns,  $t_f \leq$  3 ns.
- C. The outputs are measured one at a time, with one input transition per measurement.

Figure 5-1. Load Circuit and Voltage Waveforms

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# **6 Detailed Description**

## **6.1 Overview**

These devices perform the Boolean function  $Y = \overline{A}$ . The open-drain outputs require pullup resistors to perform correctly, and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

# 6.2 Functional Block Diagram



#### **6.3 Device Functional Modes**

# Function Table (Each Inverter)

INPUT A	OUTPUT Y
Н	L
L	Z

## 7 Application and Implementation

#### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 7.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the Section 4.3.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu$ F is recommended; if there are multiple  $V_{CC}$  pins, then 0.01  $\mu$ F or 0.022  $\mu$ F is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu$ F and a 1  $\mu$ F are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

#### 7.2 Layout

#### 7.2.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Layout Example specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the IOs, so they cannot float when disabled.

#### 7.2.2 Layout Example

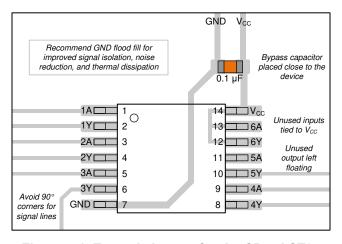


Figure 7-1. Example Layout for the CD74ACT05

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# 8 Device and Documentation Support

## 8.1 Documentation Support (Analog)

#### 8.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY	
CD54ACT05	Click here	Click here	Click here	Click here	Click here	
CD74ACT05	Click here	Click here	Click here	Click here	Click here	

### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.3 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### 8.4 Trademarks

TI E2E<sup>™</sup> is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

#### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 8.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

#### 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

## Changes from Revision D (August 2024) to Revision E (November 2024)

Page

Added BQA and PW packages to *Device Information* table, *Pin Configuration and Functions* section, and *Thermal Information* table......1

# Changes from Revision C (January 2007) to Revision D (August 2024)

Page



# 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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#### **PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-9068601QCA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9068601QC A CD54ACT05F3A
CD54ACT05F3A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9068601QC A CD54ACT05F3A
CD54ACT05F3A.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9068601QC A CD54ACT05F3A
CD74ACT05BQAR	Active	Production	WQFN (BQA)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AD05
CD74ACT05BQAR.A	Active	Production	WQFN (BQA)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AD05
CD74ACT05E	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74ACT05E
CD74ACT05E.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74ACT05E
CD74ACT05EE4	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74ACT05E
CD74ACT05M	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-55 to 125	ACT05M
CD74ACT05M.B	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-55 to 125	ACT05M
CD74ACT05M96	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT05M
CD74ACT05M96.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT05M
CD74ACT05M96.B	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT05M
CD74ACT05M96G4	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT05M
CD74ACT05M96G4.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT05M
CD74ACT05PWR	Active	Production	TSSOP (PW)   14	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-55 to 125	AD05
CD74ACT05PWR.A	Active	Production	TSSOP (PW)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AD05

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

# PACKAGE OPTION ADDENDUM

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(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF CD54ACT05, CD74ACT05:

Catalog: CD74ACT05

Military : CD54ACT05

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

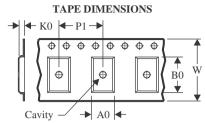
• Military - QML certified for Military and Defense Applications

# **PACKAGE MATERIALS INFORMATION**

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## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74ACT05BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
CD74ACT05M96	SOIC	D	14	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
CD74ACT05M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74ACT05PWR	TSSOP	PW	14	3000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1
CD74ACT05PWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1



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#### \*All dimensions are nominal

7 III GITTOTOTOTO GITO TIOTITICA							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74ACT05BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
CD74ACT05M96	SOIC	D	14	2500	340.5	336.1	32.0
CD74ACT05M96	SOIC	D	14	2500	353.0	353.0	32.0
CD74ACT05PWR	TSSOP	PW	14	3000	366.0	364.0	50.0
CD74ACT05PWR	TSSOP	PW	14	3000	353.0	353.0	32.0

# **PACKAGE MATERIALS INFORMATION**

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## **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74ACT05E	N	PDIP	14	25	506	13.97	11230	4.32
CD74ACT05E	N	PDIP	14	25	506	13.97	11230	4.32
CD74ACT05E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74ACT05E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74ACT05EE4	N	PDIP	14	25	506	13.97	11230	4.32
CD74ACT05EE4	N	PDIP	14	25	506	13.97	11230	4.32

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4040083-5/G





CERAMIC DUAL IN LINE PACKAGE



#### NOTES:

- 1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This package is hermitically sealed with a ceramic lid using glass frit.
- His package is remitted by sealed with a ceramic its using glass mit.
   Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
   Falls within MIL-STD-1835 and GDIP1-T14.



CERAMIC DUAL IN LINE PACKAGE



# N (R-PDIP-T\*\*)

# PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SMALL OUTLINE PACKAGE



#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





SMALL OUTLINE INTEGRATED CIRCUIT



#### NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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PLASTIC QUAD FLAT PACK-NO LEAD



#### NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



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NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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