CDx4AC373, CDx4ACT373 Octal Transparent Latch, 3-State

1 Features

- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5V to 5.5V operation and balanced noise immunity at 30% of the supply
- ±24mA output drive current
  - Fanout to 15 FAST* ICs
  - qDrives 50ohm transmission lines

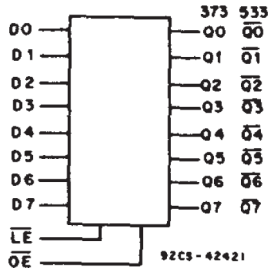
2 Description

The RCA-CDx4AC373 and the CDx4ACT373 octal transparent 3-state latches use the RCA Advanced CMOS technology.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
CDx4AC/ACT373	DW (SOIC, 20)	12.80mm × 10.3mm	12.80mm × 7.50mm
	N (PDIP, 20)	24.33mm × 9.4mm	24.33mm × 6.35mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

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3 Pin Configuration and Functions

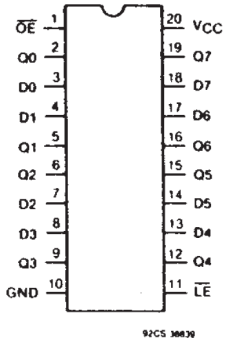


Figure 3-1. CDx4AC373, CDx4ACT373

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{OE}$	1	Input	3-state output enable input
0Q	2	Output	Output for channel 0
0D	3	Input	Input for channel 0
1D	4	Input	Input for channel 1
1Q	5	Output	Output for channel 1
2Q	6	Output	Output for channel 2
2D	7	Input	Input for channel 2
3D	8	Input	Input for channel 3
3Q	9	Output	Output for channel 3
GND	10	—	Ground
$\overline{LE}$	11	Input	Latch enable input (active HIGH)
4Q	12	Output	Output for channel 4
4D	13	Input	Input for channel 4
5D	14	Input	Input for channel 5
5Q	15	Output	Output for channel 5
6Q	16	Output	Output for channel 6
6D	17	Input	Input for channel 6
7D	18	Input	Input for channel 7
7Q	19	Output	Output for channel 7
V_{CC}	20	—	Supply voltage

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply-voltage		-0.5	6	V
I_{IK}	Input diode current	(V_I < -0.5 V or V_I > V_{CC} + 0.5 V)		±20	mA
I_{OK}	Output diode current	(V_O < -0.5 V or V_O > V_{CC} + 0.5 V)		±50	mA
I_O	Output source or sink current per output pin	(V_O > -0.5 V or V_O < V_{CC} + 0.5 V)		±50	mA
	V_{CC} or ground current, I_{CC} or I_{GND}			±100	mA(2)
T_{stg}	Storage temperature		-65	+150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For up to 4 outputs per device; add ± 25 mA for each additional output.

4.2 ESD Ratings

			Value	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	CHARACTERISTIC	MIN	MAX	UNIT
V_{CC} (2)	Supply-voltage			
	AC types	1.5	5.5	V
	ACT types	4.5	5.5	
V_I, V_O	Input or output voltage	0	V_{CC}	V
dt/dv	Input rise and fall slew rate			
	at 1.5 V to 3 V (AC types)	0	50	ns/V
	at 3.6 V to 5.5 V (AC types)	0	20	ns/V
	at 4.5 V to 5.5 V (ACT types)	0	10	ns/V
T_A	Operating-temperature range	-55	+125	°C

(1) All unused inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report: Implications of Slow or Floating CMOS Inputs.
(2) Unless otherwise specified, all voltages are referenced to ground.

4.4 Thermal Information

THERMAL METRIC(1)		CDx4AC/ACT373		UNIT
		N (PDIP)	DW (SOIC)	
		20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50	101.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

4.5 Electrical Characteristics: AC Series

CHARACTERISTICS		TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNIT
					+25		-40 to+85		-55 to +125		
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	High-Level Input Voltage			1.5	1.2	—	1.2	—	1.2	—	V
				3	2.1	—	2.1	—	2.1	—	
				5.5	3.85	—	3.85	—	3.85	—	
V_{IL}	Low-Level Input Voltage			1.5	—	0.3	—	0.3	—	0.3	V
				3	—	0.9	—	0.9	—	0.9	
				5.5	—	1.65	—	1.65	—	1.65	
V_{OH}	High-Level Output Voltage	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
			-0.05	3	2.9	—	2.9	—	2.9	—	
			-0.05	4.5	4.4	—	4.4	—	4.4	—	
			-4	3	2.58	—	2.48	—	2.4	—	
			-24	4.5	3.94	—	3.8	—	3.7	—	
		(1), (2)	-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
V_{IH} or V_{IL}	Low-Level Output Voltage	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
			0.05	3	—	0.1	—	0.1	—	0.1	
			0.05	4.5	—	0.1	—	0.1	—	0.1	
			12	3	—	0.36	—	0.44	—	0.5	
			24	4.5	—	0.36	—	0.44	—	0.5	
		(1), (2)	75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
I_I	Input Leakage Current	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
I_{OZ}	3-State Leakage Current	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
I_{CC}	Quiescent Supply Current, MSI	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

(1) Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
(2) Test verifies a minimum 50-ohm transmission-line-drive capability at +85° C, 75 ohms at +125°C.

4.6 Electrical Characteristics: ACT Series

CHARACTERISTICS		TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNIT
					+25		-40 to+85		-55 to +125		
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	High-level input voltage			4.5 to 5.5	2	—	2	—	2	—	V
V_{IL}	Low-level input voltage			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
V_{OH}	High-level output voltage	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
		(1), (2)	-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	

CHARACTERISTICS		TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNIT
					+25		-40 to+85		-55 to +125		
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	Low-level output voltage	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
		(1), (2)	75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
V_{OH}	Input leakage current	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	
I_{OZ}	3-state leakage current	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
I_{CC}	Quiescent supply current, msi	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
	Additional quiescent supply current per input pin	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	28	—	3	mA
ΔI_{CC}	TTL inputs high										
	1 unit load										

(1) Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
(2) Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C. 75 ohms at +125°C.

Table 4-1. Act Input Loading Table

INPUT	UNIT LOAD(1)	
	ACT373	ACT533
$\overline{OE}$	0.87	0.87
Dn	0.5	0.5
$\overline{LE}$	0.8	08

(1) Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g. 2.4 mA max. @ 25°C.

4.7 Prerequisite for Switching: AC Series

SYMBOL	CHARACTERISTICS	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNIT
			-40 to +85		-55 to +125		
			MIN	MAX	MIN	MAX	
t_W	$\overline{LE}$ Pulse Width	1.5	44	—	50	—	ns
		3.3(1)	4.9	—	5.6	—	
		5(2)	3.5	—	4	—	
t_{SU}	Setup Time Data to $\overline{LE}$	1.5	2	—	2	—	ns
		3.3	2	—	2	—	
		5	2	—	2	—	
t_H	Hold Time Data to $\overline{LE}$	1.5	33	—	38	—	ns
		3.3	3.7	—	4.2	—	
		5	2.6	—	3	—	

(1) 3.3 V: min. is @ 3 V
(2) 5 V: min. is @ 4.5 V

4.8 Switching Characteristics: AC Series

t_r, t_f = 3 ns, C_L = 50 pF

SYMBOL	CHARACTERISTICS	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNIT
			-40 to +85		-55 to+125		
			MIN	MAX	MIN	MAX	
t_{PLH}	Propagation Delays: Data to Qn 373	1.5	—	96	—	106	ns
		3.3[1]	3.1	10.8	3	11.9	
t_{PHL}		5[2]	2.2	7.7	2.1	8.5	
t_{pLH}	533	1.5	—	119	—	131	ns
		3.3	3.8	13.4	3.7	14.7	
t_{PHL}		5	2.7	9.5	2.6	10.5	
t_{PLH}	$\overline{LE}$ on Qn 373	1.5	—	136	—	150	ns
		3.3	4.3	15.2	4.2	16.8	
t_{PHL}		5	3.1	10.9	3	12	
t_{PLH}	533	1.5	—	136	—	150	ns
		3.3	4.3	153	4.2	16.8	
t_{PHL}		5	3.1	10.9	3	12	
t_{PZL}	Output Enable Times	1.5	—	119	—	131	ns
		3.3	4.1	14.4	4	15.8	
t_{PZH}		5	2.7	9.5	2.6	10.5	
t_{PLZ}	Output Disable Times	1.5	—	131	—	144	ns
		3.3	3.7	13.1	3.6	14.4	
t_{PHZ}		5	3	10.5	2.9	11.5	
C_{PD} [3]	Power Dissipation Capacitance	—	63 Typ.		63 Typ.		pF
V_{OHV}	Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	5	4 Typ. @ 25° C				V
V_{OLP}	Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	5	1 Typ. @25° C				V
C_I	Input Capacitance	—	—	10	—	10	pF
C_O	3-State Output Capacitance	—	—	15	—	15	pF

(1) 3.3 V: min. is @ 3.6 V
(2) 5 V: min. is @ 5.5 V
(3) C_{PD} is used to determine the dynamic power consumption, per latch.

4.9 Prerequisite for Switching: ACT Series

SYMBOL	CHARACTERISTICS	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNIT
			-40 to +85		-55 to +125		
			MIN	MAX	MIN	MAX	
t_W	$\overline{LE}$ Pulse Width	5[1]	3.6	—	4	—	ns
t_{SU}	Setup Time Data to $\overline{LE}$	5	2	—	2	—	ns
t_H	Hold Time Data to $\overline{LE}$	5	2.7	—	3	—	ns

(1) 5 V: min. is @ 4.5 V

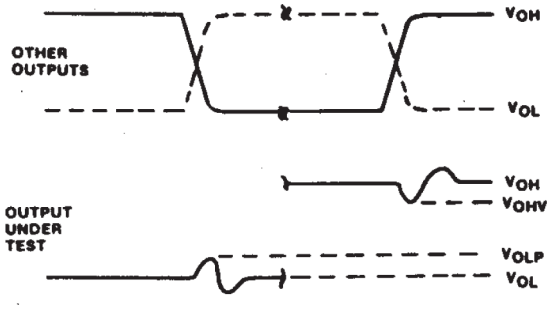
4.10 Switching Characteristics: ACT Series

t_r, t_f = 3 ns, C_L = 50 pF

SYMBOL	CHARACTERISTICS	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNIT
			-40 to +85		-55 to +125		
			MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation Delays: Data to Qn 373	5[1]	2.7	9.5	2.6	10.4	ns
	533		3	10.4	2.9	11.4	
t_{PLH} t_{PHL}	$\overline{LE}$ to Qn 373 533	5	3.1	11.4	3	12.5	ns
t_{PZL} t_{PZH}	Output Enable Times	5	3.5	12.3	3.4	13.5	ns
t_{PLZ} t_{PHZ}	Output Disable Times	5	3.2	11.4	3.1	12.5	ns
C_{PD} [2]	Power Dissipation Capacitance	—	63 Typ.		63 Typ.		pF
V_{OHV}	Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	5	4 Typ. @ 25° C				V
V_{OLP}	Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	5	1 Typ. @25° C				V
C_I	Input Capacitance	—	—	10	—	10	pF
C_O	3-State Output Capacitance	—	—	15	—	15	pF

(1) 5 V: min. is @ 5.5 V
(2) C_{PD} is used to determine the dynamic power consumption, per latch.

5 Parameter Measurement Information



A. V_{OHV} AND V_{OLP} ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
B. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS: PRR ≤ 1 MHz, t_r = 3 ns, t_f = 3 ns, SKEW 1 ns.
C. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD ANO BYPASSED WITH 0.1 *μF* CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.
D. 92CS-42406

Figure 5-1. Simultaneous Switching Transient Waveforms.

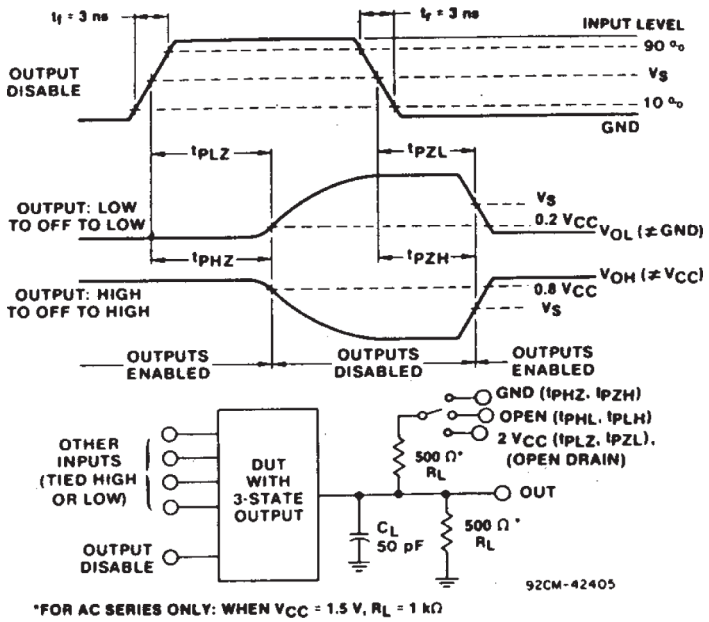


Figure 5-2. Three-state Propagation Delay Waveforms and Test Circuit.

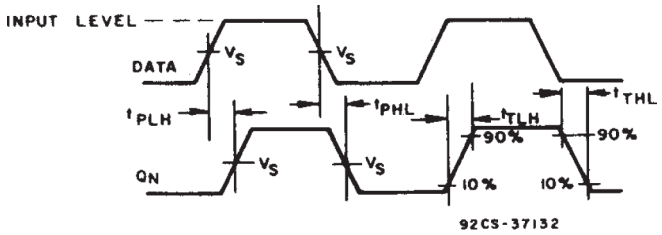


Figure 5-3. Data to Qn Output Propagation Delays and Output Transition Times.

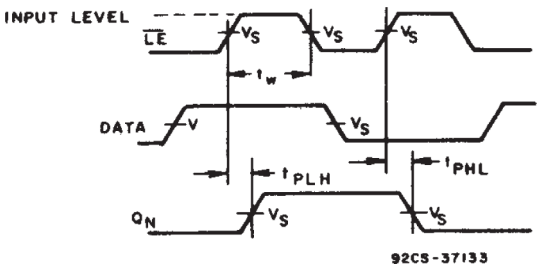


Figure 5-4. Latch Enable Propagation Delays.

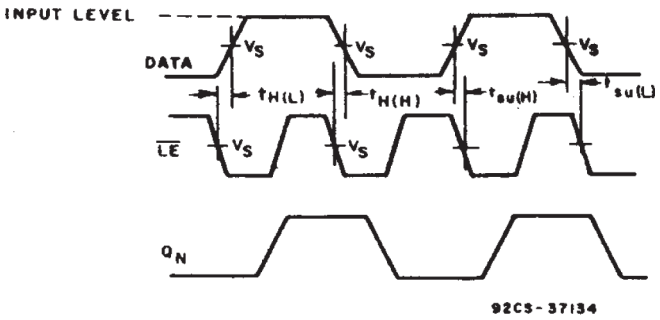


Figure 5-5. Latch Enable Prerequisite Times.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

6 Detailed Description

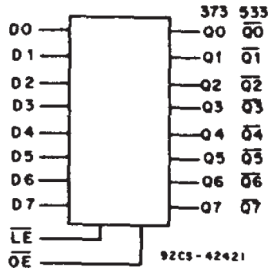
6.1 Overview

The RCA-CD54/74AC373 and the CD54/74ACT373 octal transparent 3-state latches use the RCA ADVANCED CMOS technology. The outputs are transparent to the inputs when the Latch Enable ($\overline{LE}$) is HIGH. When the Latch Enable ($\overline{LE}$) goes LOW, the data is latched. The Output Enable ($\overline{OE}$) controls the 3-state outputs. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high-impedance state. The latch operation is independent of the state of the Output Enable.

The CD74AC/ACT373 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC/ACT373, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

6.2 Functional Block Diagram



6.3 Functional Block Diagram

Table 6-1. Truth Table

$\overline{\text{Output}}$ Enable	$\overline{\text{Latch}}$ Enable	Data	AC/ACT373 Output
L	H	H	H
L	H	L	L
L	L	l	L
L	L	h	H
H	X	X	Z

7 Application and Implementation

7.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µf is recommended; if there are multiple VCC pins, then 0.01 µf or 0.022 µf is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µf and a 1 µf are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

7.2 Layout Guidelines

7.2.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.

8 Device and Documentation Support

8.1 Documentation Support (Analog)

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CD54AC373	Click here	Click here	Click here	Click here	Click here
CD74AC373	Click here	Click here	Click here	Click here	Click here
CD54ACT373	Click here	Click here	Click here	Click here	Click here
CD74ACT373	Click here	Click here	Click here	Click here	Click here

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2002) to Revision A (May 2024)	Page
• Added *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Device Functional Modes, Application and Implementation* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Updated RθJA values: DW = 40 to 101.2, all values in °C/W	5

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD54AC373F3A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54AC373F3A
CD54AC373F3A.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54AC373F3A
CD54ACT373F3A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54ACT373F3A
CD54ACT373F3A.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54ACT373F3A
CD74AC373E	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74AC373E
CD74AC373E.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74AC373E
CD74AC373M	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	-55 to 125	AC373M
CD74AC373M96	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC373M
CD74AC373M96.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC373M
CD74ACT373E	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74ACT373E
CD74ACT373E.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74ACT373E
CD74ACT373M	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	-55 to 125	ACT373M
CD74ACT373M96	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT373M
CD74ACT373M96.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT373M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF CD54AC373, CD54ACT373, CD74AC373, CD74ACT373 :

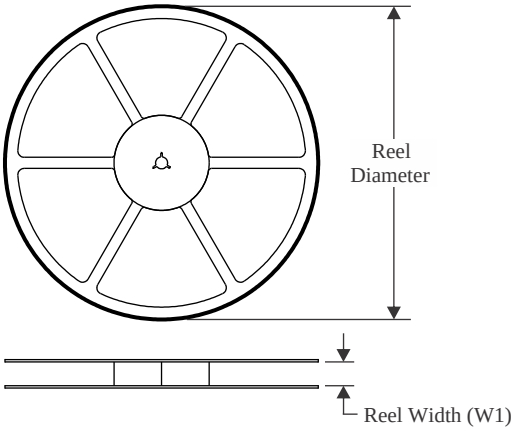
- Catalog : CD74AC373, CD74ACT373
- Military : CD54AC373, CD54ACT373

NOTE: Qualified Version Definitions:

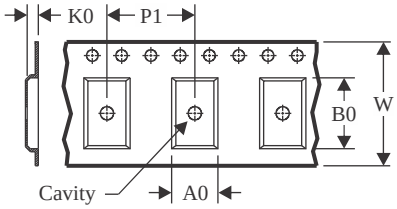
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

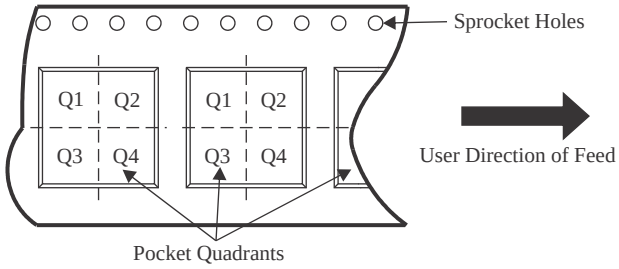


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

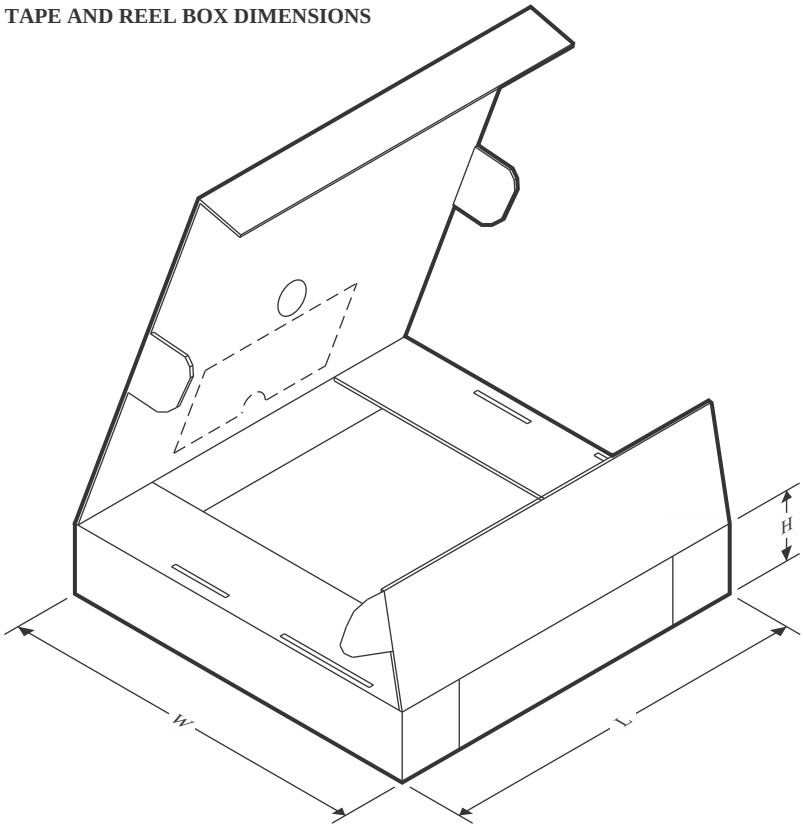
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC373M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74AC373M96	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
CD74ACT373M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

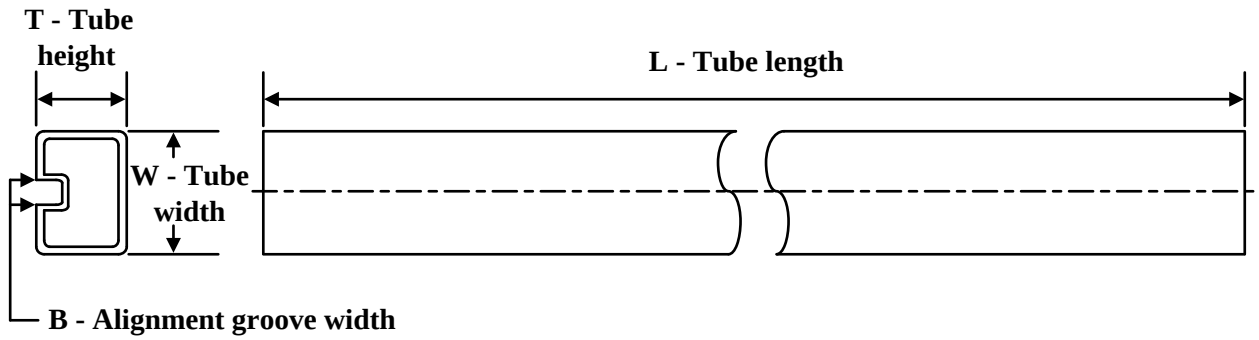
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC373M96	SOIC	DW	20	2000	356.0	356.0	45.0
CD74AC373M96	SOIC	DW	20	2000	356.0	356.0	45.0
CD74ACT373M96	SOIC	DW	20	2000	356.0	356.0	45.0

TUBE



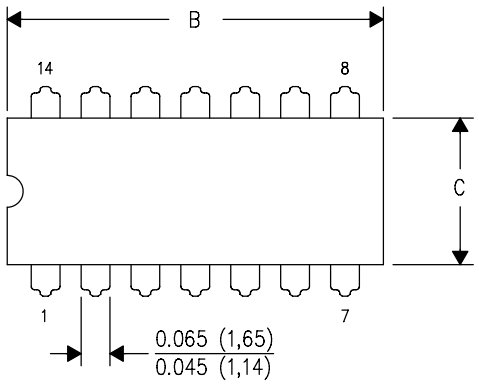
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74AC373E	N	PDIP	20	20	506	13.97	11230	4.32
CD74AC373E.A	N	PDIP	20	20	506	13.97	11230	4.32
CD74ACT373E	N	PDIP	20	20	506	13.97	11230	4.32
CD74ACT373E.A	N	PDIP	20	20	506	13.97	11230	4.32

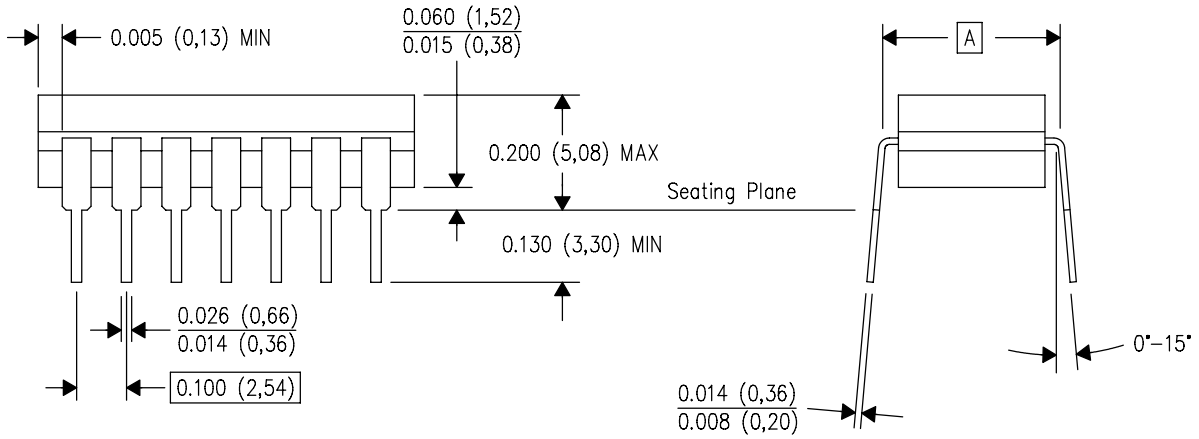
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



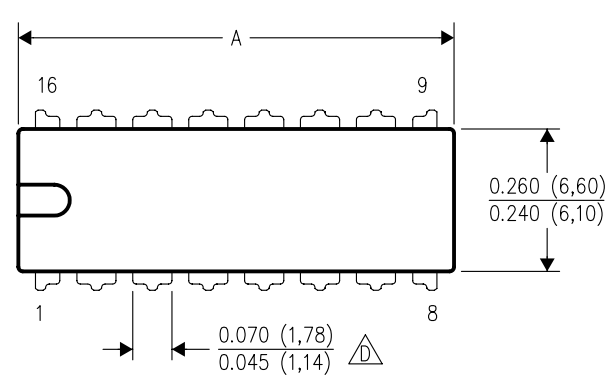
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

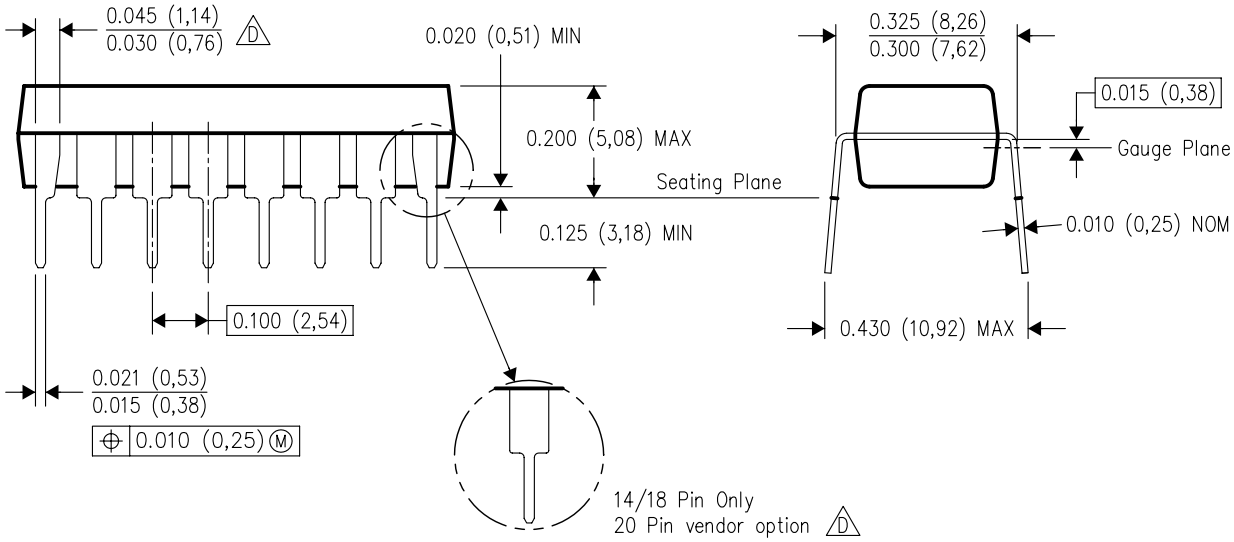
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

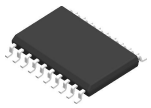


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

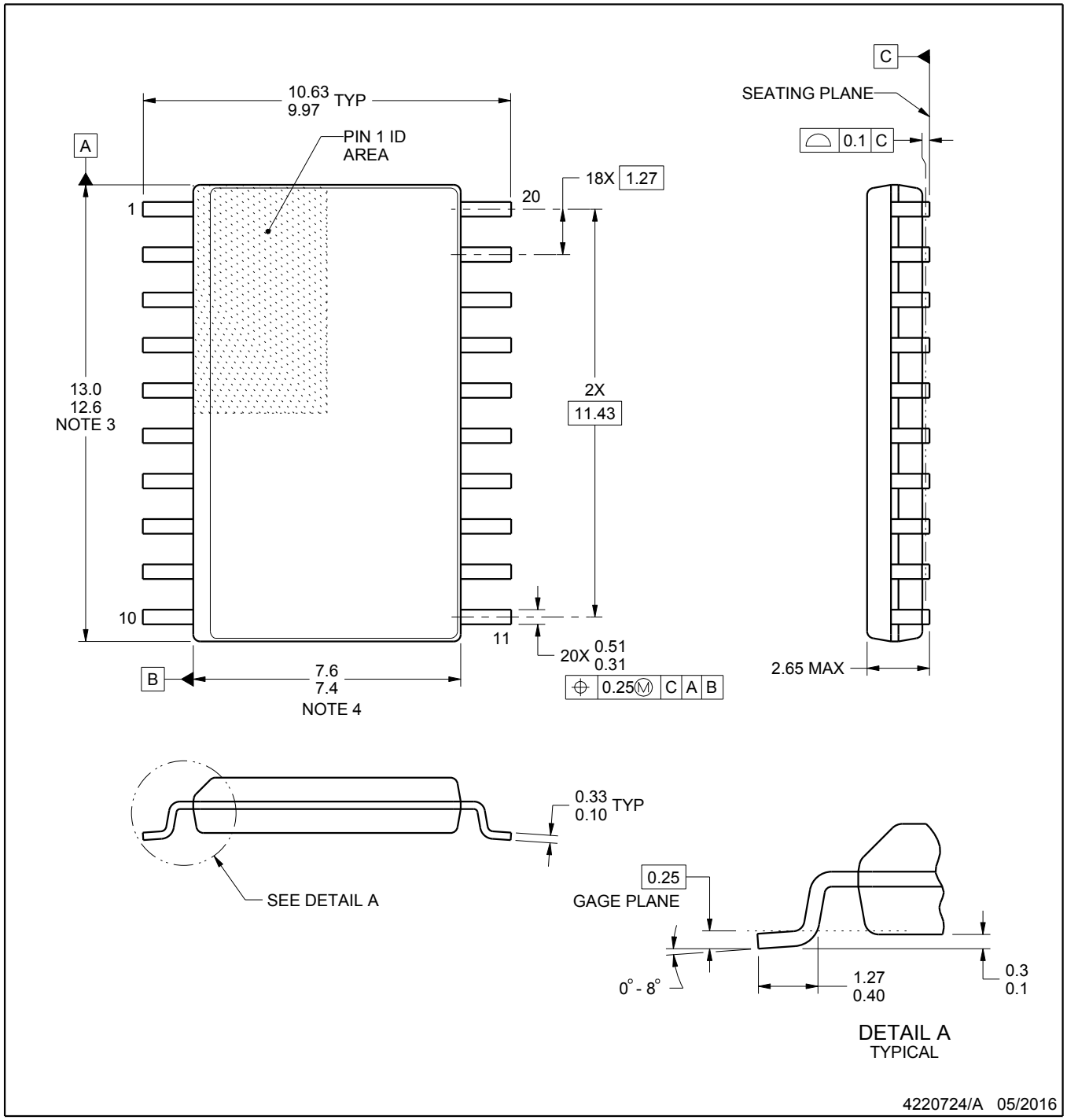


PACKAGE OUTLINE

DW0020A

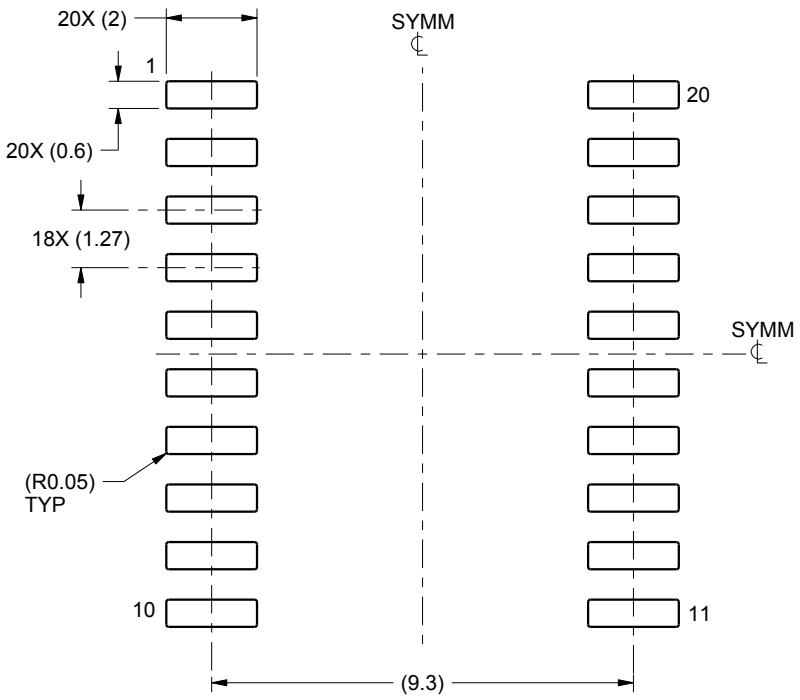
SOIC - 2.65 mm max height

SOIC

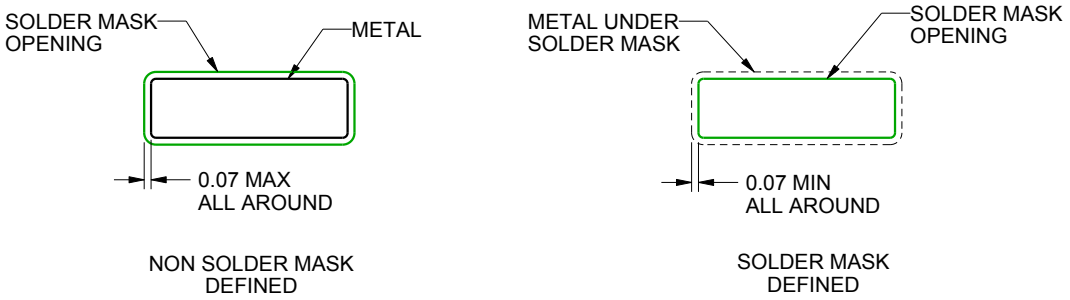


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

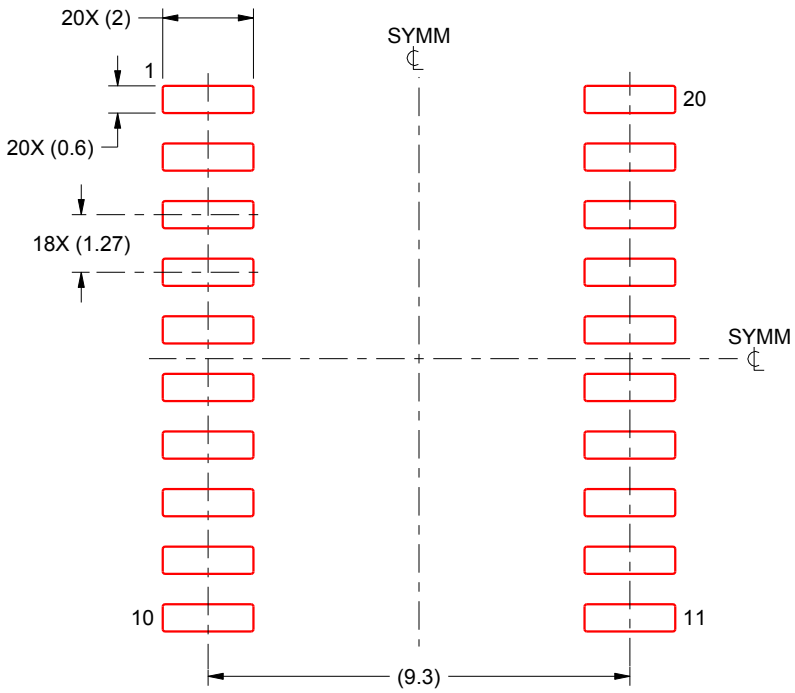


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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