









CD54HCT373, CD74HCT373 SCLS453E - FEBRUARY 2001 - REVISED JUNE 2022

# CDx4HCT373 Octal Transparent D-Type Latches With 3-State Outputs

#### 1 Features

- 4.5-V to 5.5-V V<sub>CC</sub> operation
- Wide operating temperature range of -55°C to 125°C
- Balanced propagation delays and transition times
- Standard outputs drive up to 10 LS-TTL loads
- Significant power reduction compared to LS-TTL Logic ICs
- Inputs are TTL-voltage compatible

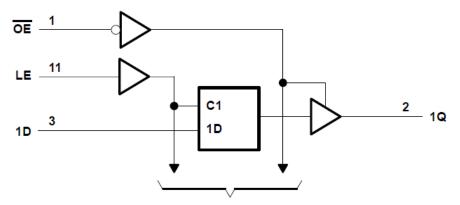
## 2 Description

The 'HCT373 devices are octal transparent D-type latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

#### **Device Information**

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
CD74HCT373M	SOIC (20)	12.80 mm × 7.50 mm
CD74HCT373E	PDIP (20)	25.40 mm × 6.35 mm
CD54HCT373F	CDIP (20)	26.92 mm × 6.92 mm

For all available packages, see the orderable addendum at the end of the data sheet.



To Seven Other Channels **Funtional Block Diagram** 



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## **3 Revision History**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision D (February 2022) to Revision E (June 2022)

Page

Junction-to-ambient thermal resistance values increased. DW was 69 is now 109.1, N was 58 is now 84.6.....

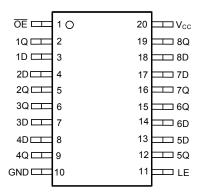
### Changes from Revision C (May 2003) to Revision D (February 2022)

Page

 Updated the numbering, formatting, tables, figures, and cross-references throughout the doucment to reflect modern data sheet standards......



## **4 Pin Configuration and Functions**



J, N, DW package 20-Pin CDIP, PDIP, SOIC Top View



## **5 Specifications**

## **5.1 Absolute Maximum Ratings**

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		-0.5	7	V
I <sub>IK</sub>	Input clamp current <sup>(2)</sup>	$V_I < 0$ or $V_I > V_{CC}$		± 20	mA
I <sub>OK</sub>	Output clamp current <sup>(2)</sup>	$V_O < 0$ or $V_O > V_{CC}$		± 20	mA
Io	Continuous output drain current per output	V <sub>O</sub> = 0 to V <sub>CC</sub>		± 35	mA
Io	Continuous output source or sink current per output	$V_O = 0$ to $V_{CC}$		± 25	mA
	Continuous current through V <sub>CC</sub> or GND			± 50	mA
TJ	Junction temperature			150	°C
T <sub>stg</sub>	Storage temperature range		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## **5.2 Recommended Operating Conditions**(1)

		T <sub>A</sub> = 25°	С	T <sub>A</sub> = -55°C	to 125°C	T <sub>A</sub> = -40°C 1	to 85°C	UNIT
		MIN	MAX	MIN MAX		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8		0.8	V
VI	Input voltage		V <sub>CC</sub>		V <sub>CC</sub>		V <sub>CC</sub>	V
Vo	Output voltage		V <sub>CC</sub>		V <sub>CC</sub>		V <sub>CC</sub>	V
Δt/Δν	Input transition rise or fall rate		500		500		500	ns

<sup>(1)</sup> All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

#### 5.3 Thermal Information

		DW (SOIC)	N (PDIP)	
THERMAL MI	ETRIC	20 PINS	20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(1)</sup>	109.1	84.6	°C/W
R <sub>0JC(top)</sub>	Junction-to-case (top) thermal resistance	76	72.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	77.6	65.3	°C/W
ΨЈТ	Junction-to-top characterization parameter	51.5	55.3	°C/W
ΨЈВ	Junction-to-board characterization parameter	77.1	65.2	°C/W
R <sub>0JC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

 For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application report.

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<sup>(2)</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

#### **5.4 Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CO	TEST CONDITIONS		T <sub>A</sub> = 25	s°C	T <sub>A</sub> = -55 125°		T <sub>A</sub> = -40°C	to 85°C	UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	$I_{OH} = -20 \mu A$		4.4		4.4		4.4		V
∨он	VI - VIH OI VIL	I <sub>OH</sub> = -6 mA	4.5 V	3.98		3.7		3.84		v
V	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	4.5 V		0.1		0.1		0.1	V
V <sub>OL</sub>	VI - VIH OI VIL	$v_1 = v_{1H}$ or $v_{1L}$ $I_{OL} = 6 \text{ mA}$			0.26		0.4		0.33	v
I <sub>1</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0		5.5 V		±0.1		±1		±1	μA
l <sub>OZ</sub>	$V_O = V_{CC}$ or 0		5.5 V		±0.5		±10		±5	μA
Icc	$V_I = V_{CC}$ or 0, I	<sub>O</sub> = 0	5.5 V		8		160		80	μA
	OE input held a	it V <sub>CC</sub> - 2.1 V	4.5 V to 5.5 V		540		735		675	μA
ΔI <sub>CC</sub> <sup>(1)</sup>	Any D input held at V <sub>CC</sub> – 2.1 V		4.5 V to 5.5 V		144		196		180	μА
	LE input held at V <sub>CC</sub> – 2.1 V		4.5 V to 5.5 V		360		490		450	μA
C <sub>i</sub>					10		10		10	pF
Co					10		10		10	pF

<sup>(1)</sup> Additional quiescent supply current per input pin, TTL inputs high, 1 unit load. For dual-supply systems, theoretical worst-case (V<sub>I</sub> = 2.4 V, V<sub>CC</sub> = 5.5 V) specification is 1.8 mA.

## 5.5 Timing Requirements

over recommended operating free-air temperature range,  $V_{CC} = 4.5 \text{ V}$  (unless otherwise noted) (see Figure 6-1)

		T <sub>A</sub> = 25°	С	T <sub>A</sub> = -55°C to	125°C	T <sub>A</sub> = -40°C	to 85°C	UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	ONII
t <sub>w</sub>	Pulse duration, LE high	16		24		20		ns
t <sub>su</sub>	Setup time, data before LE ↓	13		20		16		ns
t <sub>h</sub>	Hold time, data after LE ↓	10		15		13		ns

## 5.6 Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC}$  = 4.5 V (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 2	25°C	T <sub>A</sub> = -55°C to 125°C		T <sub>A</sub> = -40°C to	85°C	UNIT
	(INFOT)	(001701)	CAFACITANCE	MIN	MAX	MIN MA	λX	MIN	MAX	
4 .	D	Q	C <sub>L</sub> = 50 pF		32		48		40	ns
$t_{pd}$	LE	Q	CL = 30 pr		35		53		44	115
t <sub>en</sub>	ŌĒ	Q	C <sub>L</sub> = 50 pF		35		53		44	ns
t <sub>dis</sub>	ŌĒ	Q	C <sub>L</sub> = 50 pF		35		53		44	ns
t <sub>t</sub>		Q	C <sub>L</sub> = 50 pF		12		18		15	ns

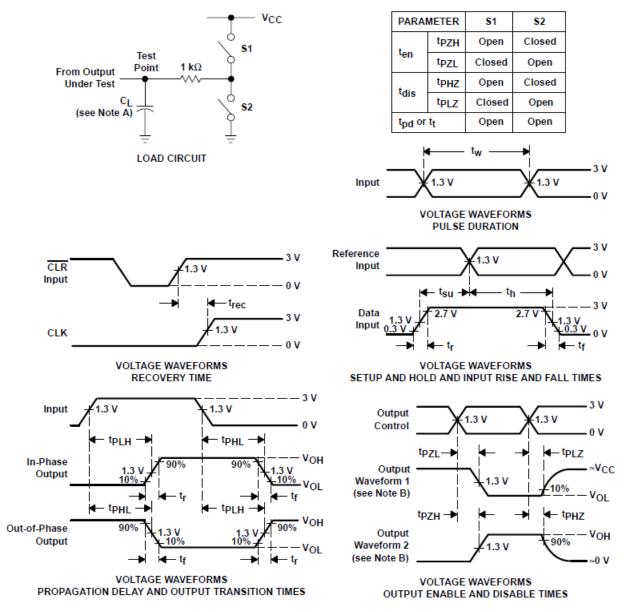
## 5.7 Operating Characteristics

 $V_{CC}$  = 5 V,  $T_A$  = 25°C

	PARAMETER	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	53	pF



#### **6 Parameter Measurement Information**



- A. C<sub>L</sub> includes probe and test-fixture capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
- D. For clock inputs,  $f_{\text{max}}$  is measured with the input duty cycle at 50%.
- E. The outputs are measured one at a time with one input transition per measurement.
- F.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- G.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- H.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 6-1. Load Circuit and Voltage Waveforms

## 7 Detailed Description

#### 7.1 Overview

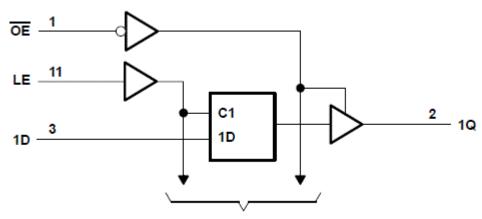
The 'HCT373 devices are octal transparent D-type latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable  $(\overline{OE})$  input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

 $\overline{\text{OE}}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  should be tied to VCC through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

#### 7.2 Functional Block Diagram



To Seven Other Channels

## 7.3 Device Functional Modes

Table 7-1. Function Table (each latch)

	INPUTS							
ŌĒ	LE	D	OUTPUT Q					
L	Н	Н	Н					
L	Н	L	L					
L	L	Х	Q <sub>0</sub>					
Н	Х	Х	Z					



## 8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

### 9 Layout

#### 9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

#### 10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 10.2 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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#### 10.3 Trademarks

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#### 10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 10.5 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
CD54HCT373F	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT373F
CD54HCT373F.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT373F
CD54HCT373F3A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8686701RA CD54HCT373F3A
CD54HCT373F3A.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8686701RA CD54HCT373F3A
CD74HCT373E	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT373E
CD74HCT373E.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT373E
CD74HCT373M	Obsolete	Production	SOIC (DW)   20	-	-	Call TI	Call TI	-55 to 125	HCT373M
CD74HCT373M96	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT373M
CD74HCT373M96.A	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT373M

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

## **PACKAGE OPTION ADDENDUM**

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#### OTHER QUALIFIED VERSIONS OF CD54HCT373, CD74HCT373:

Catalog : CD74HCT373

Military : CD54HCT373

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

• Military - QML certified for Military and Defense Applications

## **PACKAGE MATERIALS INFORMATION**

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### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HCT373M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

**PACKAGE MATERIALS INFORMATION** 

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#### \*All dimensions are nominal

	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
ı	CD74HCT373M96	SOIC	DW	20	2000	356.0	356.0	45.0	

## **PACKAGE MATERIALS INFORMATION**

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### **TUBE**



#### \*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HCT373E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT373E.A	N	PDIP	20	20	506	13.97	11230	4.32

#### 14 LEADS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SOIC



#### NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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