

# CD54HC299, CD74HC299, CD54HCT299

Data sheet acquired from Harris Semiconductor SCHS178C

January 1998 - Revised May 2003

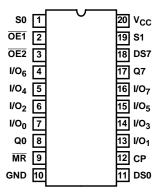
# High-Speed CMOS Logic 8-Bit Universal Shift Register; Three-State

#### Features

- Buffered Inputs
- Four Operating Modes: Shift Left, Shift Right, Load and Store
- Can be Cascaded for N-Bit Word Lengths
- I/O<sub>0</sub> I/O<sub>7</sub> Bus Drive Capability and Three-State for Bus Oriented Applications
- Typical  $f_{MAX} = 50MHz$  at  $V_{CC} = 5V$ ,  $C_L = 15pF$ ,  $T_A = 25^{o}C$
- Fanout (Over Temperature Range)
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL}$  = 30%,  $N_{IH}$  = 30% of  $V_{CC}$  at  $V_{CC}$  = 5V
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,
     V<sub>IL</sub>= 0.8V (Max), V<sub>IH</sub> = 2V (Min)
  - CMOS Input Compatibility,  $I_I \le 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

#### **Pinout**

CD54HC299, CD54HCT299 (CERDIP) CD74HC299, CD74HCT299 (PDIP, SOIC) TOP VIEW



#### Description

The 'HC259 and 'HCT299 are 8-bit shift/storage registers with three-state bus interface capability. The register has four synchronous-operating modes controlled by the two select inputs as shown in the mode select (S0, S1) table. The mode select, the serial data (DS0, DS7) and the parallel data (I/O $_0$  - I/O $_7$ ) respond only to the low-to-high transition of the clock (CP) pulse. S0, S1 and data inputs must be stable one setup time prior to the clock positive transition.

The Master Reset  $(\overline{MR})$  is an asynchronous active low input. When  $\overline{MR}$  output is low, the register is cleared regardless of the status of all other inputs. The register can be expanded by cascading same units by tying the serial output (Q0) to the serial data (DS7) input of the preceding register, and tying the serial output (Q7) to the serial data (DS0) input of the following register. Recirculating the (n x 8) bits is accomplished by tying the Q7 of the last stage to the DS0 of the first stage.

The three-state input/output I(/O) port has three modes of operation:

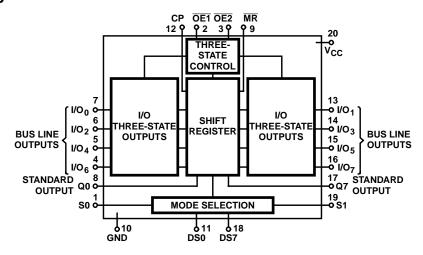
- Both output enable (OE1 and OE2) inputs are low and S0 or S1 or both are low, the data in the register is presented at the eight outputs.
- 2. When both S0 and S1 are high, I/O terminals are in the high impedance state but being input ports, ready for parallel data to be loaded into eight registers with one clock transition regardless of the status of OE1 and OE2.
- Either one of the two output enable inputs being high will force I/O terminals to be in the off-state. It is noted that each I/O terminal is a three-state output and a CMOS buffer input.

## Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC299F3A	-55 to 125	20 Ld CERDIP
CD54HCT299F3A	-55 to 125	20 Ld CERDIP
CD74HC299E	-55 to 125	20 Ld PDIP
CD74HC299M	-55 to 125	20 Ld SOIC
CD74HC299M96	-55 to 125	20 Ld SOIC
CD74HCT299E	-55 to 125	20 Ld PDIP
CD74HCT299M	-55 to 125	20 Ld SOIC
CD74HCT299M96	-55 to 125	20 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel.

## Functional Diagram



#### MODE SELECT FUNCTION TABLE THREE-STATE I/O PORT OPERATING MODE

			INPUTS			INPUTS/OUTPUTS
FUNCTION	OE1	OE2	S0	S1	Qn (REGISTER)	I/O0 I/O7
Read Register	L	L	L	Х	L	L
	L	L	L	Х	Н	Н
	L	L	Х	L	L	L
	L	L	Х	L	Н	Н
Load Register	Х	Х	Н	Н	Qn = I/On	I/On = Inputs
Disable I/O	Н	Х	Х	Х	Х	(Z)
	Х	Н	Х	Х	Х	(Z)

#### **TRUTH TABLE**

				INPUTS					REGIS	TER OU	TPUTS	
FUNCTION	MR	СР	S0	S1	DS0	DS7	I/On	Q0	Q1		Q6	Q7
RESET (CLEAR)	L	Х	Х	х	Х	Х	Х	L	L		L	L
Shift Right	Н	1	h	I	I	Х	Х	L	q <sub>0</sub>		q <sub>5</sub>	q <sub>6</sub>
	Н	1	h	I	h	Х	Х	Н	90		q <sub>5</sub>	Q6
Shift Left	Н	1	I	h	Х	I	Х	91	q2		97	L
	Н	1	I	h	Х	h	Х	91	q <sub>2</sub>		97	Н
Hold (Do Nothing)	Н	1	I	I	Х	Х	Х	q <sub>0</sub>	<b>9</b> 1		q <sub>6</sub>	97
Parallel Load	Н	1	h	h	Х	Х	Ī	L	L		L	L
	Н	1	h	h	Х	Х	h	Н	Н		Н	Н

H = Input Voltage High Level, h = Input voltage high one set-up timer prior clock transition; L = Input Voltage Low Level; I = Input voltage low one set-up time prior to clock transition; qn = Lower case letter indicates the state of the reference output one set-up time prior to clock transition; X - Voltage level on logic status don't care; Z = Output in high impedance state, ↑ = Low to High Clock Transition.

### **Absolute Maximum Ratings** DC Supply Voltage, V $_{CC}$ .....-0.5V to 7V DC Input Diode Current, I<sub>IK</sub> For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ ..... $\pm 20$ mA DC Output Diode Current, $I_{OK}$ DC Drain Current, per Output, $I_{O}$ , For -0.5V < $V_{O}$ < $V_{CC}$ + 0.5V For I/O Outputs......±35mA DC Output Source or Sink Current per Output Pin, $I_{\mbox{\scriptsize O}}$ **Operating Conditions**

#### **Thermal Information**

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ (°C/W)
E (PDIP) Package	69
M (SOIC) Package	58
Maximum Junction Temperature	150 <sup>0</sup> C
Maximum Storage Temperature Range	65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C
(SOIC - Lead Tips Only)	

Temperature Range, T <sub>A</sub>	55°C to 125°C
HC Types	2V to 6V
HCT Types	
DC Input or Output Voltage, V <sub>I</sub> , V <sub>O</sub>	0V to V <sub>CC</sub>
Input Rise and Fall Time	
2V	1000ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

1. The package thermal impedance is calculated in accordance with JESD 51-7.

#### **DC Electrical Specifications**

		· -	EST DITION	s	v <sub>cc</sub>		25°C		-40°C 1	O 85°C	-55°C T	O 125 <sup>0</sup> C	
PARAMETER	SYMBOL	V <sub>I</sub> (V)	l <sub>o</sub> (	mA)	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES													
High Level Input	V <sub>IH</sub>	-		-	2	1.5	-	-	1.5	-	1.5	-	V
Voltage					4.5	3.15	-	-	3.15	-	3.15	-	V
					6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input	V <sub>IL</sub>	-		-	2	-	-	0.5	-	0.5	-	0.5	V
Voltage					4.5	-	-	1.35	-	1.35	-	1.35	V
					6	-	-	1.8	-	1.8	-	1.8	V
High Level Output	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0	.02	2	1.9	-	-	1.9	-	1.9	-	V
Voltage CMOS Loads					4.5	4.4	-	-	4.4	-	4.4	-	V
OWOC Loads					6	5.9	-	-	5.9	-	5.9	-	V
High Level Output			Qn	I/On	-	-	-	-	-	-	-	-	V
Voltage TTL Loads			-4	-6	4.5	3.98	-	-	3.84	-	3.7	-	V
112 2000			-5.2	-7.8	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.	02	2	-	-	0.1	-	0.1	-	0.1	V
Voltage CMOS Loads					4.5	-	-	0.1	-	0.1	-	0.1	V
ower Loads					6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output			Qn	I/On	-	-	-	-	-	-	-	-	V
Voltage TTL Loads			4	6	4.5	-	-	0.26	-	0.33	-	0.4	V
1122000			5.2	7.8	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	Ι <sub>Ι</sub>	V <sub>CC</sub> or GND		-	6	-	-	±0.1	-	±1	-	±1	μА

## DC Electrical Specifications (Continued)

		1	EST DITIONS	V <sub>CC</sub>		25°C		-40°C T	TO 85°C	-55°C T		
PARAMETER	SYMBOL	V <sub>I</sub> (V)	I <sub>O</sub> (mA)	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
Quiescent Device Current	Icc	V <sub>CC</sub> or GND	0	6	-	-	8	-	80	-	160	μΑ
Three- State Leak- age Current	V <sub>IL</sub> or V <sub>IH</sub>	V <sub>O</sub> =V <sub>CC</sub> or GND	-	6	-	-	±0.5	-	±5	-	±10	μА
HCT TYPES	•					•		•				
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V <sub>ОН</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	lı	V <sub>CC</sub> and GND	0	5.5	-		±0.1	-	±1	-	±1	μА
Quiescent Device Current	Icc	V <sub>CC</sub> or GND	0	5.5	-	-	8	-	80	-	160	μА
Three- State Leak- age Current	V <sub>IL</sub> or V <sub>IH</sub>	V <sub>O</sub> =V <sub>CC</sub> or GND	-	6	-	-	±0.5	-	±5	-	±10	μА
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI <sub>CC</sub> (Note 2)	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μΑ

#### NOTE:

## **HCT Input Loading Table**

INPUT	UNIT LOADS
S1, MR	0.25
I/O <sub>0</sub> - I/O <sub>7</sub>	0.25
DS0, DS7	0.25
S0, CP	0.6
OE1, OE2	0.3

NOTE: Unit Load is  $\Delta I_{\hbox{CC}}$  limit specific in Static Specifications Table, e.g., 360 $\mu A$  max. at  $25^{o}C.$ 

<sup>2.</sup> For dual-supply systems theoretical worst case ( $V_I$  = 2.4V,  $V_{CC}$  = 5.5V) specification is 1.8mA.

## **Prerequisite for Switching Specifications**

				25°C		-40	°C TO 8	5°C	-55°C TO 125°C			
PARAMETER	SYMBOL	V <sub>CC</sub> (V)	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
HC TYPES		!									<u> </u>	
Maximum Clock	f <sub>MAX</sub>	2	6	-	-	5	-	-	4	-	-	MHz
Frequency		4.5	30	-	-	25	-	-	20	-	-	MHz
		6	35	-	-	29	-	-	23	-	-	MHz
MR Pulse Width	t <sub>W</sub>	2	50	-	-	65	-	-	75	-	-	ns
		4.5	10	-	-	13	-	-	15	-	-	ns
		6	9	-	-	11	-	-	13	-	-	ns
Clock Pulse Width	t <sub>W</sub>	2	80	-	-	100	-	-	120	-	-	ns
		4.5	16	-	-	20	-	-	24	-	-	ns
		6	14	-	-	17	-	-	20	-	-	ns
Setup Time	t <sub>SU</sub>	2	100	-	-	125	-	-	150	-	-	ns
DS0, DS7, I/On to Clock		4.5	20	-	-	25	-	-	30	-	-	ns
		6	17	-	-	21	-	-	26	-	-	ns
Hold Time DS0, DS7,		2	0	-	-	0	-	-	0	-	-	ns
I/On, S0, S1 to Clock		4.5	0	-	-	0	-	-	0	-	-	ns
		6	0	-	-	0	-	-	0	-	-	ns
Recovery Time	t <sub>REC</sub>	2	5	-	-	5	-	-	5	-	-	ns
MR to Clock		4.5	5	-	-	5	-	-	5	-	-	ns
		6	5	-	-	5	-	-	5	-	-	ns
Setup Time	t <sub>SU</sub>	2	120	-	-	150	-	-	180	-	-	ns
S1, S0 to Clock		4.5	24	-	-	30	-	-	36	-	-	ns
		6	20	-	-	26	-	-	31	-	-	ns
HCT TYPES												
Maximum Clock Frequency	f <sub>MAX</sub>	4.5	25	-	-	20	-	-	16	-	-	MHz
MR Pulse Width	t <sub>W</sub>	4.5	15	-	-	19	-	-	22	-	-	ns
Clock Pulse Width	t <sub>W</sub>	4.5	20	-	-	25	-	-	30	-	-	ns
Setup Time DS0, DS7, I/On, S0, S1 to Clock	t <sub>SU</sub>	4.5	20	-	-	25	-	-	30	-	-	ns
Hold Time DS0, DS7, I/On, S0, S1 to Clock	t <sub>H</sub>	4.5	0	-	-	0	-	-	0	-	-	ns
Recovery Time MR to Clock	tREC	4.5	5	-	-	5	-	-	5	-	-	ns
Setup Time S1, S0 to Clock	t <sub>SU</sub>	4.5	27	-	-	34	-	-	41	-	-	ns

## **Switching Specifications** $C_L = 50pF$ , Input $t_f$ , $t_f = 6ns$

		TEST			25°C			C TO °C	-55°C TO 125°C		- - - -
PARAMETER	SYMBOL	CONDITIONS	V <sub>CC</sub> (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES										-	
Propagation Delay	t <sub>PLH</sub> , t <sub>PHL</sub>	$C_L = 50pF$									
Clock to I/O Output, Clock to Q0 and Q7,			2	-	-	200	-	250	-	300	ns
MR to Output			4.5	-	-	40	-	50	-	60	ns
		C <sub>L</sub> = 15pF	5	-	17	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	34	-	43	-	51	ns
Output Enable and Disable Times	<sup>t</sup> PZL	C <sub>L</sub> = 15pF	5	-	10	-	-	-	-	-	ns
Times	t <sub>PZH</sub> , t <sub>PLZ</sub>			ı	13	-	1	-	-	-	ns
	t <sub>PHZ</sub>			-	15	-	-	-	-	-	ns
Output High-Z to High Level	t <sub>PZH</sub>	C <sub>L</sub> = 50pF	2	-	-	155	-	195	-	235	ns
			4.5	-	-	31	-	39	-	47	ns
			6	-	-	26	-	33	-	40	ns
Output High Level to High-Z	t <sub>PHZ</sub>	C <sub>L</sub> = 50pF	2	-	-	185	-	230	-	280	ns
			4.5	-	-	37	-	46	-	56	ns
			6	-	-	31	-	39	-	48	ns
Output Low Level to High-Z	t <sub>PLZ</sub>	C <sub>L</sub> = 50pF	2	-	-	155	-	195	-	235	ns
			4.5	-	-	31	-	39	-	47	ns
			6	-	-	26	-	33	-	40	ns
Output High-Z to Low Level	t <sub>PZL</sub>	C <sub>L</sub> = 50pF	2	-	-	130	-	165	-	195	ns
			4.5	-	-	26	-	33	-	39	ns
			6	-	-	22	-	28	-	33	ns
Output Transition Time	t <sub>THL</sub> , t <sub>TLH</sub>	C <sub>L</sub> = 50pF									
Q0, Q7			2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
I/O <sub>0</sub> to I/O <sub>7</sub>	t <sub>THL</sub> , t <sub>TLH</sub>	C <sub>L</sub> = 50pF	2	-	-	60	-	75	-	90	ns
			4.5	-	-	12	-	15	-	18	ns
			6	-	-	10	-	13	-	15	ns
Input Capacitance	C <sub>I</sub>	C <sub>L</sub> = 50pF	-	10	-	10	-	10	-	10	pF
Three-State Output Capacitance	CO	-	-	20	-	20	-	20	-	20	pF
Power Dissipation Capacitance (Notes 3, 4)	C <sub>PD</sub>	C <sub>L</sub> = 15pF	5	-	150	-	-	-	-	-	pF

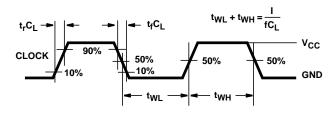
#### Switching Specifications $C_L = 50pF$ , Input $t_r$ , $t_f = 6ns$ (Continued)

		TEST			25°C			С ТО °С		C TO 5°C	
PARAMETER	SYMBOL	CONDITIONS	V <sub>CC</sub> (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HCT TYPES											
Propagation Delay	t <sub>PHL</sub> , t <sub>PLH</sub>										
Clock to I/O Output, Clock to Q0 and Q7		$C_L = 50pF$	4.5	-	-	45	-	56	-	68	ns
Clock to Qu and Q1		C <sub>L</sub> = 15pF	5	-	19	-	-	-	-	-	ns
MR to Output	t <sub>PHL</sub> , t <sub>PLH</sub>	C <sub>L</sub> = 50pF	4.5	-	-	46	-	58	-	69	ns
Output Enable and Disable Times	t <sub>PZL</sub> , t <sub>PZH</sub> , t <sub>PLZ</sub> , t <sub>PHZ</sub>	C <sub>L</sub> = 15pF	5	-	10, 13, 15	-	-	-	-	-	ns
Output High-Z to High Level	t <sub>PZH</sub>	C <sub>L</sub> = 50pF	4.5	-	-	32	-	40	-	48	ns
Output High Level to High-Z	t <sub>PHZ</sub>	C <sub>L</sub> = 50pF	4.5	-	-	37	-	46	-	56	ns
Output Low Level to High-Z	t <sub>PLZ</sub>	C <sub>L</sub> = 50pF	4.5	-	-	32	-	40	-	48	ns
Output High-Z to Low Level	t <sub>PZL</sub>	C <sub>L</sub> = 50pF	4.5	-	-	30	-	38	-	45	ns
Output Transition Time Q0, Q7	t <sub>TLH</sub> , t <sub>THL</sub>	C <sub>L</sub> = 50pF	4.5	-	-	15	-	19	-	22	ns
I/O <sub>0</sub> to I/O <sub>7</sub>		C <sub>L</sub> = 50pF	4.5	-	-	12	-	15	-	18	ns
Input Capacitance	C <sub>IN</sub>	C <sub>L</sub> = 50pF	-	10	-	10	-	10	-	10	pF
Three-State Output Capacitance	CO	-	-	20	-	20	-	20	-	20	pF
Power Dissipation Capacitance (Notes 3, 4)	C <sub>PD</sub>	C <sub>L</sub> = 15pF	5	ī	170	í	-	-	-	-	pF

#### NOTES:

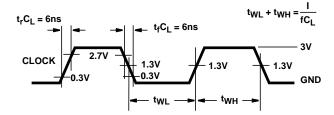
- 3.  $C_{\mbox{\scriptsize PD}}$  is used to determine the dynamic power consumption, per register.
- 4.  $P_D = C_{PD} \, V_{CC}^2 \, f_i + \sum (C_L \, V_{CC}^2 \, f_O)$  where  $f_i$  = Input Frequency,  $f_O$  = Output Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

#### Test Circuits and Waveforms



NOTE: Outputs should be switching from 10% V $_{CC}$  to 90% V $_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

#### Test Circuits and Waveforms (Continued)

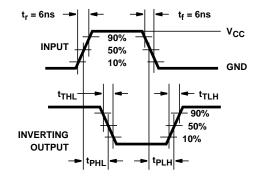


FIGURE 3. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

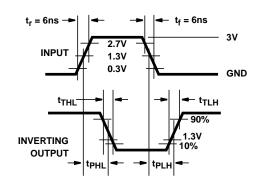


FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

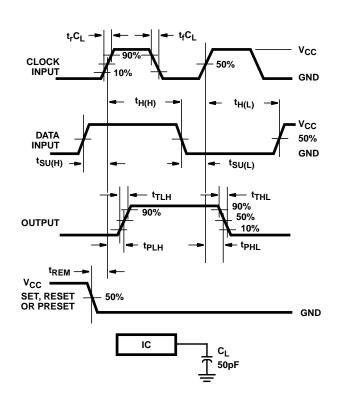


FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

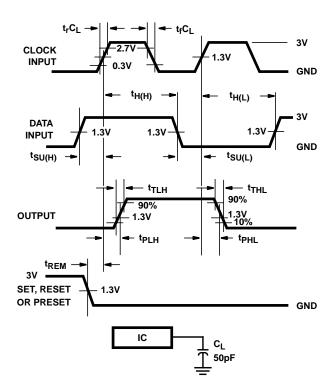


FIGURE 6. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

#### Test Circuits and Waveforms (Continued) 6ns V<sub>CC</sub> OUTPUT OUTPUT 90% DISABLE 50% DISABLE 10% 0.3 GND t<sub>PZL</sub> → - t<sub>PLZ</sub> → t<sub>PZL</sub> ► t<sub>PLZ</sub> → **OUTPUT LOW** OUTPUT LOW 50% TO OFF TO OFF 1.3V 10% 10% ◆ t<sub>PHZ</sub> ◆ - t<sub>PZH</sub> · t<sub>PHZ</sub> → tpzh -90% 90% **OUTPUT HIGH OUTPUT HIGH** 50% TO OFF TO OFF 1.3V

**OUTPUTS** 

ENABLED

FIGURE 7. HC THREE-STATE PROPAGATION DELAY WAVEFORM

**OUTPUTS** 

DISABLED

**OUTPUTS** 

**ENABLED** 

FIGURE 8. HCT THREE-STATE PROPAGATION DELAY WAVEFORM

**OUTPUTS** 

**DISABLED** 

OUTPUTS

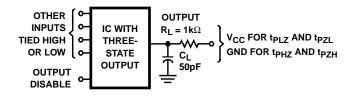
ENABLED

3V

GND

**OUTPUTS** 

**ENABLED** 



NOTE: Open drain waveforms  $t_{PLZ}$  and  $t_{PZL}$  are the same as those for three-state shown on the left. The test circuit is Output  $R_L = 1k\Omega$  to  $V_{CC}$ ,  $C_L = 50pF$ .

FIGURE 9. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT

www.ti.com

31-Oct-2025

#### **PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-8780601RA	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8780601RA CD54HC299F3A
5962-8943601MRA	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8943601MR A CD54HCT299F3A
CD54HC299F	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC299F
CD54HC299F.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC299F
CD54HC299F3A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8780601RA CD54HC299F3A
CD54HC299F3A.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8780601RA CD54HC299F3A
CD54HCT299F3A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8943601MR A CD54HCT299F3A
CD54HCT299F3A.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8943601MR A CD54HCT299F3A
CD74HC299E	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC299E
CD74HC299E.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC299E
CD74HC299M	Obsolete	Production	SOIC (DW)   20	-	-	Call TI	Call TI	-55 to 125	HC299M
CD74HC299M96	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC299M
CD74HC299M96.A	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC299M
CD74HC299M96E4	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC299M
CD74HCT299E	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT299E
CD74HCT299E.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT299E
CD74HCT299M	Obsolete	Production	SOIC (DW)   20	-	-	Call TI	Call TI	-55 to 125	HCT299M
CD74HCT299M96	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT299M
CD74HCT299M96.A	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT299M

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

### PACKAGE OPTION ADDENDUM

www.ti.com 31-Oct-2025

- (2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF CD54HC299, CD54HCT299, CD74HC299, CD74HCT299:

Catalog: CD74HC299, CD74HCT299

Military: CD54HC299, CD54HCT299

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

## **PACKAGE MATERIALS INFORMATION**

www.ti.com 24-Jul-2025

#### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC299M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HCT299M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

## **PACKAGE MATERIALS INFORMATION**

www.ti.com 24-Jul-2025



#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC299M96	SOIC	DW	20	2000	356.0	356.0	45.0
CD74HCT299M96	SOIC	DW	20	2000	356.0	356.0	45.0

## **PACKAGE MATERIALS INFORMATION**

www.ti.com 24-Jul-2025

#### **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC299E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HC299E.A	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT299E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT299E.A	N	PDIP	20	20	506	13.97	11230	4.32

#### 14 LEADS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SOIC



#### NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



#### IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025