# CD54HC175, CD74HC175, CD54HCT175, CD74HCT175

Data sheet acquired from Harris Semiconductor
SCHS160C

August 1997 - Revised October 2003

## High-Speed CMOS Logic Quad D-Type Flip-Flop with Reset

### Features

- **Common Clock and Asynchronous Reset on Four D-Type Flip-Flops**
- **Positive Edge Pulse Triggering**
- **Complementary Outputs**
- **Buffered Inputs**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55$^{O}$C to 125$^{O}$C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: $N_{IL}$ = 30%, $N_{IH}$ = 30% of $V_{CC}$ at $V_{CC}$ = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, $V_{IL}$= 0.8V (Max), $V_{IH}$ = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at $V_{OL}$, $V_{OH}$**

### Description

The ’HC175 and ’HCT175 are high speed Quad D-type Flip-Flops with individual D-inputs and Q, $\overline{Q}$ complementary outputs. The devices are fabricated using silicon gate CMOS technology. They have the low power consumption advantage of standard CMOS ICs and the ability to drive 10 LSTTL devices.

Information at the D input is transferred to the Q, $\overline{Q}$ outputs on the positive going edge of the clock pulse. All four Flip-Flops are controlled by a common clock (CP) and a common reset ($\overline{MR}$). Resetting is accomplished by a low voltage level independent of the clock. All four Q outputs are reset to a logic 0 and all four $\overline{Q}$ outputs to a logic 1.

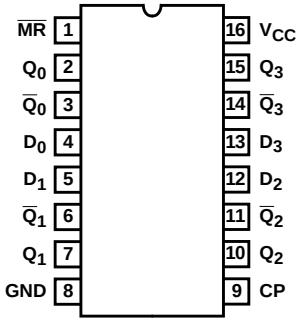
### Ordering Information

| PART NUMBER | TEMP. RANGE ($^{O}$C) | PACKAGE |
|---|---|---|
| CD54HC175F3A | -55 to 125 | 16 Ld CERDIP |
| CD54HCT175F3A | -55 to 125 | 16 Ld CERDIP |
| CD74HC175E | -55 to 125 | 16 Ld PDIP |
| CD74HC175M | -55 to 125 | 16 Ld SOIC |
| CD74HC175MT | -55 to 125 | 16 Ld SOIC |
| CD74HC175M96 | -55 to 125 | 16 Ld SOIC |
| CD74HCT175E | -55 to 125 | 16 Ld PDIP |
| CD74HCT175M | -55 to 125 | 16 Ld SOIC |
| CD74HCT175MT | -55 to 125 | 16 Ld SOIC |
| CD74HCT175M96 | -55 to 125 | 16 Ld SOIC |

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

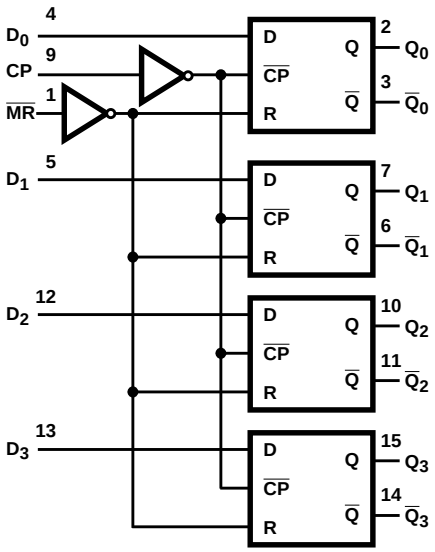
### Pinout

**CD54HC175, CD54HCT175**
**(CERDIP)**
**CD74HC175, CD74HCT175**
**(PDIP, SOIC)**
TOP VIEW




CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

## Functional Diagram

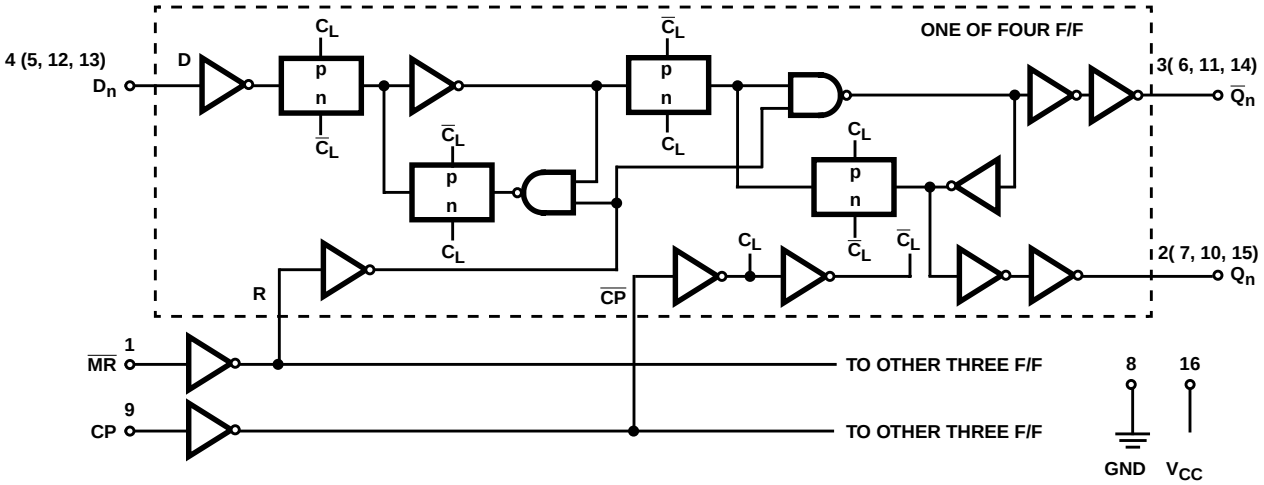



**TRUTH TABLE**

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| RESET ($\overline{MR}$) | CLOCK CP | DATA $D_n$ | $Q_n$ | $\overline{Q}_n$ |
| L | X | X | L | H |
| H | ↑ | H | H | L |
| H | ↑ | L | L | H |
| H | L | X | $Q_0$ | $\overline{Q}_0$ |

H = High Voltage Level, L = Low Voltage Level, X = Don't Care, ↑ = Transition from Low to High Level,
$Q_0$ = Level Before the Indicated Steady-State Input Conditions Were Established.

## Logic Diagram



## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ . . . . . -0.5V to 7V
DC Input Diode Current, $I_{IK}$
For $V_I$ < -0.5V or $V_I$ > $V_{CC}$ + 0.5V . . . . . ±20mA
DC Output Diode Current, $I_{OK}$
For $V_O$ < -0.5V or $V_O$ > $V_{CC}$ + 0.5V . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, $I_O$
For $V_O$ > -0.5V or $V_O$ < $V_{CC}$ + 0.5V . . . . . ±25mA
DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$ . . . . . ±50mA

## Operating Conditions

Temperature Range ($T_A$) . . . . . -55°C to 125°C
Supply Voltage Range, $V_{CC}$
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, $V_I$, $V_O$ . . . . . 0V to $V_{CC}$
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)

## Thermal Information

| Thermal Resistance (Typical, Note 1) | $\theta_{JA}$ (°C/W) |
|---|---|
| E (PDIP) Package | 67 |
| M (SOIC) Package | 73 |

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | $V_{CC}$ (V) | 25°C | | | -40°C TO +85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $I_O$ (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 2 | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | | | 4.5 | 3.15 | - | - | 3.15 | - | 3.15 | - | V |
| | | | | 6 | 4.2 | - | - | 4.2 | - | 4.2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 2 | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | | | 4.5 | - | - | 1.35 | - | 1.35 | - | 1.35 | V |
| | | | | 6 | - | - | 1.8 | - | 1.8 | - | 1.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 2 | 1.9 | - | - | 1.9 | - | 1.9 | - | V |
| | | | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| | | | -0.02 | 6 | 5.9 | - | - | 5.9 | - | 5.9 | - | V |
| High Level Output Voltage TTL Loads | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| | | | -5.2 | 6 | 5.48 | - | - | 5.34 | - | 5.2 | - | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 2 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 6 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| | | | 5.2 | 6 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ or GND | - | 6 | - | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 6 | - | - | 8 | - | 80 | - | 160 | µA |

## DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | | $V_{CC}$ (V) | 25°C | | | -40°C TO +85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $I_O$ (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HCT TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 4.5 to 5.5 | 2 | - | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 4.5 to 5.5 | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| High Level Output Voltage TTL Loads | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ to GND | 0 | 5.5 | - | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 5.5 | - | - | 8 | - | 80 | - | 160 | µA |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | $\Delta I_{CC}$ (Note 2) | $V_{CC}$ -2.1 | - | 4.5 to 5.5 | - | 100 | 360 | - | 450 | - | 490 | µA |

NOTES:

2. For dual-supply systems theoretical worst case ($V_I$ = 2.4V, $V_{CC}$ = 5.5V) specification is 1.8mA.

## HCT Input Loading Table

| INPUT | UNIT LOADS |
|---|---|
| $\overline{MR}$ | 1 |
| CP | 0.60 |
| D | 0.15 |

NOTE: Unit Load is $\Delta I_{CC}$ limit specified in DC Electrical Specifications table, e.g. 360µA max at 25°C.

## Prerequisite For Switching Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | | |
| Clock Pulse Width | $t_w$ | - | 2 | 80 | - | - | 100 | - | 120 | - | ns |
| | | | 4.5 | 16 | - | - | 20 | - | 24 | - | ns |
| | | | 6 | 14 | - | - | 17 | - | 20 | - | ns |
| $\overline{MR}$ Pulse Width | $t_w$ | - | 2 | 80 | - | - | 100 | - | 120 | - | ns |
| | | | 4.5 | 16 | - | - | 20 | - | 24 | - | ns |
| | | | 6 | 14 | - | - | 17 | - | 20 | - | ns |

## Prerequisite For Switching Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| Setup Time, Data to Clock | $t_{SU}$ | - | 2 | 80 | - | - | 100 | - | 120 | - | ns |
| | | | 4.5 | 16 | - | - | 20 | - | 24 | - | ns |
| | | | 6 | 14 | - | - | 17 | - | 20 | - | ns |
| Hold Time, Data to Clock | $t_H$ | - | 2 | 5 | - | - | 5 | - | 5 | - | ns |
| | | | 4.5 | 5 | - | - | 5 | - | 5 | - | ns |
| | | | 6 | 5 | - | - | 5 | - | 5 | - | ns |
| Removal Time, $\overline{MR}$ to Clock | $t_{REM}$ | - | 2 | 5 | - | - | 5 | - | 5 | - | ns |
| | | | 4.5 | 5 | - | - | 5 | - | 5 | - | ns |
| | | | 6 | 5 | - | - | 5 | - | 5 | - | ns |
| Clock Frequency | $f_{MAX}$ | - | 2 | 6 | - | - | 5 | - | 4 | - | MHz |
| | | | 4.5 | 30 | - | - | 25 | - | 20 | - | MHz |
| | | | 6 | 35 | - | - | 29 | - | 23 | - | MHz |
| **HCT TYPES** | | | | | | | | | | | |
| Clock Pulse Width | $t_W$ | - | 4.5 | 20 | - | - | 25 | - | 30 | - | ns |
| $\overline{MR}$ Pulse Width | $t_W$ | - | 4.5 | 20 | - | - | 25 | - | 30 | - | ns |
| Setup Time Data to Clock | $t_{SU}$ | - | 4.5 | 20 | - | - | 25 | - | 30 | - | ns |
| Hold Time Data to Clock | $t_H$ | - | 4.5 | 5 | - | - | 5 | - | 5 | - | ns |
| Removal Time $\overline{MR}$ to Clock | $t_{REM}$ | - | 4.5 | 5 | - | - | 5 | - | 5 | - | ns |
| Clock Frequency | $f_{MAX}$ | - | 4.5 | 25 | - | - | 20 | - | 16 | - | MHz |

## Switching Specifications Input $t_r$, $t_f$ = 6ns

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | -40°C TO 85°C | -55°C TO 125°C | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | | | TYP | MAX | MAX | MAX | |
| **HC TYPES** | | | | | | | | |
| Propagation Delay, Clock to Q or $\overline{Q}$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | 175 | 220 | 265 | ns |
| | | | 4.5 | - | 35 | 44 | 53 | ns |
| | | | 6 | - | 30 | 37 | 45 | ns |
| | | $C_L$ = 15pF | 5 | 14 | - | - | - | ns |
| Propagation Delay, $\overline{MR}$ to Q or $\overline{Q}$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | 175 | 220 | 265 | ns |
| | | | 4.5 | - | 35 | 44 | 53 | ns |
| | | | 6 | - | 30 | 37 | 45 | ns |
| | | $C_L$ = 15pF | 5 | 14 | - | - | - | ns |
| Output Transition Times | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 2 | - | 75 | 95 | 110 | ns |
| | | | 4.5 | - | 15 | 19 | 22 | ns |
| | | | 6 | - | 13 | 16 | 19 | ns |
| Input Capacitance | $C_{IN}$ | - | - | - | 10 | 10 | 10 | pF |
| Power Dissipation Capacitance (Notes 3, 4) | $C_{PD}$ | - | 5 | 65 | - | - | - | pF |

**Switching Specifications** Input $t_r$, $t_f$ = 6ns **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C TYP | 25°C MAX | -40°C TO 85°C MAX | -55°C TO 125°C MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **HCT TYPES** | | | | | | | | |
| Propagation Delay, Clock to Q or $\overline{Q}$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | 33 | 41 | 50 | ns |
| | | $C_L$ = 15pF | 5 | 13 | - | - | - | ns |
| Propagation Delay, $\overline{MR}$ to Q or $\overline{Q}$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | 35 | 44 | 53 | ns |
| | | $C_L$ = 15pF | 5 | 17 | - | - | - | ns |
| Output Transition Times | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 4.5 | - | 15 | 19 | 22 | ns |
| Input Capacitance | $C_{IN}$ | - | - | - | 10 | 10 | 10 | pF |
| Power Dissipation Capacitance (Notes 3, 4) | $C_{PD}$ | - | 5 | 67 | - | - | - | pF |

NOTES:

3. $C_{PD}$ is used to determine the dynamic power consumption, per flip-flop.
4. $P_D = V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 + f_O)$ where $f_i$ = Input Frequency, $f_O$ = Input Frequency, $C_L$ = Output Load Capacitance, $V_{CC}$ = Supply Voltage.

## Test Circuits and Waveforms

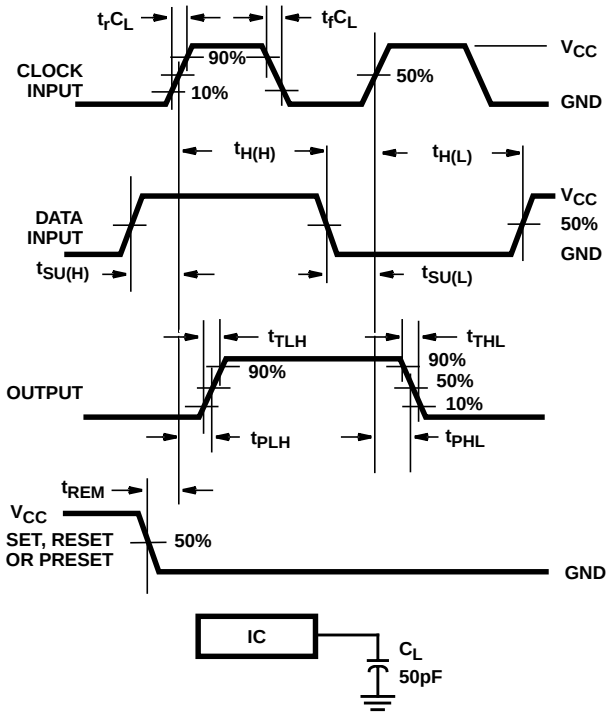



**FIGURE 1. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS**

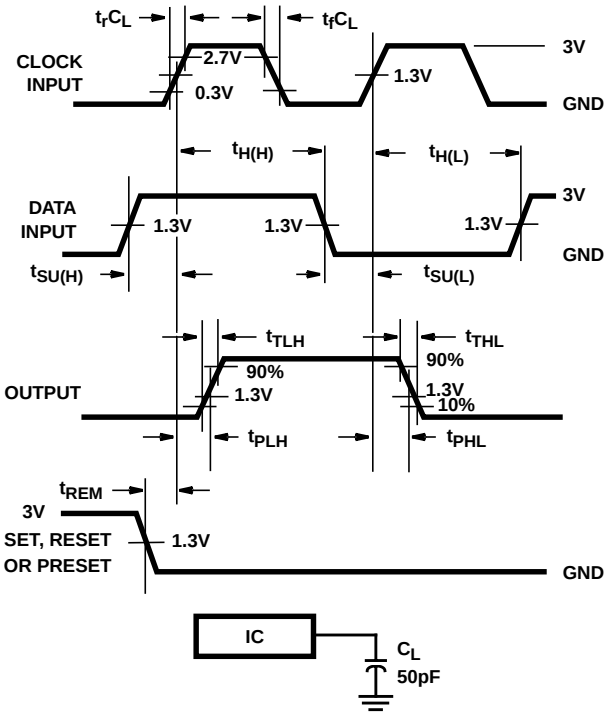



**FIGURE 2. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS**

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-8970101EA | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8970101EA CD54HCT175F3A |
| CD54HC175F3A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8408901EA CD54HC175F3A |
| CD54HC175F3A.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8408901EA CD54HC175F3A |
| CD54HCT175F3A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8970101EA CD54HCT175F3A |
| CD54HCT175F3A.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8970101EA CD54HCT175F3A |
| CD74HC175E | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HC175E |
| CD74HC175E.A | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HC175E |
| CD74HC175EE4 | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HC175E |
| CD74HC175M | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | -55 to 125 | HC175M |
| CD74HC175M96 | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC175M |
| CD74HC175M96.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC175M |
| CD74HCT175E | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HCT175E |
| CD74HCT175E.A | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HCT175E |
| CD74HCT175EE4 | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HCT175E |
| CD74HCT175M | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | -55 to 125 | HCT175M |
| CD74HCT175M96 | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT175M |
| CD74HCT175M96.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT175M |
| CD74HCT175M96G4 | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT175M |
| CD74HCT175MT | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | -55 to 125 | HCT175M |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.



**OTHER QUALIFIED VERSIONS OF CD54HC175, CD54HCT175, CD74HC175, CD74HCT175 :**

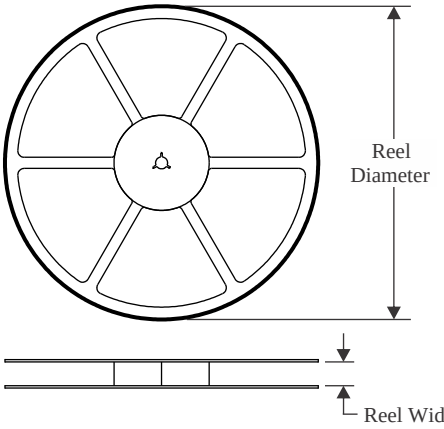
- Catalog : CD74HC175, CD74HCT175
- Military : CD54HC175, CD54HCT175

NOTE: Qualified Version Definitions:

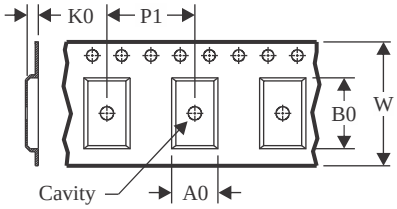
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

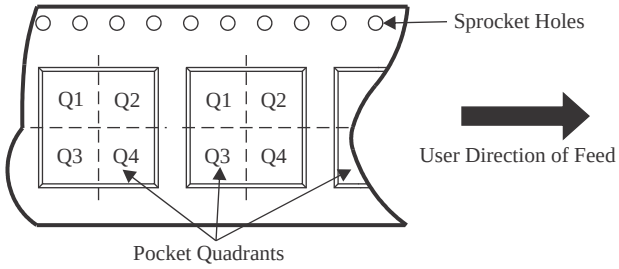



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

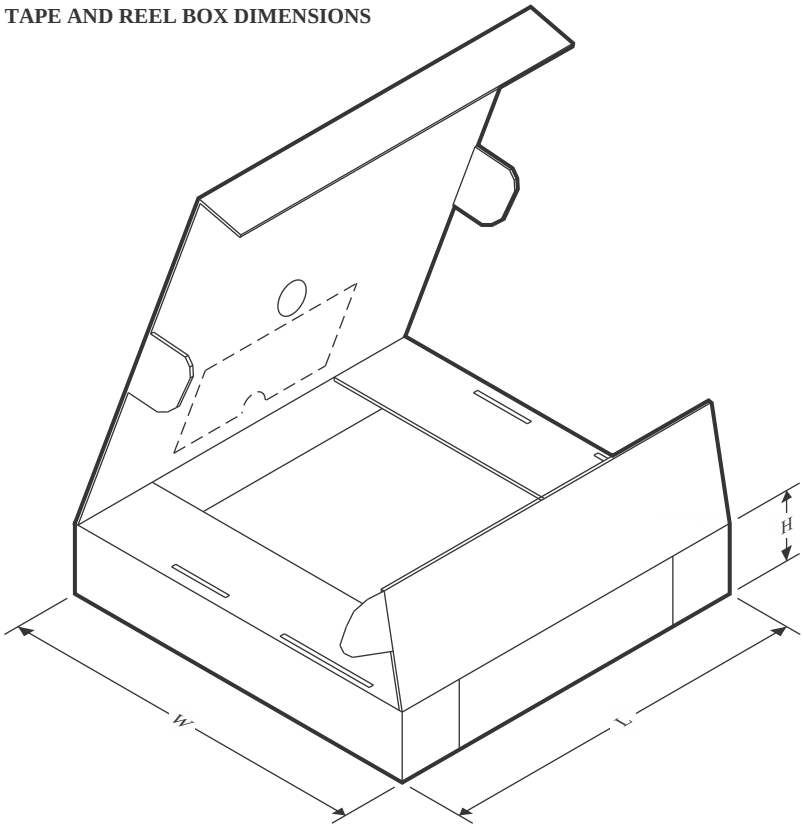
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74HC175M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HCT175M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

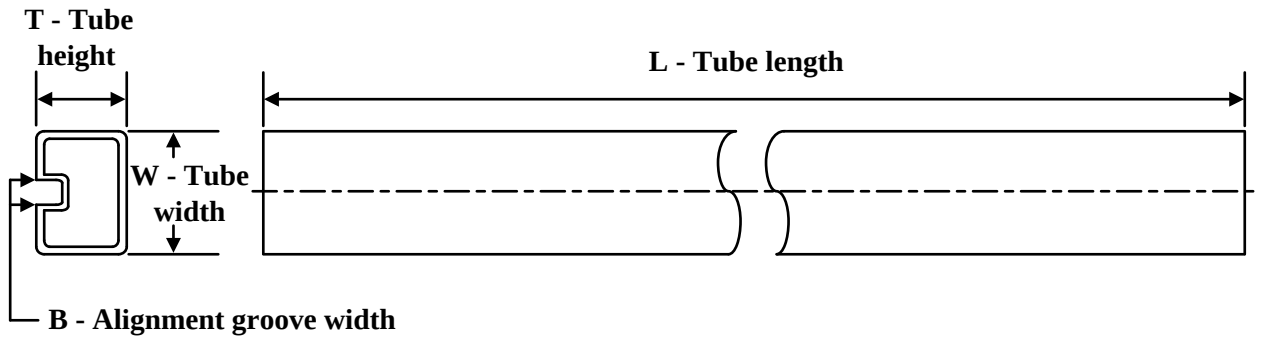
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD74HC175M96 | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| CD74HCT175M96 | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |

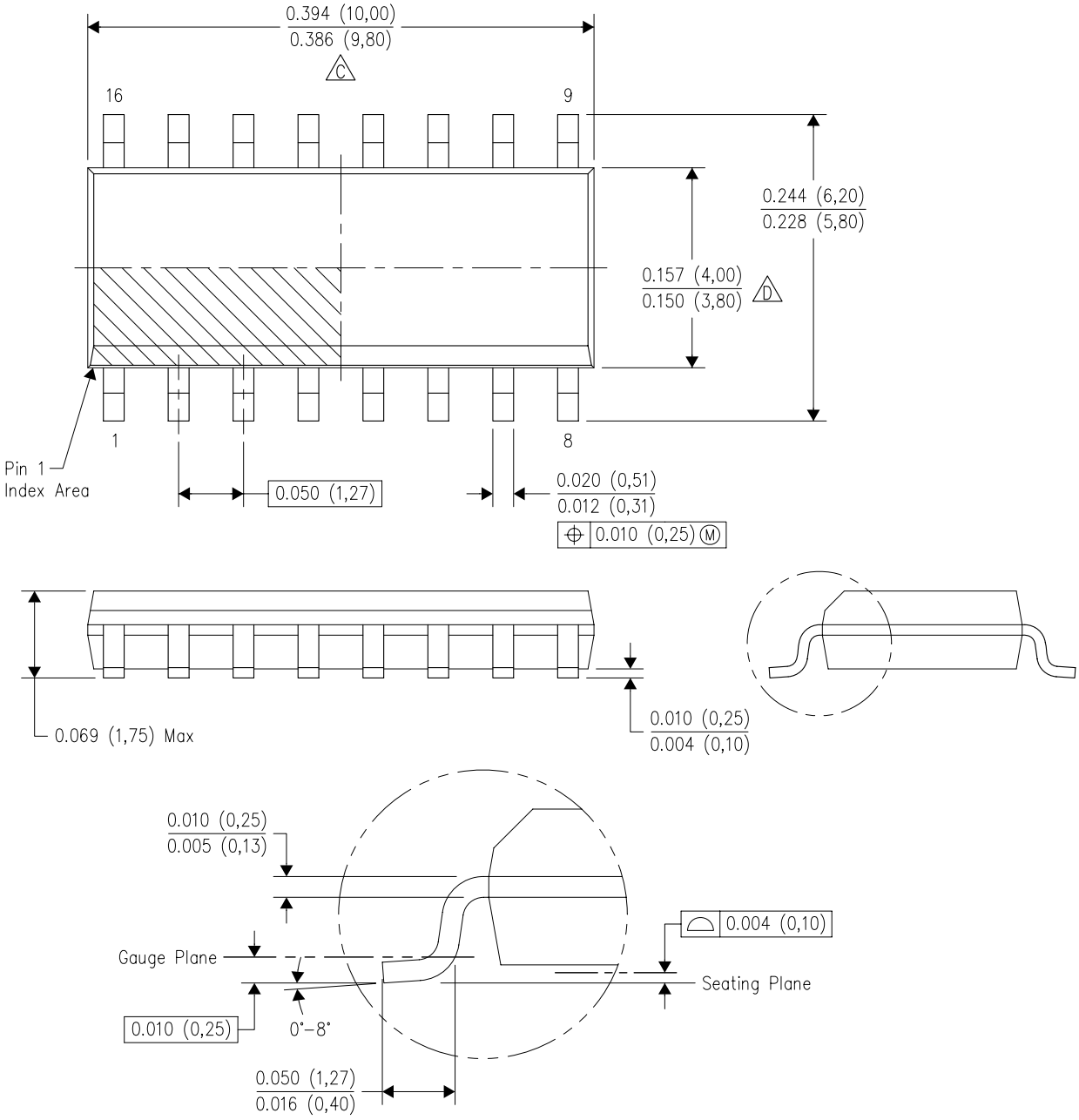
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| CD74HC175E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC175E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC175E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC175E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC175EE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC175EE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT175E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT175E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT175E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT175E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT175EE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT175EE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

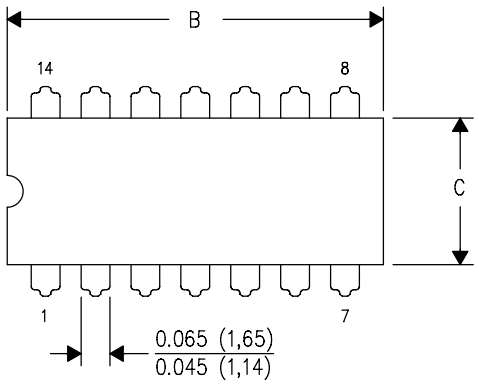



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

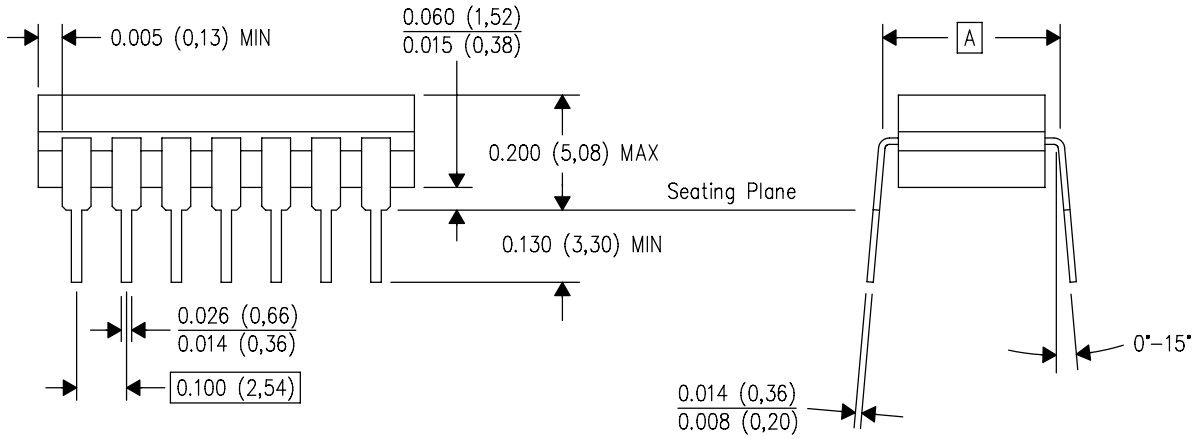
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



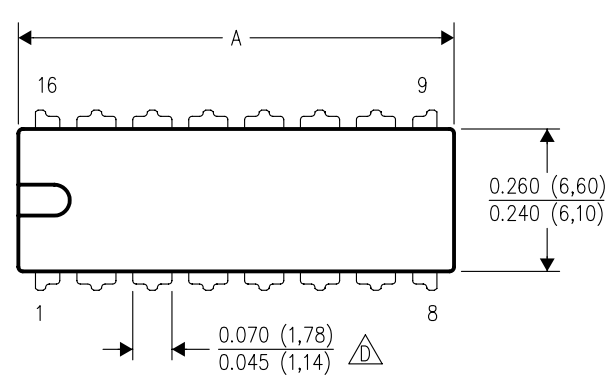

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

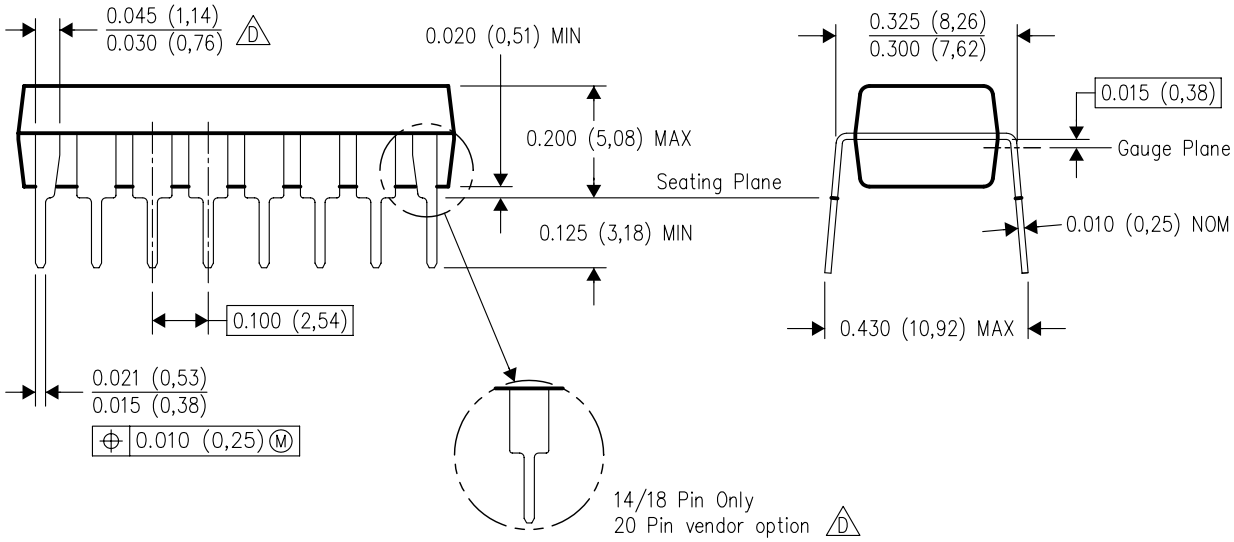
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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