CDx4HC164, CDx4HCT164 High-Speed CMOS Logic 8-Bit Serial-In, Parallel-Out Shift Register

1 Features

- Buffered inputs
- Asynchronous reset
- Typical f_{MAX} = 60MHz at V_{CC} = 5V, C_L = 15pF, T_A = 25°C
- Fanout (overtemperature range)
  - Standard Outputs: 10 LSTTL loads
  - Bus driver outputs: 15 LSTTL loads
- Wide operating temp range: – 55°C to 125°C
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL logic ICs
- HC types
  - 2V to 6V operation
  - High noise immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V
- HCT types
  - 4.5V to 5.5V operation
  - Direct LSTTL input logic compatibility, V_{IL} = 0.8V (Max), V_{IH} = 2V (Min)
  - CMOS input compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}

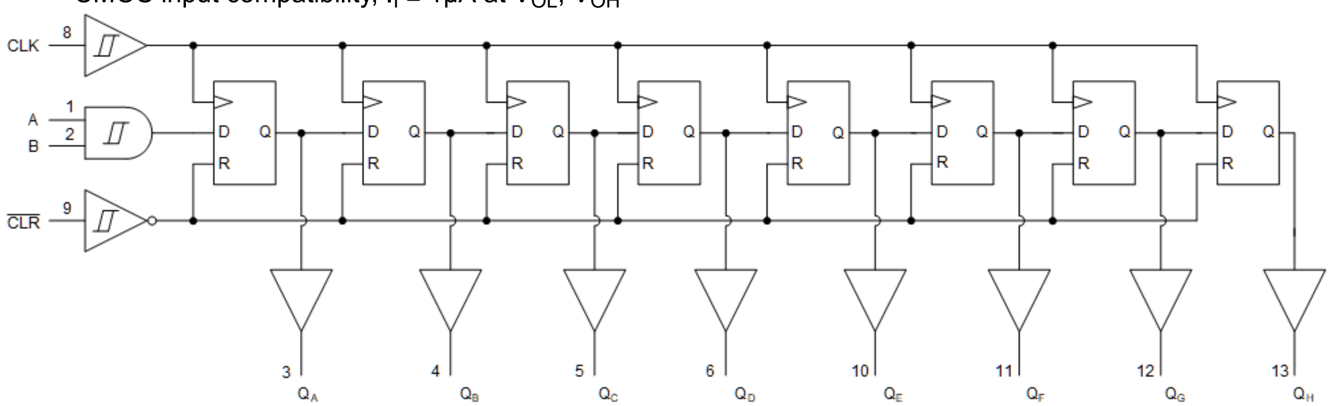
2 Description

The ’HC164 and ’HCT164 are 8-bit, serial-in, parallel-out, shift registers with asynchronous reset. Data is shifted on the positive edge of Clock (CLK). A LOW on the RESET ($\overline{CLR}$) pin resets the shift register and all outputs go to the LOW state regardless of the input conditions. Two Serial Data inputs (A and B) are provided, either one can be used as a data enable control.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
CD74HC164M	SOIC (14)	8.65mm × 3.90mm
CD74HCT164M	SOIC (14)	8.65mm × 3.90mm
CD74HC164E	PDIP (14)	19.31mm × 6.35mm
CD74HCT164E	PDIP (14)	19.31mm × 6.35mm
CD54HC164F	CDIP (14)	19.55mm × 6.71mm

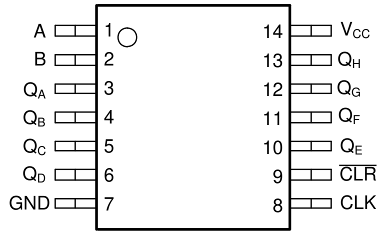
(1) For all available packages, see Section 11.



Functional Block Diagram

Table of Contents

3 Pin Configuration and Functions



J, D, and N Package
14-Pin CDIP, SOIC, and PDIP
Top View

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	7	V
I_{IK}	Input clamp current[(2)]	($V_I < 0$ or $V_I > V_{CC}$)		±20	mA
I_{OK}	Output clamp current[(2)]	($V_O < 0$ or $V_O > V_{CC}$)		±20	mA
I_O	Continuous output current	($V_O = 0$ to V_{CC})		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage range	HC types	2	6	V
		HCT types	4.5	5.5	
V_I, V_O	Input or output voltage		0	V_{CC}	V
	Input rise and fall time	2 V		1000	ns
		4.5 V		500	
		6 V		400	
T_A	Temperature range		–55	125	℃

4.3 Thermal Information

THERMAL METRIC[(1)]		D (SOIC)	N (PDIP)	UNIT
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86	80	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

4.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS(1)	V_{CC} (V)	25℃			–40℃ to 85℃		–55℃ to 125℃		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V_{IH}	High level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		
			6	4.2			4.2		4.2		
V_{IL}	Low level input voltage		2			0.5		0.5		0.5	V
			4.5			1.35		1.35		1.35	
			6			1.8		1.8		1.8	
V_{OH}	High level output voltage	I_{OH} = – 20 μA	2	1.9			1.9		1.9		V
		I_{OH} = – 20 μA	4.5	4.4			4.4		4.4		
		I_{OH} = – 20 μA	6	5.9			5.9		5.9		
	High level output voltage	I_{OH} = – 4 mA	4.5	3.98			3.84		3.7		
		I_{OH} = – 5.2 mA	6	5.48			5.34		5.2		
V_{OL}	Low level output voltage	I_{OL} = 20 μA	2			0.1		0.1		0.1	V
		I_{OL} = 20 μA	4.5			0.1		0.1		0.1	
		I_{OL} = 20 μA	6			0.1		0.1		0.1	
	Low level output voltage	I_{OL} = 4 mA	4.5			0.26		0.33		0.4	
		I_{OL} = 5.2 mA	6			0.26		0.33		0.4	V
I_I	Input leakage current		6			±0.1		±1		±1	μA
I_{CC}	Supply current	V_I = V_{CC} or GND	6			8		80		160	μA
HCT TYPES											
V_{IH}	High level input voltage		4.5 to 5.5	2			2		2		V
V_{IL}	Low level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	High level output voltage	I_{OH} = – 20 μA	4.5	4.4			4.4		4.4		V
	High level output voltage	I_{OH} = – 4 μA	4.5	3.98			3.84		3.7		
V_{OL}	Low level output voltage	I_{OL} = 20 μA	4.5			0.1		0.1		0.1	V
	Low level output voltage	I_{OL} = 4 μA	4.5			0.26		0.33		0.4	
I_I	Input leakage current	V_I = V_{CC} or GND	5.5			±0.1		±1		±1	μA
I_{CC}	Supply current	V_I = V_{CC} or GND	5.5			8		80		160	μA
ΔI_{CC} (2) (3)	Additional supply current per input pin	Date Shift-In (1,2)	4.5 to 5.5		100	108		135		147	μA
		$\overline{CLR}$	4.5 to 5.5		100	324		405		441	μA
		CLK	4.5 to 5.5		100	252		315		343	μA

(1) V_I = V_{IH} or V_{IL}, unless otherwise noted.
(2) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.
(3) Inputs held at V_{CC} – 2.1.

4.5 Prerequisite for Switching Characteristics

PARAMETER		V_{CC} (V)	25°C		– 40°C to 85°C		– 55°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
HC TYPES									
f_{MAX}	Maximum clock frequency	2	6		5		4		MHz
		4.5	30		24		20		MHz
		6	35		28		24		MHz
t_W	$\overline{CLR}$ pulse width	2	60		75		90		ns
		4.5	12		15		18		ns
		6	10		13		15		ns
t_w	CLK pulse width	2	80		100		120		ns
		4.5	16		20		24		ns
		6	14		17		20		ns
t_{SU}	Set-up time	2	60		75		90		ns
		4.5	12		15		18		ns
		6	10		13		15		ns
t_H	Hold time	2	4		4		4		ns
		4.5	4		4		4		ns
		6	4		4		4		ns
t_{REM}	$\overline{CLR}$ to clock, Removal time	2	80		100		120		ns
		4.5	16		20		24		ns
		6	14		17		20		ns
HCT TYPES									
f_{MAX}	Maximum clock frequency	4.5	27		22		18		MHz
t_W	$\overline{CLR}$ pulse width	6	18		23		27		ns
t_W	CLK pulse width	4.5	18		23		27		ns
t_{SU}	Set-up time	6	12		15		18		ns
t_H	Hold time	4.5	4		4		4		ns
t_{REM}	$\overline{CLR}$ to clock, Removal time	6	16		20		24		ns

4.6 Switching Characteristics

Input t_r, t_f = 6ns. C_L = 50pF unless otherwise noted

PARAMETER		V_{CC} (V)	25°C		– 40°C to 85°C	– 55°C to 125°C	UNIT
			TYP	MAX	MAX	MAX	
HC TYPES							
t_{PLH}, t_{PHL}	CLK to Q	2		170	212	255	ns
		4.5	14[(3)]	34	43	51	ns
		6		29	36	43	ns
t_{PLH}, t_{PHL}	$\overline{CLR}$ to Q	2		140	175	210	ns
		4.5	11[(3)]	28	35	42	ns
		6		24	30	36	ns
t_{TLH}, t_{THL}	Output transition times	2		75		110	ns
		4.5		15		22	ns
		6		13		19	ns
f_{MAX}	Maximum clock frequency	5	60[(3)]				ns
C_{IN}	Input capacitance			10	10	10	pF
C_{PD}	Power dissipation capacitance[(1) (2)]	5	47				pF
HCT TYPES							
t_{PLH}, t_{PHL}	CLK to Q	4.5		36	45	54	ns
		5	15[(3)]				
t_{PLH}, t_{PHL}	$\overline{CLR}$ to Q	4.5		38	46	57	ns
		5	16[(3)]				
t_{TLH}, t_{THL}	Output Transition time	4.5		15	19	22	ns
C_{IN}	Input Capacitance						pF
f_{MAX}	Maximum clock frequency		54[(4)]				MHz
C_{PD}	Power dissipation capacitance[(1) (2)]	5	49	10	10	10	pF

(1) C_{PD} is used to determine the dynamic power consumption, per device.
(2) $P_D = V_{CC}{}^2 f_i + \Sigma (C_L V_{CC}{}^2 + f_O)$ where f_i = Input Frequency, f_O = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.
(3) C_L = 15pF. V_{CC} = 5.
(4) C_L = 15pF.

5 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t < 6ns.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.

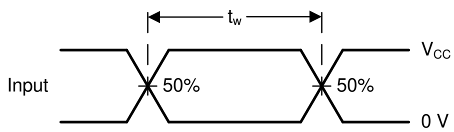


Figure 5-1. Voltage Waveforms, Standard CMOS Inputs Pulse Duration

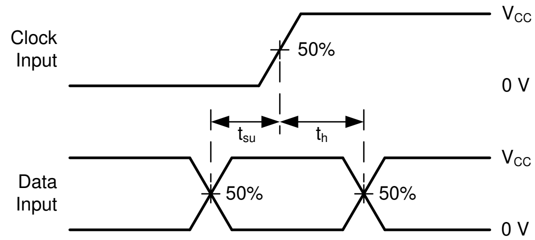


Figure 5-2. Voltage Waveforms, Standard CMOS Inputs Setup and Hold Times

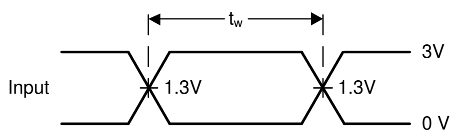


Figure 5-3. Voltage Waveforms, TTL-Compatible CMOS Inputs Pulse Duration

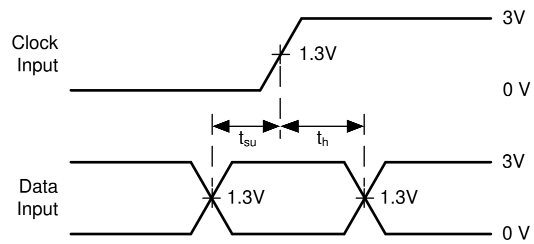


Figure 5-4. Voltage Waveforms, TTL-Compatible CMOS Inputs Setup and Hold Times

6 Detailed Description

6.1 Overview

The ’HC164 and ’HCT164 are 8-bit, serial-in, parallel-out, shift registers with asynchronous reset. Data is shifted on the positive edge of Clock (CLK). A LOW on the RESET ($\overline{CLR}$) pin resets the shift register and all outputs go to the LOW state regardless of the input conditions. Two Serial Data inputs (A and B) are provided, either one can be used as a data enable control.

6.2 Functional Block Diagram

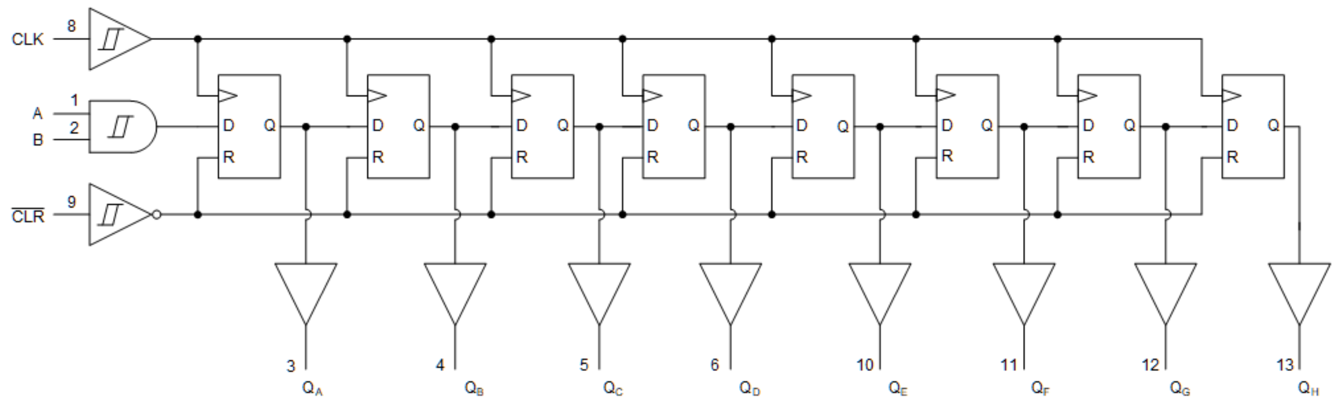


Figure 6-1. Functional Block Diagram

6.3 Device Functional Modes

Truth Table(1)

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{CLR}$	CLK	A	B	Q_A	Q_B- Q_H
RESET (CLEAR)	**L**	**X**	**X**	**X**	**L**	**L - L**
Shift	H	↑	l	l	L	q_A - q_F
	H	↑	l	h	L	q_A - q_F
	H	↑	h	l	L	q_A - q_F
	H	↑	h	h	H	q_A - q_F

(1) H = High voltage level.
h = High voltage level one set-up time prior to the low-to-high clock transition.
l = Low voltage level one set-up time prior to the low-to-high clock transition.
L = Low voltage level.
X = Don't care.
↑ = Transition from low to high level.
q_n = Lower case letters indicate the state of the reference input clock transition.

7 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating, located in the *Recommended Operating Conditions*. Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. TI recommends a 0.1μF capacitor for this device. Paralleling multiple bypass caps is acceptable to reject different frequencies of noise. The 0.1μF and 1μF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for better results.

8 Layout

8.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must not be left floating. In many cases, functions of digital logic devices, or parts of functions, are unused. For example, when a triple-input AND gate only uses two inputs or the buffer gates only use three of the four buffers. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2022) to Revision E (March 2024) **Page**

- Updated the functional block diagram image............ 1

Changes from Revision C (August 2003) to Revision D (March 2022) **Page**

- Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect current data sheet standards............ 1
- Updated naming conventions to reflect modern TI function. DS1 is now A; DS2 is now B; Q_0 is now Q_A; Q_1 is now Q_B; Q_2 is now Q_C; Q_3 is now Q_D; CP is now CLK; $\overline{MR}$ is now $\overline{CLR}$; Q_4 is now Q_E; Q_5 is now Q_F; Q_6 is now Q_G; Q_7 is now Q_H 3

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8970401CA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8970401CA CD54HCT164F3A
CD54HC164F	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC164F
CD54HC164F.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC164F
CD54HC164F3A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8416201CA CD54HC164F3A
CD54HC164F3A.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8416201CA CD54HC164F3A
CD54HCT164F3A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8970401CA CD54HCT164F3A
CD54HCT164F3A.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8970401CA CD54HCT164F3A
CD74HC164E	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC164E
CD74HC164E.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC164E
CD74HC164M	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	HC164M
CD74HC164M96	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC164M
CD74HC164M96.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC164M
CD74HC164M96G4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC164M
CD74HC164MT	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	HC164M
CD74HCT164E	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT164E
CD74HCT164E.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT164E
CD74HCT164M	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	HCT164M
CD74HCT164M96	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	(HCT164, HCT164M)
CD74HCT164M96.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	(HCT164, HCT164M)

[1] **Status:** For more details on status, see our product life cycle.

[2] **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

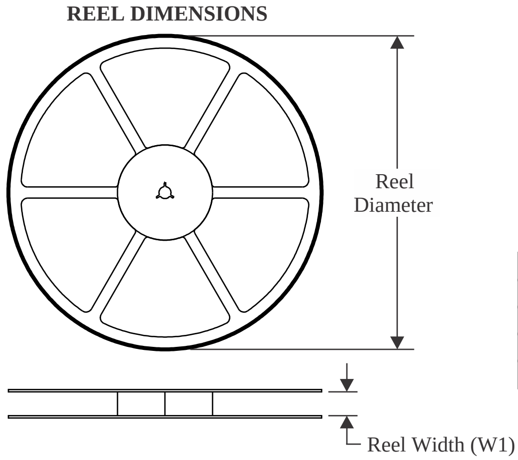
OTHER QUALIFIED VERSIONS OF CD54HC164, CD54HCT164, CD74HC164, CD74HCT164 :

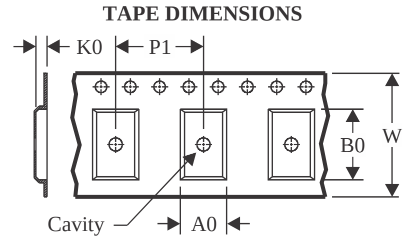
- Catalog : CD74HC164, CD74HCT164
- Military : CD54HC164, CD54HCT164

NOTE: Qualified Version Definitions:

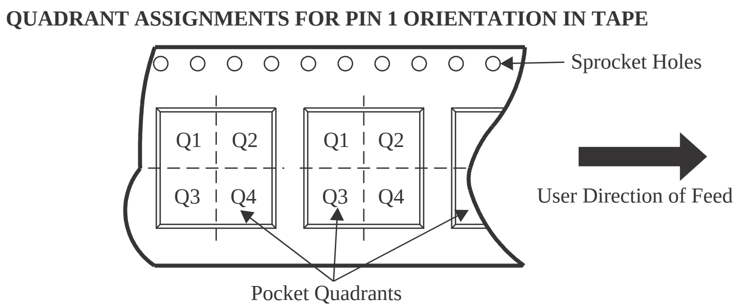
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION





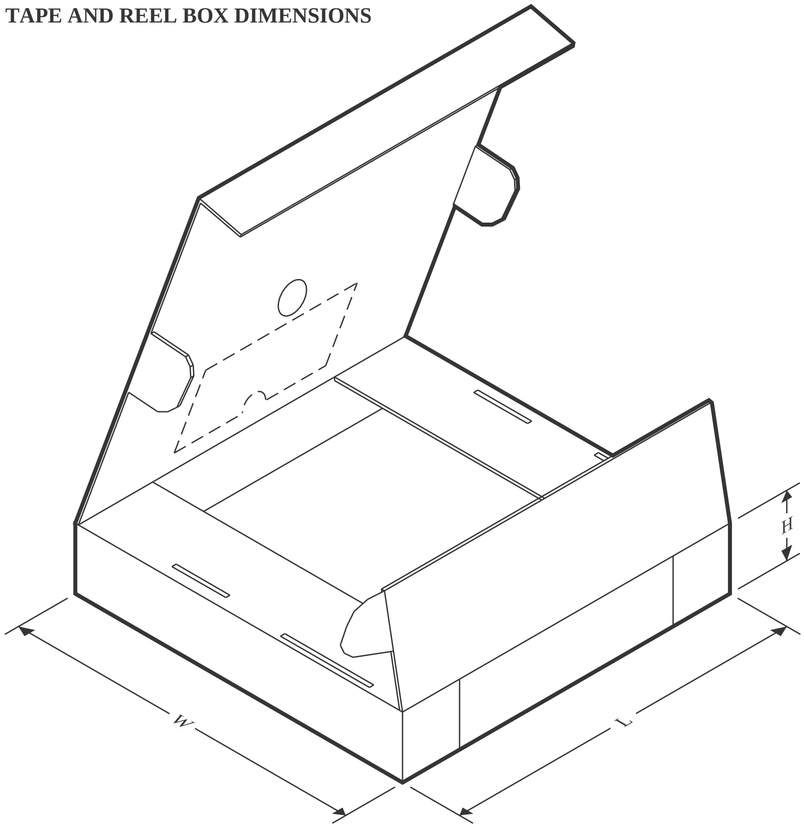
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC164M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HCT164M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

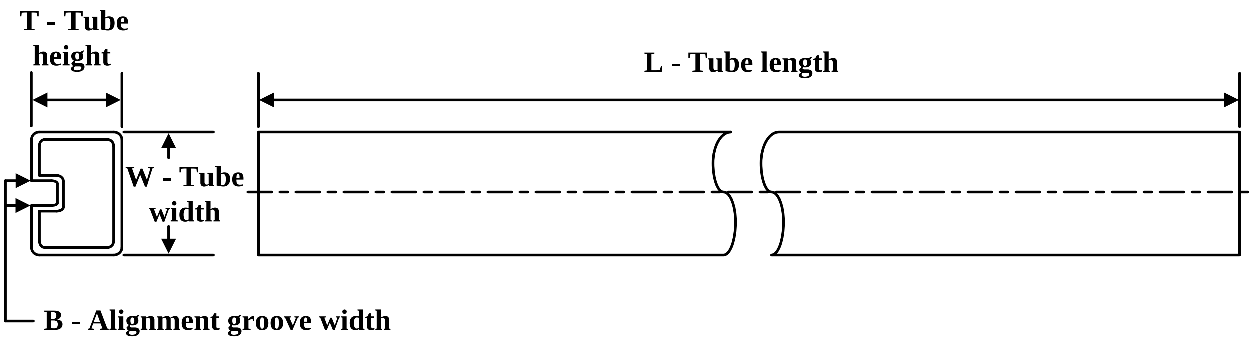
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC164M96	SOIC	D	14	2500	353.0	353.0	32.0
CD74HCT164M96	SOIC	D	14	2500	353.0	353.0	32.0

TUBE

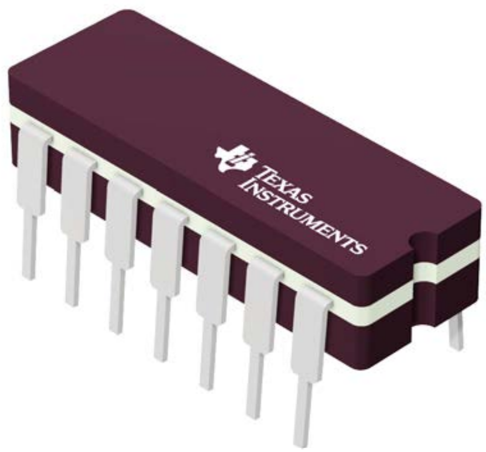


*All dimensions are nominal

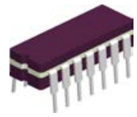
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC164E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC164E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC164E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC164E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT164E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT164E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT164E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT164E.A	N	PDIP	14	25	506	13.97	11230	4.32

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



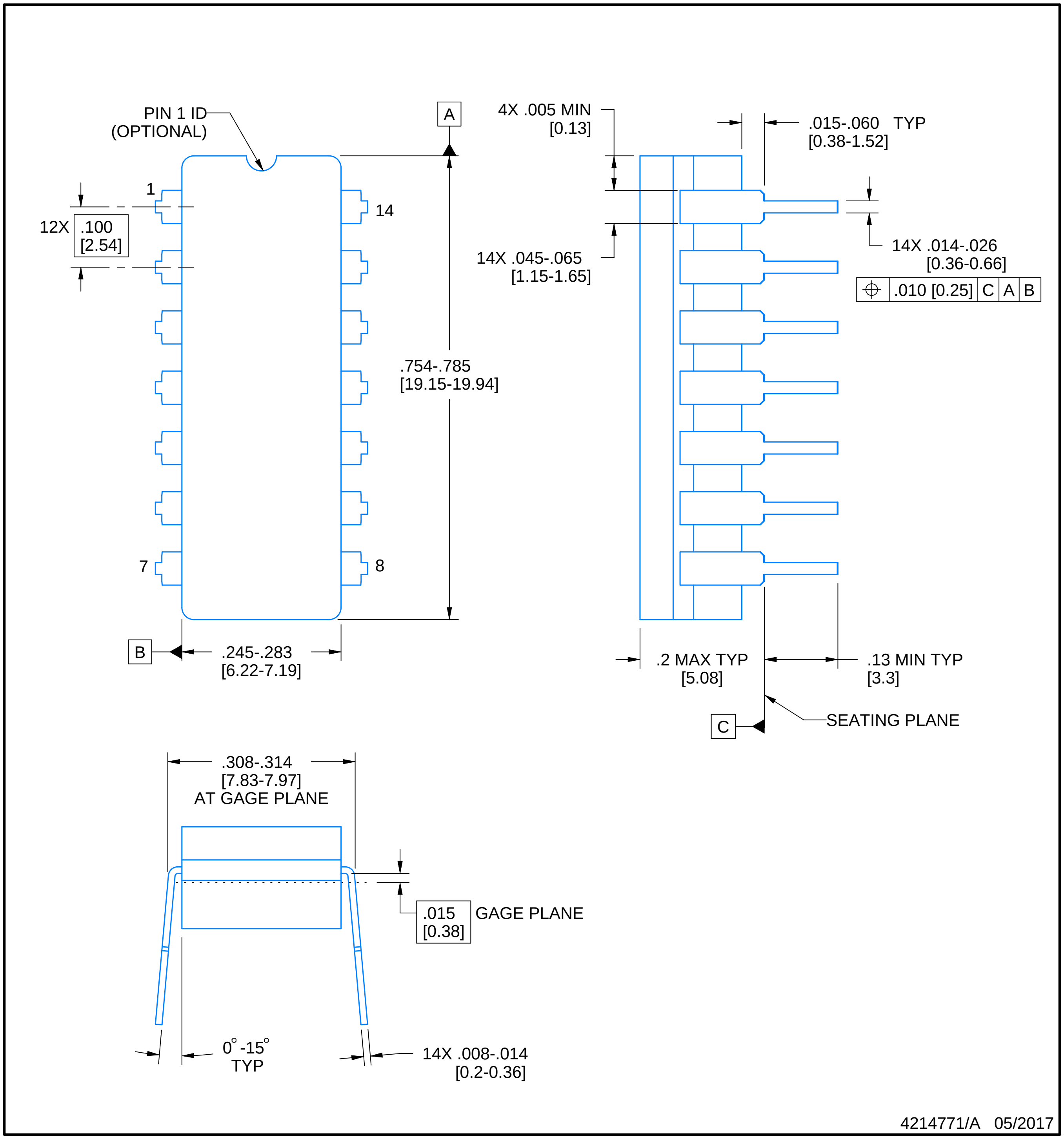
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



PACKAGE OUTLINE

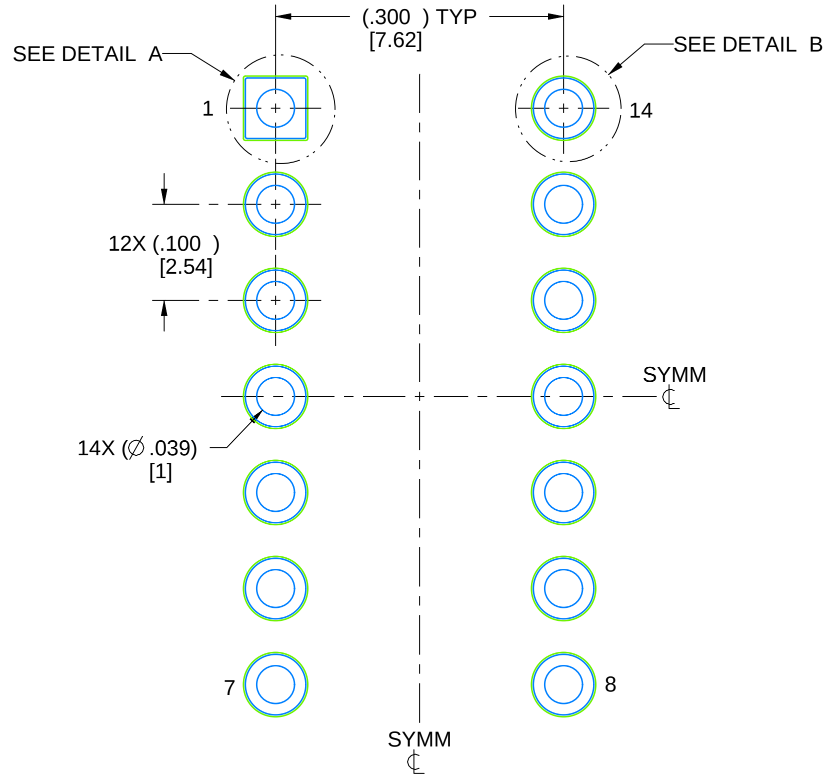
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE

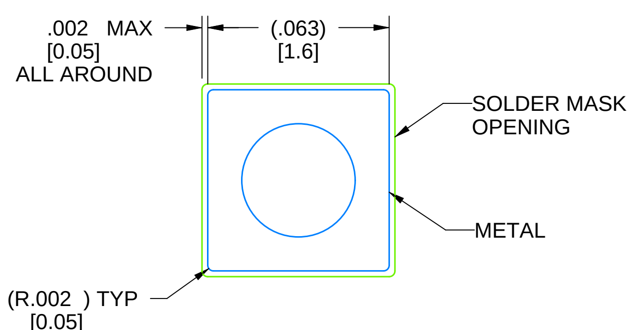


NOTES:

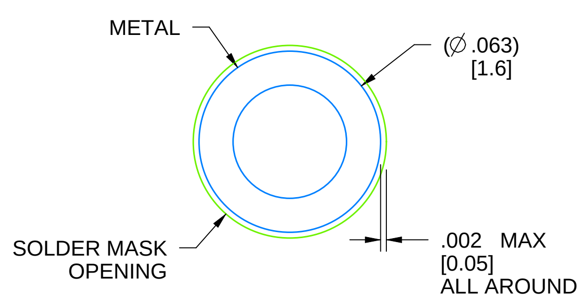
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X

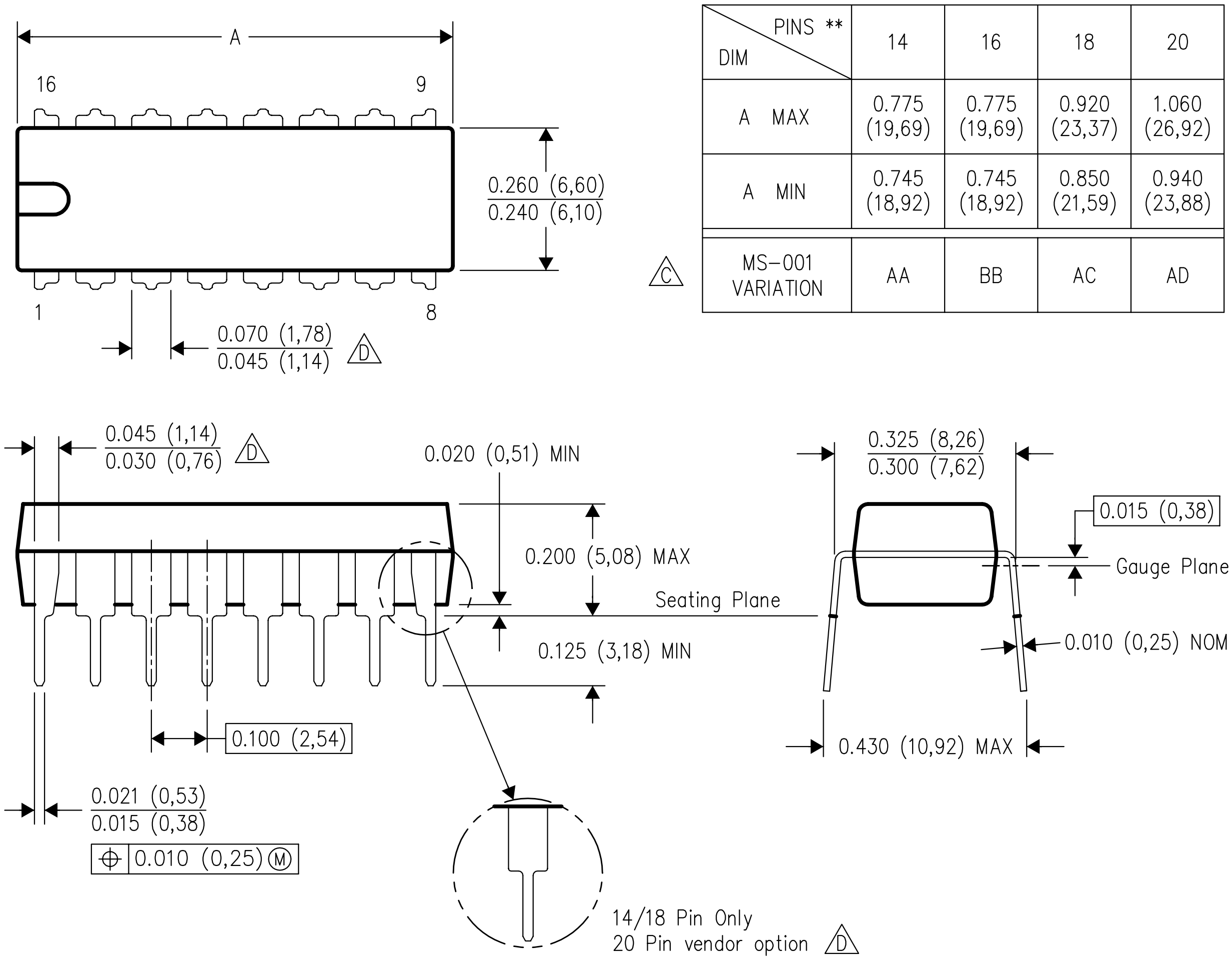


DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

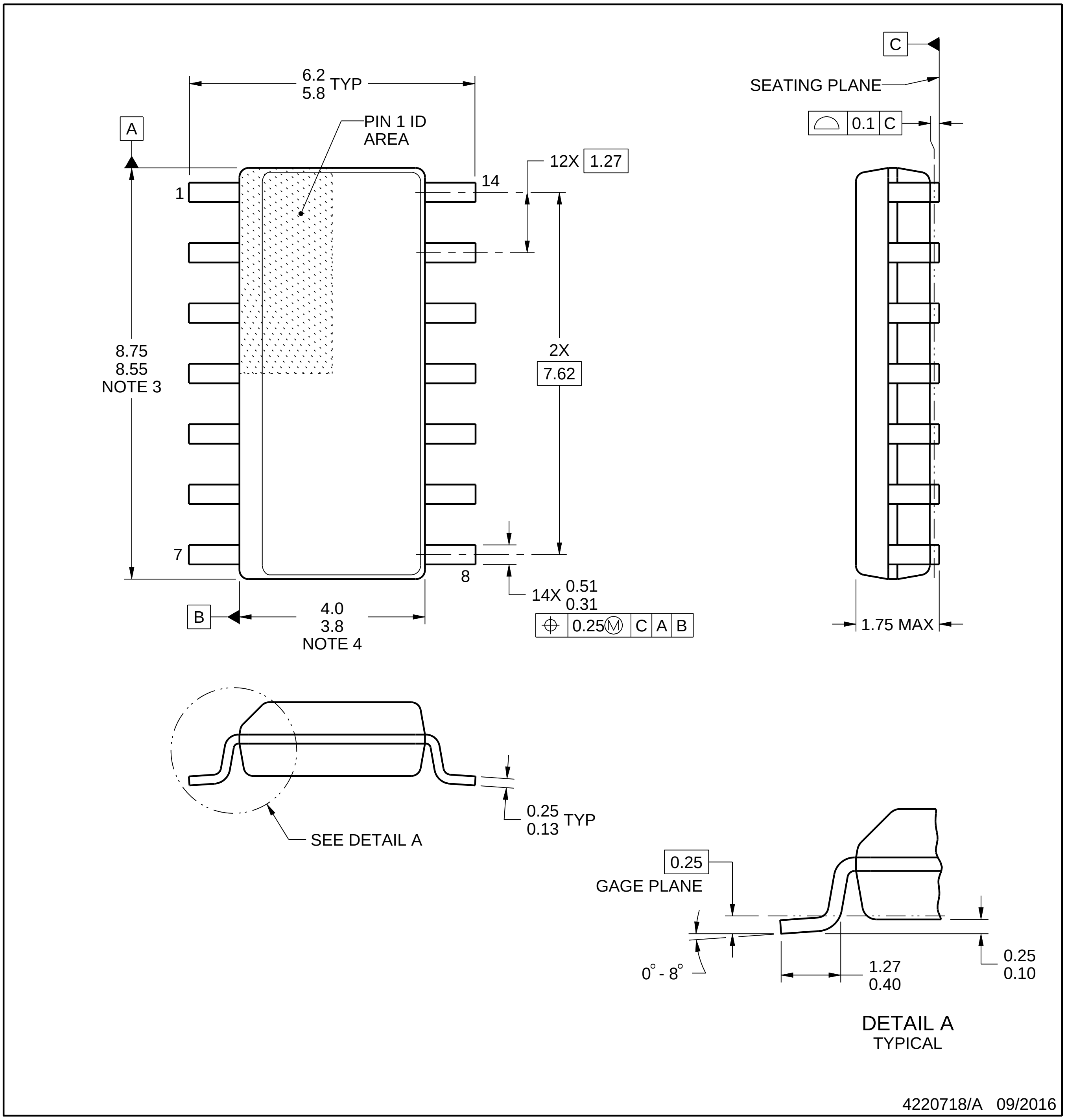
16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD

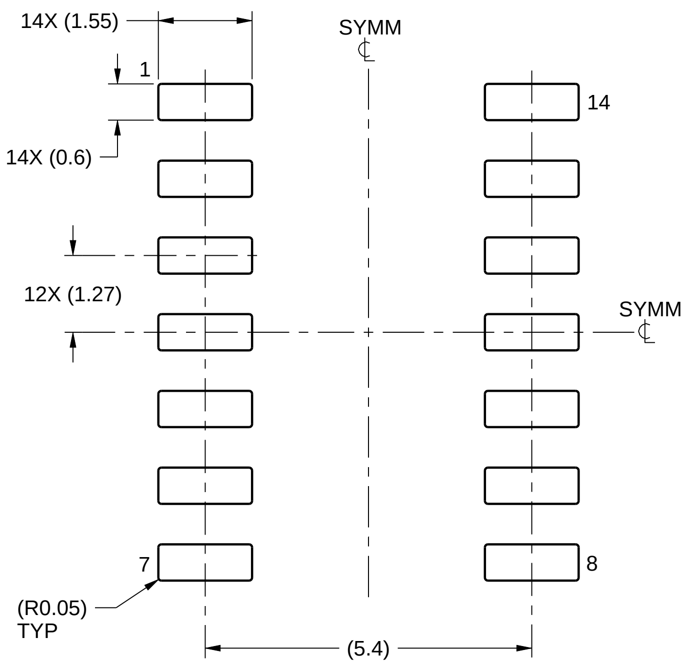
4040049/E 12/2002

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

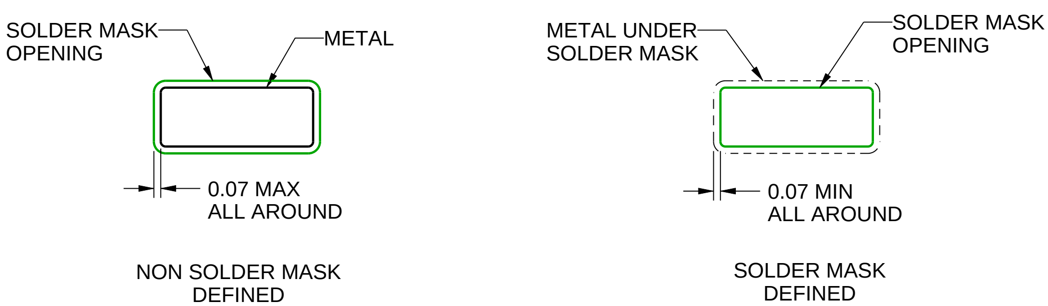


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

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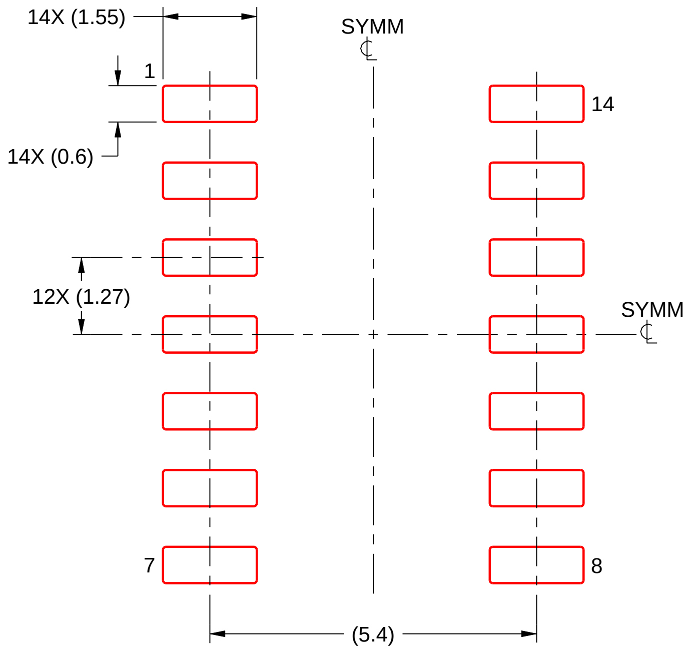
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.