

## CMOS 8-Bit Priority Encoder

### High-Voltage Types (20-Volt Rating)

■ CD4532B consists of combination logic that encodes the highest priority input (D7-D0) to a 3-bit binary code. The eight inputs, D7 through D0, each have an assigned priority; D7 is the highest priority and D0 is the lowest. The priority encoder is inhibited when the chip-enable input  $E_I$  is low. When  $E_I$  is high, the binary representation of the highest-priority input appears on output lines Q2-Q0, and the group select line GS is high to indicate that priority inputs are present. The enable-out ( $E_O$ ) is high when no priority inputs are present. If any one input is high,  $E_O$  is low and all cascaded lower-order stages are disabled.

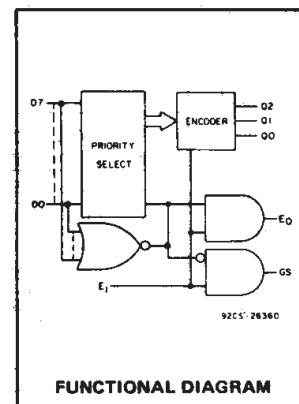
The CD4532B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

#### Features:

- Converts from 1 of 8 to binary
- Provides cascading feature to handle any number of inputs
- Group select indicates one or more priority inputs
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1  $\mu$ A at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range):
  - 0.5 V at  $V_{DD} = 5$  V
  - 1.5 V at  $V_{DD} = 10$  V
  - 1.5 V at  $V_{DD} = 15$  V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

#### Applications:

- Priority encoder
- Binary or BCD encoder (keyboard encoding)
- Floating point arithmetic



#### RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

| Characteristic                                              | Min. | Max. | Units |
|-------------------------------------------------------------|------|------|-------|
| Supply Voltage Range (for $T_A =$ Full Package Temp. Range) | 3    | 18   | V     |

#### MAXIMUM RATINGS, Absolute-Maximum Values:

##### DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )

Voltages referenced to  $V_{SS}$  Terminal) ..... -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to  $V_{DD} + 0.5$ V

DC INPUT CURRENT, ANY ONE INPUT .....  $\pm 10$ mA

##### POWER DISSIPATION PER PACKAGE ( $P_D$ ):

For  $T_A = -55^\circ\text{C}$  to  $+100^\circ\text{C}$  ..... 500mW

For  $T_A = +100^\circ\text{C}$  to  $+125^\circ\text{C}$  ..... Derate Linearly at 12mW/ $^\circ\text{C}$  to 200mW

##### DEVICE DISSIPATION PER OUTPUT TRANSISTOR

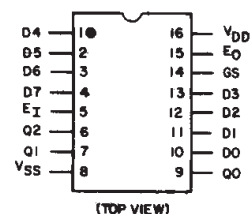
FOR  $T_A =$  FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100mW

OPERATING-TEMPERATURE RANGE ( $T_A$ ) .....  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

STORAGE TEMPERATURE RANGE ( $T_{stg}$ ) .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$

##### LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16  $\pm$  1/32 inch (1.59  $\pm$  0.79mm) from case for 10s max .....  $+265^\circ\text{C}$



#### TERMINAL ASSIGNMENT

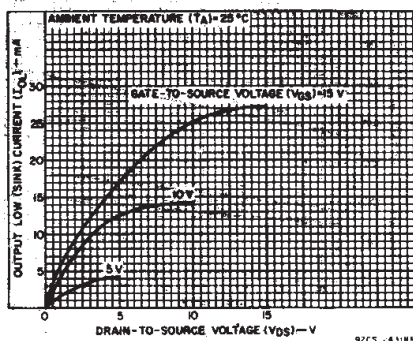


Fig. 1 - Typical output low (sink) current characteristics.

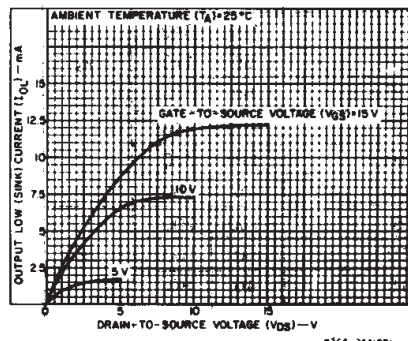


Fig. 2 - Minimum output low (sink) current characteristics.

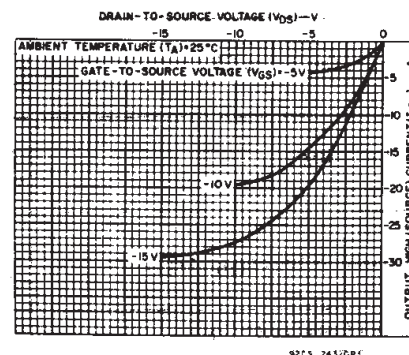


Fig. 3 - Typical output high (source) current characteristics.

# CD4532B Types

## STATIC ELECTRICAL CHARACTERISTICS

| CHARACTER-<br>ISTIC                                         | CONDITIONS            |                        |                        | LIMITS AT INDICATED TEMPERATURES (°C) |       |       |       |       |                   |      | UNITS |
|-------------------------------------------------------------|-----------------------|------------------------|------------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
|                                                             | V <sub>O</sub><br>(V) | V <sub>IN</sub><br>(V) | V <sub>DD</sub><br>(V) | +25                                   |       |       |       |       |                   |      |       |
|                                                             |                       |                        |                        | -55                                   | -40   | +85   | +125  | Min.  | Typ.              | Max. |       |
| Quiescent Device<br>Current,<br>I <sub>DD</sub> Max.        | —                     | 0,5                    | 5                      | 5                                     | 5     | 150   | 150   | —     | 0.04              | 5    | μA    |
|                                                             | —                     | 0,10                   | 10                     | 10                                    | 10    | 300   | 300   | —     | 0.04              | 10   |       |
|                                                             | —                     | 0,15                   | 15                     | 20                                    | 20    | 600   | 600   | —     | 0.04              | 20   |       |
|                                                             | —                     | 0,20                   | 20                     | 100                                   | 100   | 3000  | 3000  | —     | 0.08              | 100  |       |
| Output Low<br>(Sink) Current<br>I <sub>OL</sub> Min.        | 0.4                   | 0,5                    | 5                      | 0.64                                  | 0.61  | 0.42  | 0.36  | 0.51  | 1                 | —    | mA    |
|                                                             | 0.5                   | 0,10                   | 10                     | 1.6                                   | 1.5   | 1.1   | 0.9   | 1.3   | 2.6               | —    |       |
|                                                             | 1.5                   | 0,15                   | 15                     | 4.2                                   | 4     | 2.8   | 2.4   | 3.4   | 6.8               | —    |       |
| Output High<br>(Source)<br>Current,<br>I <sub>OH</sub> Min. | 4.6                   | 0,5                    | 5                      | -0.64                                 | -0.61 | -0.42 | -0.36 | -0.51 | -1                | —    | mA    |
|                                                             | 2.5                   | 0,5                    | 5                      | -2                                    | -1.8  | -1.3  | -1.15 | -1.6  | -3.2              | —    |       |
|                                                             | 9.5                   | 0,10                   | 10                     | -1.6                                  | -1.5  | -1.1  | -0.9  | -1.3  | -2.6              | —    |       |
|                                                             | 13.5                  | 0,15                   | 15                     | -4.2                                  | -4    | -2.8  | -2.4  | -3.4  | -6.8              | —    |       |
| Output Voltage:<br>Low-Level,<br>V <sub>OL</sub> Max.       | —                     | 0,5                    | 5                      | 0.05                                  |       |       |       | —     | 0                 | 0.05 | V     |
|                                                             | —                     | 0,10                   | 10                     | 0.05                                  |       |       |       | —     | 0                 | 0.05 |       |
|                                                             | —                     | 0,15                   | 15                     | 0.05                                  |       |       |       | —     | 0                 | 0.05 |       |
| Output Voltage:<br>High-Level,<br>V <sub>OH</sub> Min.      | —                     | 0,5                    | 5                      | 4.95                                  |       |       |       | 4.95  | 5                 | —    | V     |
|                                                             | —                     | 0,10                   | 10                     | 9.95                                  |       |       |       | 9.95  | 10                | —    |       |
|                                                             | —                     | 0,15                   | 15                     | 14.95                                 |       |       |       | 14.95 | 15                | —    |       |
| Input Low<br>Voltage,<br>V <sub>IL</sub> Max. *             | 0.5, 4.5              | —                      | 5                      | 1                                     |       |       |       | —     | —                 | 1.5  | V     |
|                                                             | 1, 9                  | —                      | 10                     | 2.5                                   |       |       |       | —     | —                 | 3    |       |
|                                                             | 1.5,13.5              | —                      | 15                     | 3                                     |       |       |       | —     | —                 | 4    |       |
| Input High<br>Voltage,<br>V <sub>IH</sub> Min. *            | 0.5, 4.5              | —                      | 5                      | 4                                     |       |       |       | 3.5   | —                 | —    | V     |
|                                                             | 1, 9                  | —                      | 10                     | 7.5                                   |       |       |       | 7     | —                 | —    |       |
|                                                             | 1.5,13.5              | —                      | 15                     | 12                                    |       |       |       | 11    | —                 | —    |       |
| Input Current<br>I <sub>IN</sub> Max.                       |                       | 0,18                   | 18                     | ±0.1                                  | ±0.1  | ±1    | ±1    | —     | ±10 <sup>-5</sup> | ±0.1 | μA    |

\*One input is tested at a time; other inputs should be at V<sub>DD</sub> or V<sub>SS</sub>. For testing all inputs at V<sub>IL</sub> and V<sub>IH</sub> levels, use 20%/80% V<sub>DD</sub>.

DYNAMIC ELECTRICAL CHARACTERISTICS at T<sub>A</sub>=25°C; C<sub>L</sub>=50 pF,  
Input t<sub>r</sub>, t<sub>f</sub>= 20 ns, R<sub>L</sub>=200 kΩ

| CHARACTERISTIC                                                                                                                    | TEST CONDITIONS<br>V <sub>DD</sub><br>VOLTS | LIMITS |      | UNITS |
|-----------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------|--------|------|-------|
|                                                                                                                                   |                                             | TYP.   | MAX. |       |
| Propagation Delay Time t <sub>PHL</sub> , t <sub>PLH</sub><br>E <sub>I</sub> to E <sub>O</sub> , E <sub>I</sub> to G <sub>S</sub> | 5                                           | 110    | 220  | ns    |
|                                                                                                                                   | 10                                          | 55     | 110  |       |
|                                                                                                                                   | 15                                          | 45     | 85   |       |
| E <sub>I</sub> to Q <sub>M</sub> , D <sub>n</sub> to G <sub>S</sub>                                                               | 5                                           | 170    | 340  |       |
|                                                                                                                                   | 10                                          | 85     | 170  |       |
|                                                                                                                                   | 15                                          | 65     | 125  |       |
| D <sub>n</sub> to Q <sub>M</sub>                                                                                                  | 5                                           | 220    | 440  | ns    |
|                                                                                                                                   | 10                                          | 110    | 220  |       |
|                                                                                                                                   | 15                                          | 85     | 160  |       |
| Transition Time t <sub>THL</sub> , t <sub>TLH</sub>                                                                               | 5                                           | 100    | 200  | ns    |
|                                                                                                                                   | 10                                          | 50     | 100  |       |
|                                                                                                                                   | 15                                          | 40     | 80   |       |
| Input Capacitance C <sub>IN</sub>                                                                                                 | Any Input                                   | 5      | 7.5  | pF    |

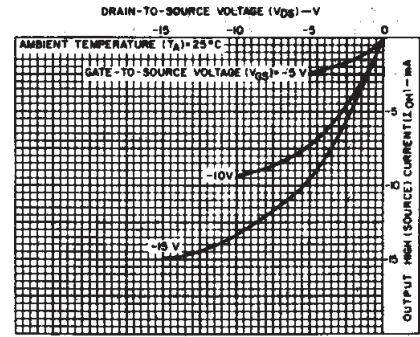


Fig. 4 — Minimum output high (source) current characteristics.

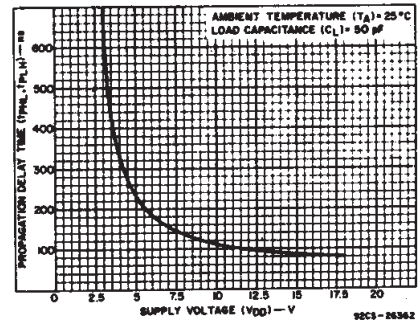


Fig. 5 — Typical propagation delay (D<sub>n</sub> to Q<sub>m</sub>) vs. supply voltage.

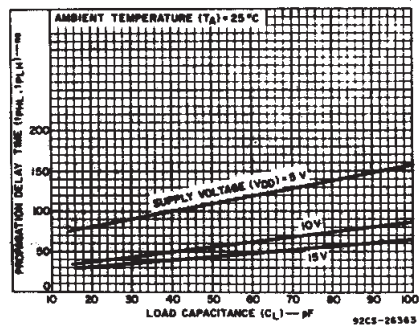


Fig. 6 — Typical propagation delay (E<sub>I</sub> to G<sub>S</sub>, E<sub>I</sub> to E<sub>O</sub>) vs. load capacitance.

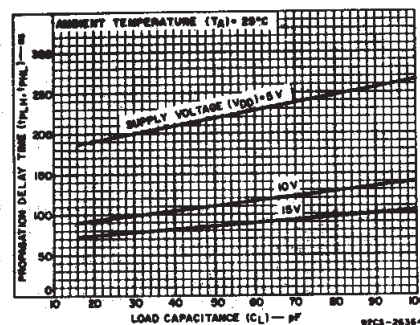
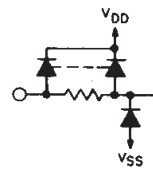
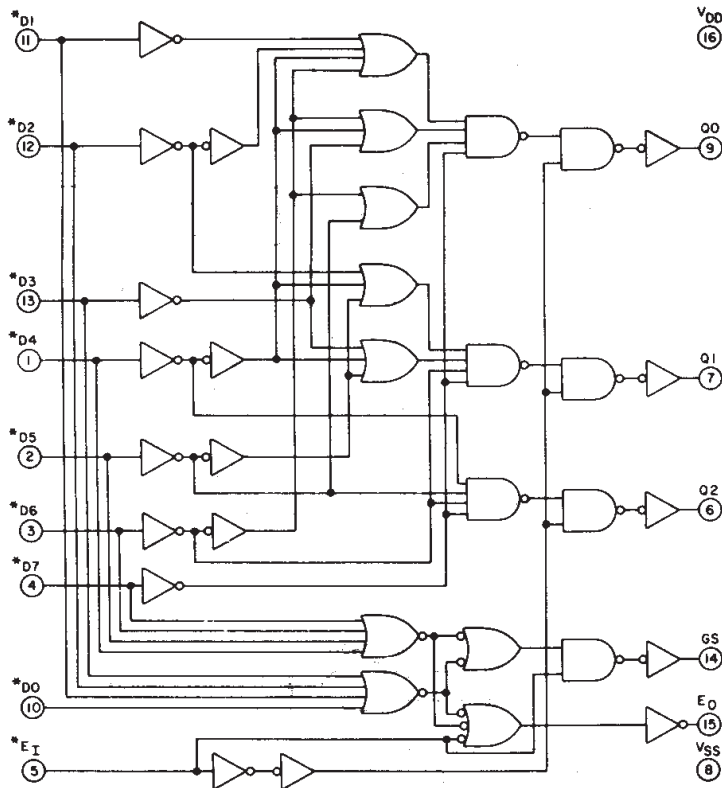


Fig. 7 — Typical propagation delay (D<sub>n</sub> to Q<sub>m</sub>) vs. load capacitance.

## CD4532B Types



\*ALL INPUTS PROTECTED BY CMOS PROTECTION NETWORK

Fig. 8 — CD4532 logic diagram.

TRUTH TABLE

| Input          |    |    |    |    |    |    |    |    | Output |    |    |    |                |
|----------------|----|----|----|----|----|----|----|----|--------|----|----|----|----------------|
| E <sub>I</sub> | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | GS     | Q2 | Q1 | Q0 | E <sub>O</sub> |
| 0              | X  | X  | X  | X  | X  | X  | X  | X  | 0      | 0  | 0  | 0  | 0              |
| 1              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0      | 0  | 0  | 0  | 1              |
| 1              | 1  | X  | X  | X  | X  | X  | X  | X  | 1      | 1  | 1  | 1  | 0              |
| 1              | 0  | 1  | X  | X  | X  | X  | X  | X  | 1      | 1  | 1  | 0  | 0              |
| 1              | 0  | 0  | 1  | X  | X  | X  | X  | X  | 1      | 1  | 0  | 1  | 0              |
| 1              | 0  | 0  | 0  | 1  | X  | X  | X  | X  | 1      | 1  | 0  | 0  | 0              |
| 1              | 0  | 0  | 0  | 0  | 1  | X  | X  | X  | 1      | 0  | 1  | 1  | 0              |
| 1              | 0  | 0  | 0  | 0  | 0  | 1  | X  | X  | 1      | 0  | 1  | 0  | 0              |
| 1              | 0  | 0  | 0  | 0  | 0  | 0  | 1  | X  | 1      | 0  | 0  | 1  | 0              |
| 1              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1      | 0  | 0  | 0  | 0              |

X = Don't Care

Logic 1  $\equiv$  High

Logic 0  $\equiv$  Low

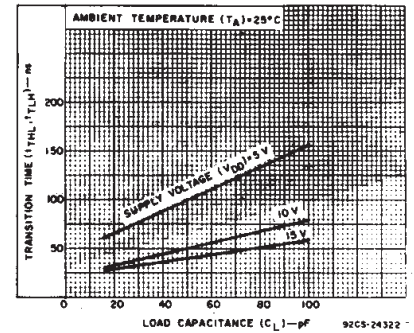


Fig. 9 — Typical transition time vs. load capacitance.

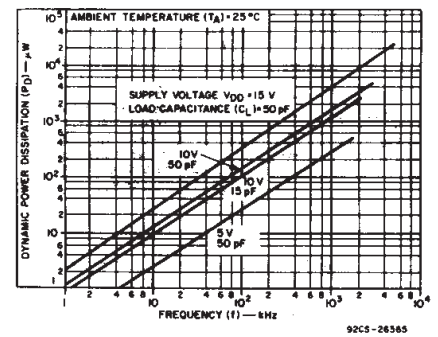


Fig. 10 — Typical dynamic power dissipation vs. frequency.

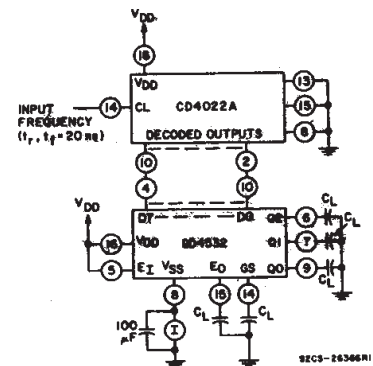


Fig. 11 — Dynamic power dissipation test circuit.

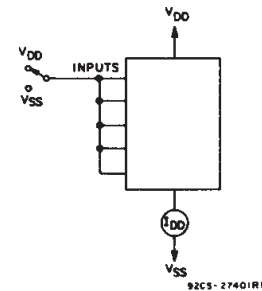


Fig. 12 — Quiescent device current test circuit.

## CD4532B Types

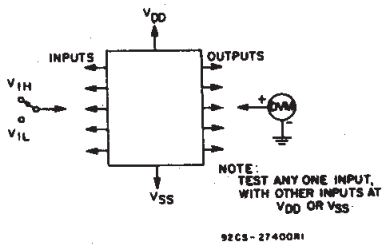


Fig. 13 - Input voltage test circuit.

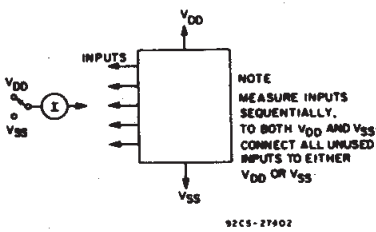
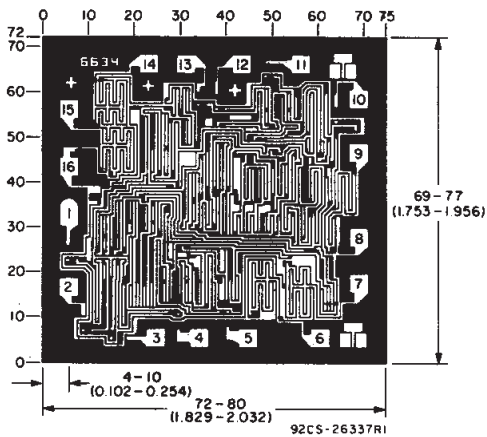


Fig. 14 - Input current test circuit.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

Dimensions and pad layout for CD4532BH.

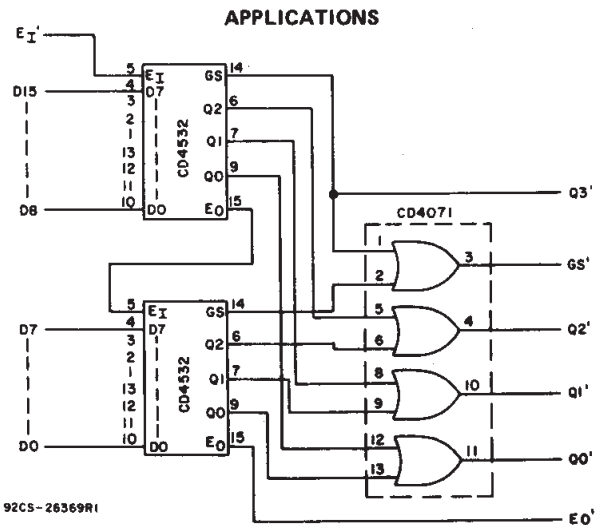
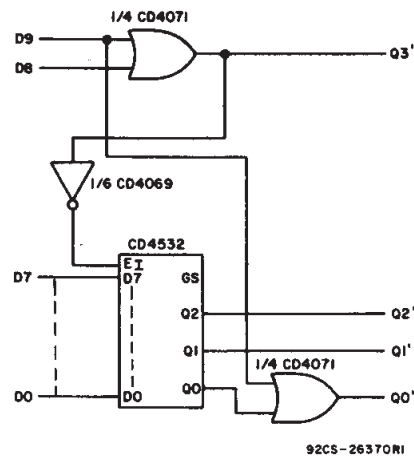


Fig. 15 - 16-level priority encoder.



TRUTH TABLE

| Input |    |    |    |    |    |    |    |    |    | Output |     |     |     |     |
|-------|----|----|----|----|----|----|----|----|----|--------|-----|-----|-----|-----|
| D9    | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | G5     | Q3' | Q2' | Q1' | Q0' |
| 1     | X  | X  | X  | X  | X  | X  | X  | X  | X  | 0      | 1   | 0   | 0   | 1   |
| 0     | 1  | X  | X  | X  | X  | X  | X  | X  | X  | 0      | 1   | 0   | 0   | 0   |
| 0     | 0  | 1  | X  | X  | X  | X  | X  | X  | X  | 1      | 0   | 1   | 1   | 1   |
| 0     | 0  | 0  | 1  | X  | X  | X  | X  | X  | X  | 1      | 0   | 1   | 1   | 0   |
| 0     | 0  | 0  | 0  | 1  | X  | X  | X  | X  | X  | 1      | 0   | 1   | 0   | 1   |
| 0     | 0  | 0  | 0  | 0  | 1  | X  | X  | X  | X  | 1      | 0   | 1   | 0   | 0   |
| 0     | 0  | 0  | 0  | 0  | 0  | 1  | X  | X  | X  | 1      | 0   | 0   | 1   | 1   |
| 0     | 0  | 0  | 0  | 0  | 0  | 0  | 1  | X  | X  | 1      | 0   | 0   | 1   | 0   |
| 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | X  | 1      | 0   | 0   | 0   | 1   |
| 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1      | 0   | 0   | 0   | 0   |

X = Don't Care

Logic 1  $\equiv$  High

Logic 0  $\equiv$  Low

Fig. 16 - 0-to-9 keyboard encoder.

## PACKAGING INFORMATION

| Orderable part number      | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|----------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">CD4532BE</a>   | Active        | Production           | PDIP (N)   16   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD4532BE            |
| CD4532BE.A                 | Active        | Production           | PDIP (N)   16   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD4532BE            |
| CD4532BEE4                 | Active        | Production           | PDIP (N)   16   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD4532BE            |
| <a href="#">CD4532BF3A</a> | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD4532BF3A          |
| CD4532BF3A.A               | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD4532BF3A          |
| <a href="#">CD4532BM</a>   | Obsolete      | Production           | SOIC (D)   16   | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | CD4532BM            |
| <a href="#">CD4532BM96</a> | Active        | Production           | SOIC (D)   16   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | CD4532BM            |
| CD4532BM96.A               | Active        | Production           | SOIC (D)   16   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | CD4532BM            |
| <a href="#">CD4532BNSR</a> | Active        | Production           | SOP (NS)   16   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | CD4532B             |
| CD4532BNSR.A               | Active        | Production           | SOP (NS)   16   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | CD4532B             |
| <a href="#">CD4532BPWR</a> | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | CM532B              |
| CD4532BPWR.A               | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | CM532B              |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD4532B, CD4532B-MIL :**

- Catalog : [CD4532B](#)
- Military : [CD4532B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD4532BM96 | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| CD4532BNSR | SOP          | NS              | 16   | 2000 | 330.0              | 16.4               | 8.1     | 10.4    | 2.5     | 12.0    | 16.0   | Q1            |
| CD4532BPWR | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD4532BM96 | SOIC         | D               | 16   | 2500 | 353.0       | 353.0      | 32.0        |
| CD4532BNSR | SOP          | NS              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| CD4532BPWR | TSSOP        | PW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |

## TUBE



\*All dimensions are nominal

| Device     | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CD4532BE   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD4532BE   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD4532BE.A | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD4532BE.A | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD4532BEE4 | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD4532BEE4 | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



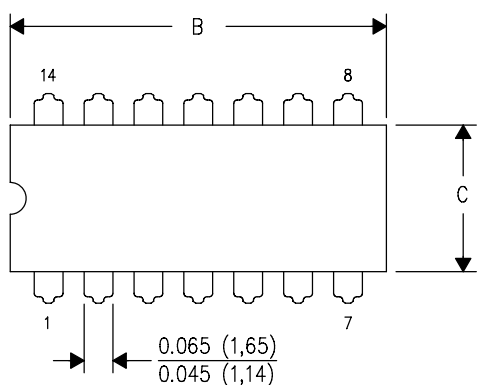
4040047-6/M 06/11

NOTES:

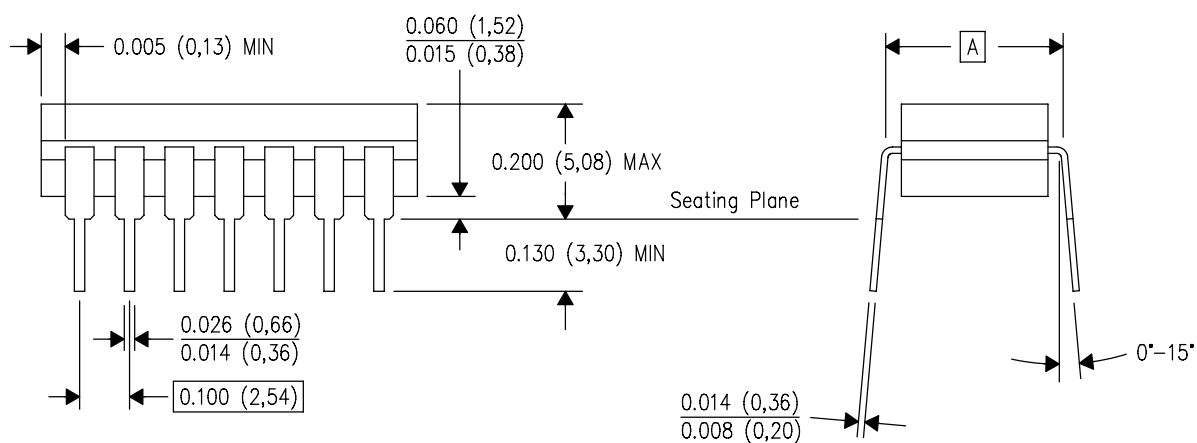
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



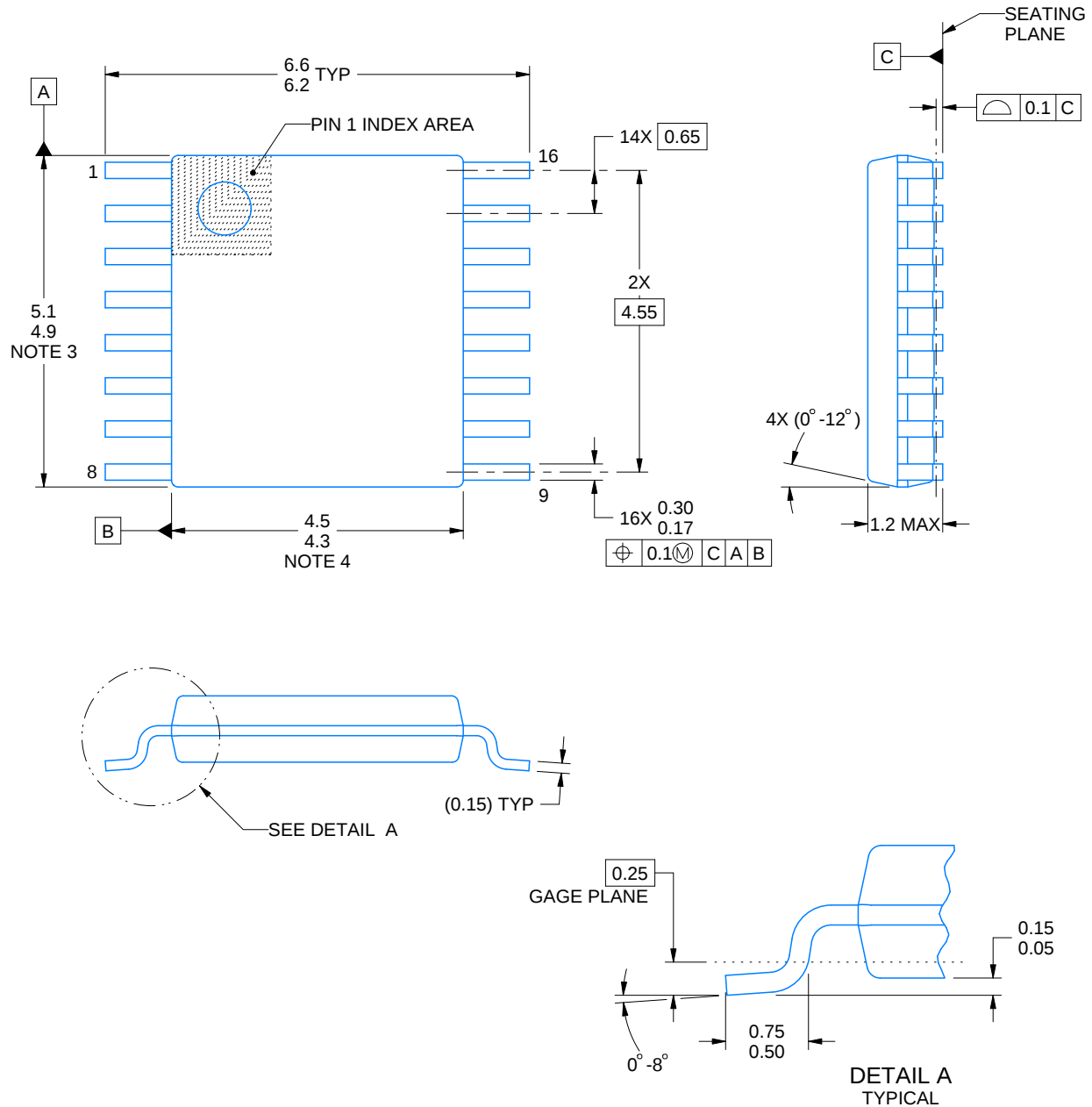
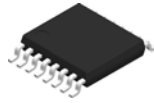
| DIM \ PINS ** | 14                     | 16                     | 18                     | 20                     |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A             | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX         | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN         | —                      | —                      | —                      | —                      |
| C MAX         | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN         | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



4220204/B 12/2023

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



# PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

## NOTES:

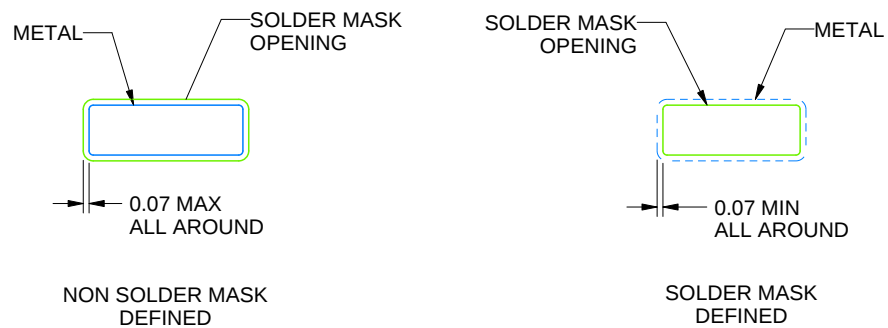
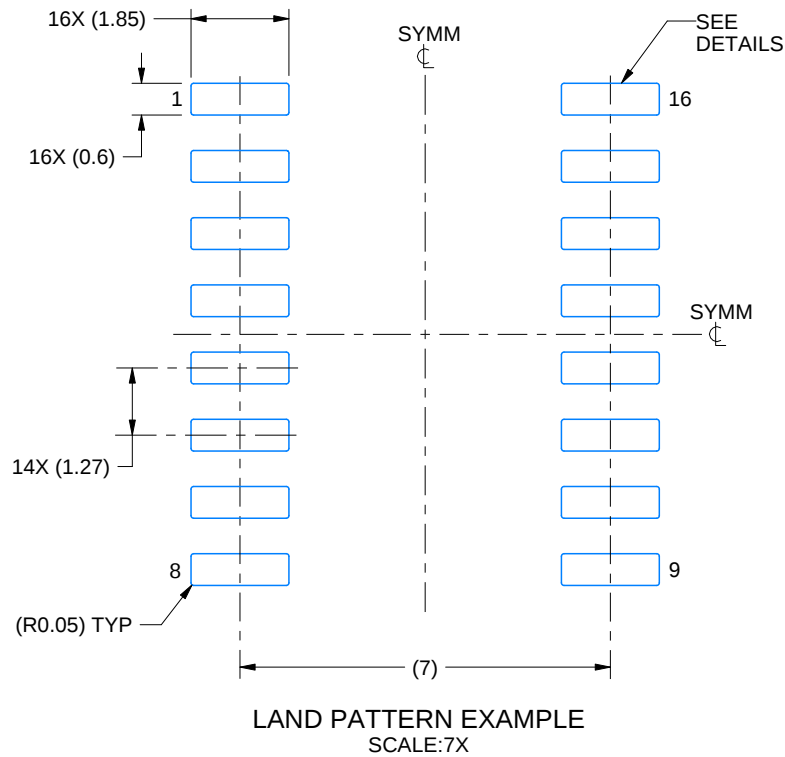
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



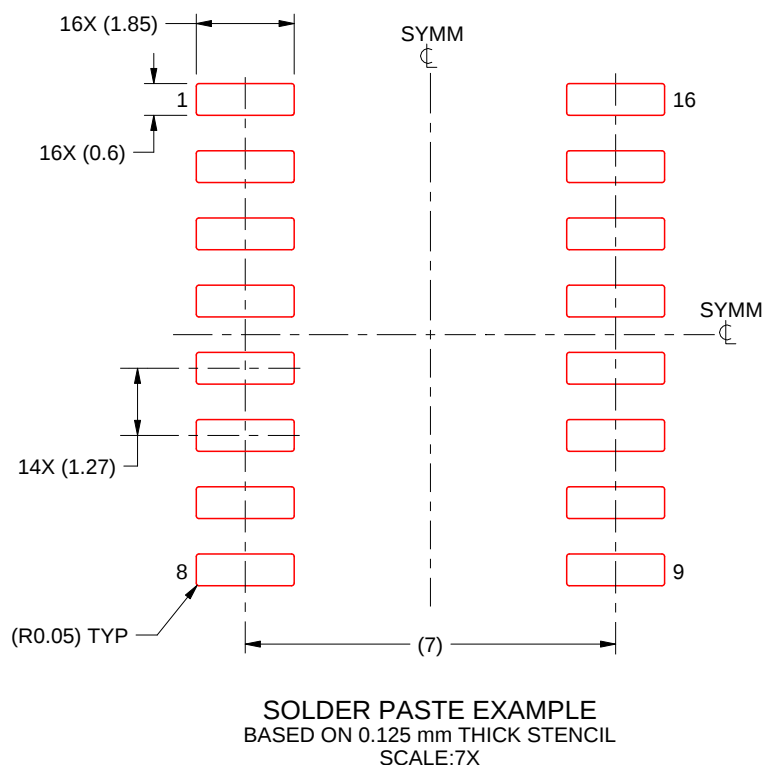
SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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