CD4053B-Q1 Automotive CMOS Single 8-Channel Analog Multiplexer or Demultiplexer with Logic-Level Conversion

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –45°C to +125°C, T_A
- Wide range of digital and analog signal levels:
  - Digital: 3V to 20V
  - Analog: ≤ $20V_{P-P}$
- Low ON resistance, 125Ω (typical) over 15VP-P signal input range for VDD – VEE = 18V
- High OFF resistance, channel leakage of ±100pA (typical) at VDD – VEE = 18V
- Logic-level conversion for digital addressing signals of 3V to 20V (VDD – VSS = 3V to 20V) to switch analog signals to 20VP-P (VDD – VEE = 20V) matched switch characteristics, r_{ON} = 5Ω (typical) for VDD – VEE = 15V very low quiescent power dissipation under all digital-control input and supply conditions, 0.2µW (typical) at VDD – VSS = VDD – VEE = 10V
- Binary address decoding on chip
- 5V, 10V, and 15V parametric ratings
- 100% tested for quiescent current at 20V
- Maximum input current of 1µA at 18V over full package temperature range, 100nA at 18V and 25°C
- Break-before-make switching eliminates channel overlap
- Pin compatible with Industry Standard 4053 Multiplexers

2 Applications

- Analog and digital multiplexing and demultiplexing
- Analog to digital and digital to analog conversion
- Signal gating
- Factory automation
- Televisions
- Appliances
- Consumer audio
- Programmable logic circuits
- Sensors

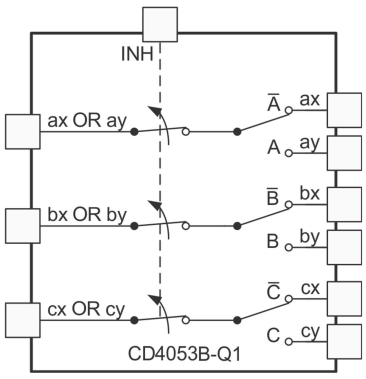
3 Description

The CD4053B-Q1 analog multiplexers and demultiplexers are digitally-controlled analog switches having low ON impedance and very low OFF leakage current. These multiplexer circuits dissipate extremely low quiescent power over the full V_{DD} – V_{SS} and V_{DD} – V_{EE} supply-voltage ranges, independent of the logic state of the control signals.

Package Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE(2)
CD4053B-Q1	D (SOIC, 16)	9.9mm × 6mm
	PW (TSSOP, 16)	5mm × 6.4mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Functional Diagrams of CD4053B-Q1

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4 Pin Configuration and Functions

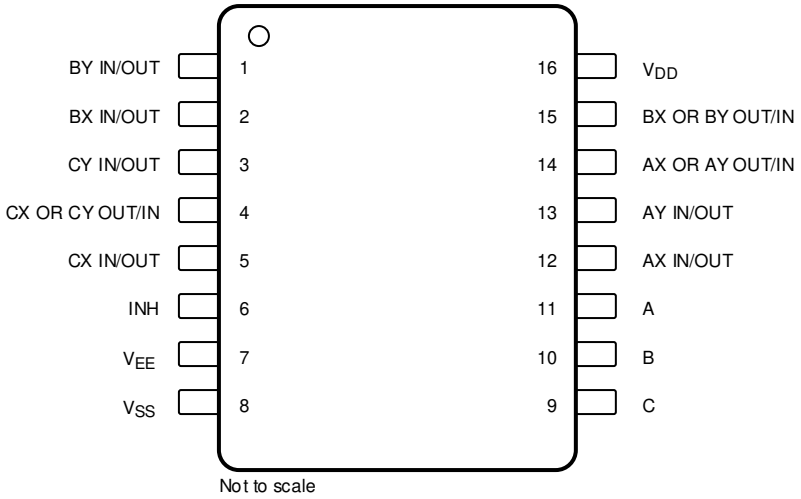


Figure 4-1. CD4053B-Q1 D or PW Package, (Top View)

Table 4-1. Pin Functions CD4053B-Q1

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	BY IN/OUT	I/O	B channel Y in/out
2	BX IN/OUT	I/O	B channel X in/out
3	CY IN/OUT	I/O	C channel Y in/out
4	CX OR CY OUT/IN	I/O	C common out/in
5	CX IN/OUT	I/O	C channel X in/out
6	INH	I	Disables all channels. See Table 7-1.
7	V_{EE}	—	Negative power input
8	V_{SS}	—	Ground
9	C	I	Channel select C. See Table 7-1.
10	B	I	Channel select B. See Table 7-1.
11	A	I	Channel select A. See Table 7-1.
12	AX IN/OUT	I/O	A channel X in/out
13	AY IN/OUT	I/O	A channel Y in/out
14	AX OR AY OUT/IN	I/O	A common out/in
15	BX OR BY OUT/IN	I/O	B common out/in
16	V_{DD}	—	Positive power input

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
	Supply Voltage	V+ to V-, Voltages Referenced to V_{SS} Terminal	–0.5	20	V
	DC Input Voltage		–0.5	V_{DD}+0.5	V
	DC Input Current	Any One Input	–10	10	mA
T_{JMAX1}	Maximum junction temperature, ceramic package			175	°C
T_{JMAX2}	Maximum junction temperature, plastic package			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Temperature Range	–55		125	°C

5.4 Thermal Information

THERMAL METRIC[1]		CD4053B-Q1		UNIT
		D (SOIC)	PW (TSSOP)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.7	116.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.3	47.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.3	63.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	12.1	6.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	44.9	62.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics - CD4053B-Q1

Over operating free-air temperature range, V_{SUPPLY} = ±5 V, and R_L = 100 Ω, (unless otherwise noted) (1)

PARAMETER	TEST CONDITIONS					MIN	TYP	MAX	UNIT
SIGNAL INPUTS (V_{IS}) AND OUTPUTS (V_{OS}) - CDIP, PDIP, SOIC and SOP Packages									
	V_{IS} (V)	**V_{EE} (V)**	**V_{SS} (V)**	**V_{DD} (V)**	**TEMP**				
Quiescent Device Current, I_{DD} (Max)		0 V	0 V	5 V	–55°C			5	μA
					–40°C			5	
					25°C		0.04	5	
					85°C			150	
					125°C			150	
		0 V	0 V	10 V	–55°C			10	
					–40°C			10	
					25°C		0.04	10	
					85°C			300	
					125°C			300	
		0 V	0 V	15 V	–55°C			20	
					–40°C			20	
					25°C		0.04	20	
					85°C			600	
					125°C			600	
		0 V	0 V	20 V	–55°C			100	
					–40°C			100	
					25°C		18	100	
					85°C			3000	
					125°C			3000	
Drain to Source ON Resistance r_{ON} (Max) $0 \le V_{IS} \le V_{DD}$		0 V	0 V	5 V	–55°C			800	Ω
					–40°C			850	
					25°C		470	1050	
					85°C			1200	
					125°C			1300	
		0 V	0 V	10 V	–55°C			310	
					–40°C			300	
					25°C		180	400	
					85°C			520	
					125°C			550	
		0 V	0	15 V	–55°C			200	
					–40°C			210	
					25°C		125	240	
					85°C			300	
					125°C			300	
Change in ON Resistance (Between Any Two Channels), ΔR_{ON}		0 V	0 V	5 V	25°C		15		Ω
		0 V	0 V	10 V			10		
		0 V	0 V	15 V			5		

Over operating free-air temperature range, V_{SUPPLY} = ±5 V, and R_L = 100 Ω, (unless otherwise noted) (1)

PARAMETER			TEST CONDITIONS					MIN	TYP	MAX	UNIT
OFF Channel Leakage Current: Any Channel OFF (Max) or ALL Channels OFF (COMMON OUT/IN) (Max)				0 V	0 V	18 V	–55°C			± 100	nA
							–40°C				
							25°C		± 0.3	± 100 (2)	
							85°C			± 1000 (2)	
							125°C				
ON Channel Leakage Current: Any Channel ON (Max) or ALL Channels ON (COMMON OUT/IN) (Max)			5 or 0	–5 V	0 V	10.5 V	85°C			± 800	nA
			5	0 V	0 V	18 V	85°C			± 800	
Capacitance	Input, C_{IS}			0 V	0 V	10 V	25°C		5		pF
	Output, C_{OS}	CD4053-Q1							9		
	Feed through, C_{IOS}								0.2		
Prop Delay			V_{DD}	R_L = 200 kΩ		5 V	25°C		30	60	ns
				C_L = 50 pF		10 V			15	30	
				t_r, t_f = 20 ns		15 V			10	20	

Over operating free-air temperature range, V_{SUPPLY} = ±5 V, and R_L = 100 Ω, (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS					MIN	TYP	MAX	UNIT
CONTROL (ADDRESS OR INHIBIT), V_C - CDIP, PDIP, SOIC and SOP Packages										
Input Low Voltage, V_{IL}, (Max)					5 V	–55°C		1.5		V
						–40°C		1.5		
						25°C			1.5	
						85°C		1.5		
						125°C		1.5		
					10 V	–55°C		3		
						–40°C		3		
						25°C			3	
						85°C		3		
						125°C		3		
					15 V	–55°C		4		
						–40°C		4		
						25°C			4	
						85°C		4		
						125°C		4		
Input High Voltage, V_{IH}, (Min)					5 V	–55°C		3.5		V
						–40°C		3.5		
						25°C	3.5			
						85°C		3.5		
						125°C		3.5		
					10 V	–55°C		7		
						–40°C		7		
						25°C	7			
						85°C		7		
						125°C		7		
					15 V	–55°C		11		
						–40°C		11		
						25°C	11			
						85°C		11		
						125°C		11		
Input current, I_{IN} (Max)		V_{IN} = 0, 18			18 V	–55°C		± 0.1		µA
						–40°C		± 0.1		
						25°C		$±10^{-5}$	± 0.1	
						85°C		± 1		
						125°C		± 1		
Propagation Delay Time	Address-to-Signal OUT (Channels ON or OFF) (See Figure 10, Figure 11, and Figure 15)	t_r , t_f = 20ns, C_L = 50 pF, R_L = 10 kΩ	0 V	0 V	5 V			450	720	ns
			0 V	0 V	10 V			160	320	
			0 V	0 V	15 V			120	240	
			–5 V	0 V	5 V			225	450	
Propagation Delay Time	Inhibit-to-Signal OUT (Channel Turning ON) (See Figure 11)	t_r , t_f = 20 ns, C_L = 50 pF, R_L = 1 kΩ	0 V	0 V	5 V			400	720	ns
			0 V	0 V	10 V			160	320	
			0 V	0 V	15 V			120	240	
			–10 V	0 V	5 V			200	400	

Over operating free-air temperature range, V_{SUPPLY} = ±5 V, and R_L = 100 Ω, (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS					MIN	TYP	MAX	UNIT
Propagation Delay Time	Inhibit-to-Signal OUT (Channel Turning OFF) (See Figure 17)	t_r , t_f = 20 ns, C_L = 50 pF, R_L = 10 kΩ	0 V	0 V	5 V			200	450	ns
			0 V	0 V	10 V			90	210	
			0 V	0 V	15 V			90	160	
			–10 V	0 V	5 V			130	300	
Input Capacitance, C_{IN} (Any Address or Inhibit Input)			–5 V	0 V	5 V	25°C		5	7.5	pF

(1) Peak-to-Peak voltage symmetrical about (V_{DD} – V_{EE}) / 2.
(2) Determined by minimum feasible leakage measurement for automatic testing.

5.6 AC Performance Characteristics - CD4053B-Q1

V_{DD} = +15 V, V_{SS} = V_{EE} = 0 V,
T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS					TYP	UNIT
	V_{IS} (V)	**V_{DD} (V)**	**R_L (kΩ)**				
Cutoff (–3dB) Frequency Channel ON (Sine Wave Input)	5(1)	10	1	V_{OS} at Common OUT/IN	CD4053-Q1	30	MHz
	V_{EE} = V_{SS} , 20Log(V_{OS}/V_{IS}) = –3 dB			V_{OS} at Any Channel		60	MHz
Total Harmonic Distortion, THD	2(1)	5	10			0.3%	%
	3(1)	10	10			0.2%	%
	5(1)	15	10			0.12%	%
	V_{EE} = V_{SS}, f_{IS} = 1 kHz Sine Wave						%
–40dB Feedthrough Frequency (All Channels OFF)	5(1)	10	1	V_{OS} at Common OUT/IN	CD4053-Q1	8	MHz
	V_{EE} = V_{SS} , 20Log(V_{OS}/V_{IS}) = –40 dB			V_{OS} at Any Channel		8	MHz
–40dB Signal Crosstalk Frequency	5(1)	10	1			3	MHz
	V_{EE} = V_{SS} , 20Log(V_{OS}/V_{IS}) = –3 dB			Between Any Two Sections, CD4053-Q1 Only	In Pin 2, Out Pin 14	2.5	MHz
					In Pin 15, Out Pin 14	6	MHz
Address-or-Inhibit-to-Signal Crosstalk		10	10(2)			65	mV_{PEAK}
	V_{EE} = 0, V_{SS} = 0, t_r , t_f = 20 ns, mVPEAK V_{CC} = V_{DD} – V_{SS} (Square Wave)					65	mV_{PEAK}

(1) Peak-to-Peak voltage symmetrical about (V_{DD} - V_{EE}) / 2.
(2) Both ends of channel.

5.7 Typical Characteristics

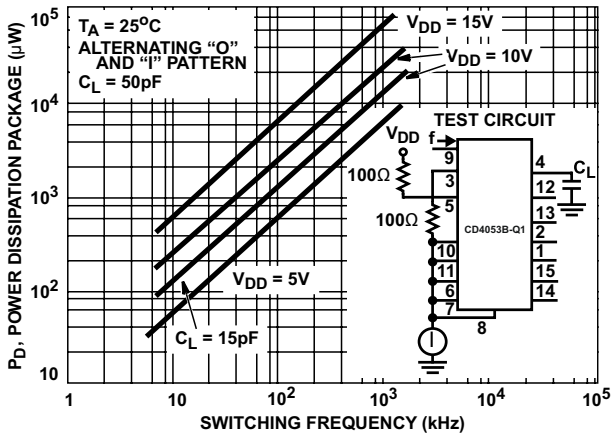


Figure 5-1. Dynamic Power Dissipation vs Switching Frequency (CD4053B-Q1)

6 Parameter Measurement Information

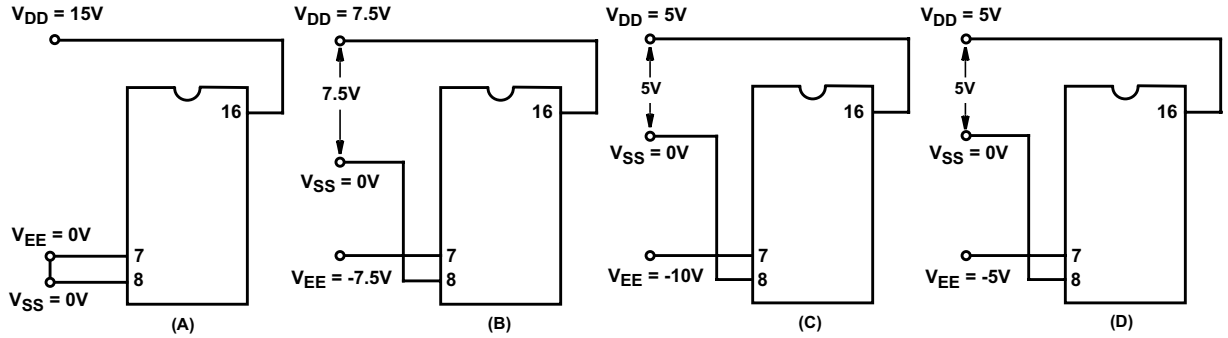


Figure 6-1. Typical Bias Voltages

Note

The ADDRESS (digital-control inputs) and INHIBIT logic levels are: 0 = V_{SS} and 1 = V_{DD}. The analog signal (through the TG) may swing from V_{EE} to V_{DD}.

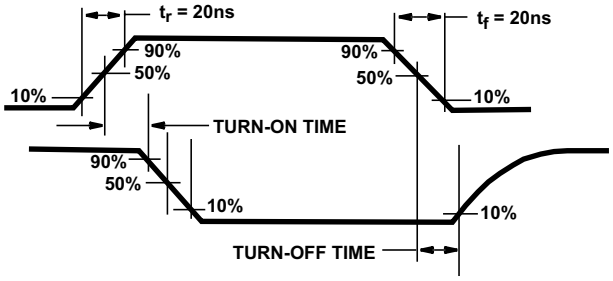


Figure 6-2. Waveforms, Channel Being Turned ON (R_L = 1kΩ)

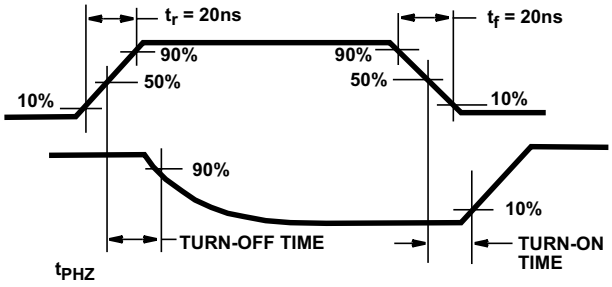


Figure 6-3. Waveforms, Channel Being Turned OFF (R_L = 1kΩ)

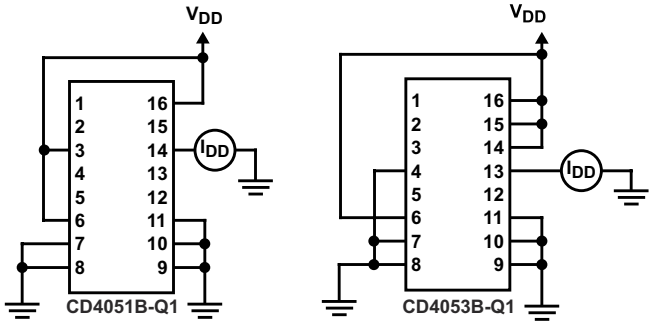


Figure 6-4. OFF Channel Leakage Current – Any Channel OFF

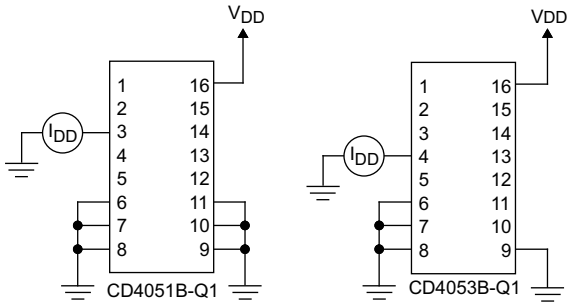


Figure 6-5. On Channel Leakage Current – Any Channel On

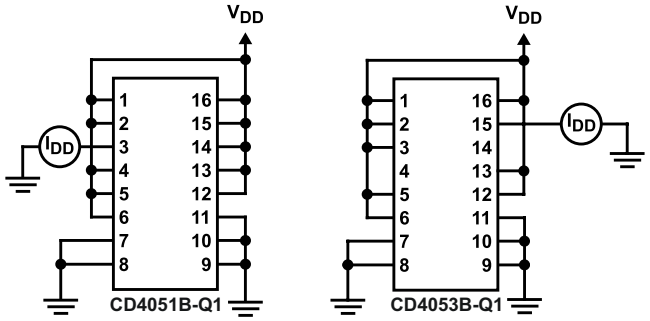


Figure 6-6. OFF Channel Leakage Current – All Channels OFF

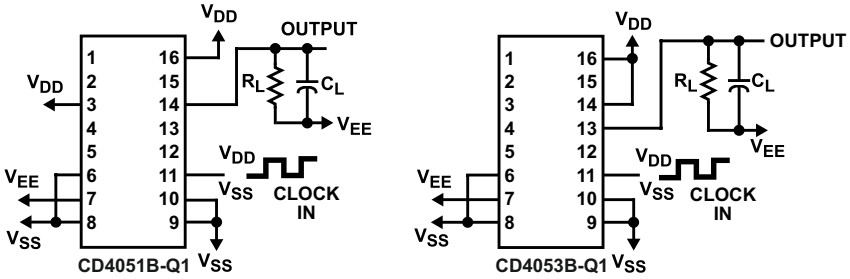


Figure 6-7. Propagation Delay – Address Input to Signal Output

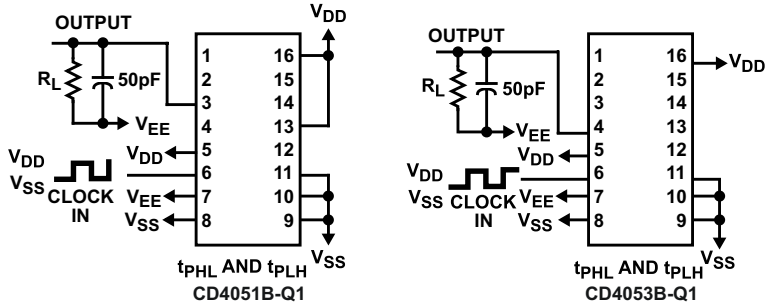


Figure 6-8. Propagation Delay – Inhibit Input to Signal Output

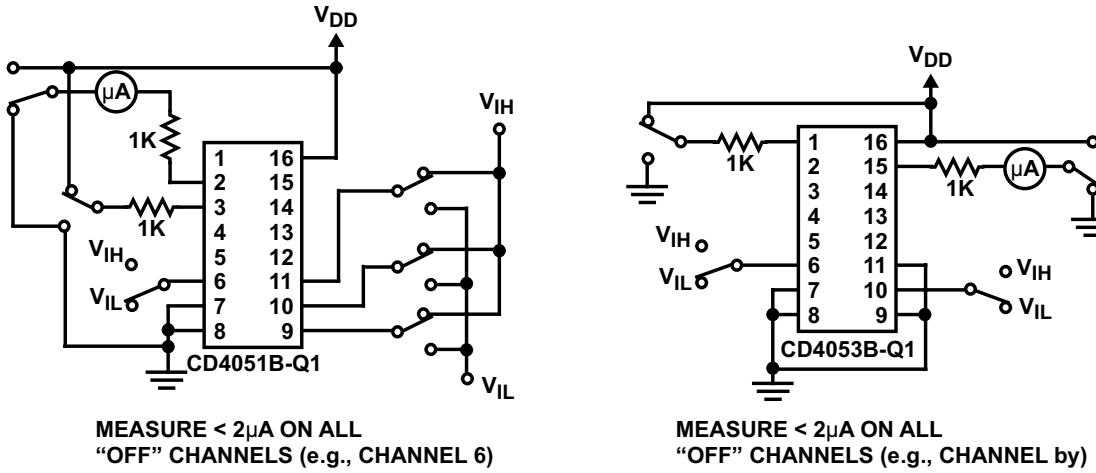


Figure 6-9. Input Voltage Test Circuits (Noise Immunity)

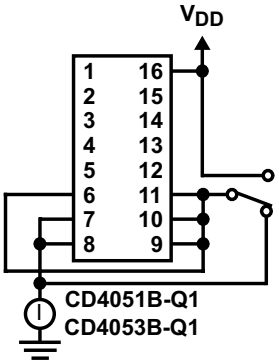


Figure 6-10. Quiescent Device Current

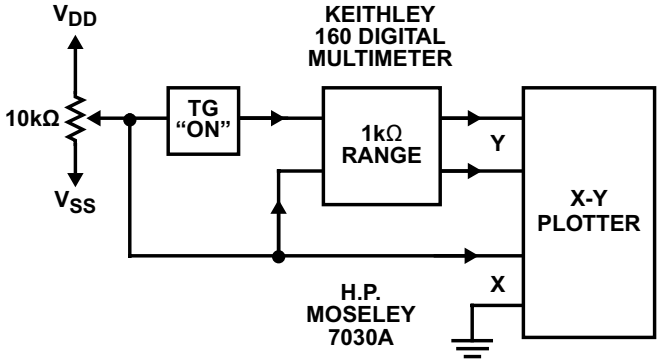
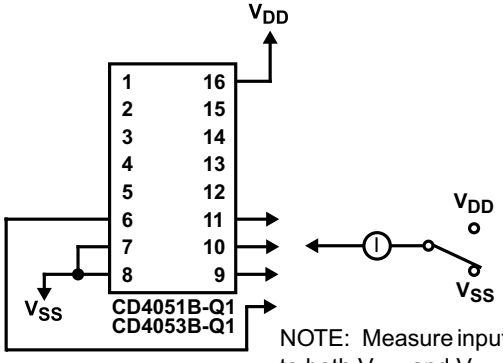


Figure 6-11. Channel ON Resistance Measurement Circuit



NOTE: Measure inputs sequentially, to both V_{DD} and V_{SS} connect all unused inputs to either V_{DD} or V_{SS}.

Figure 6-12. Input Current

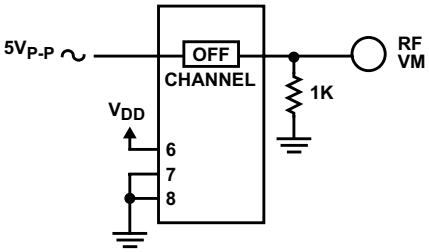


Figure 6-13. Feed-Through (All Types)

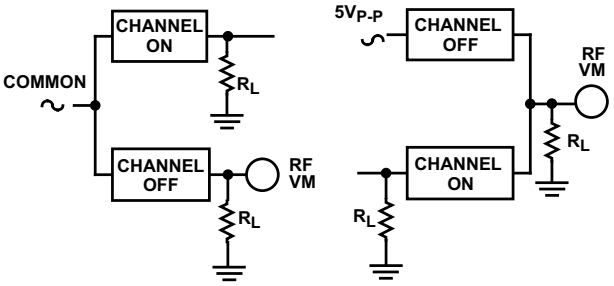


Figure 6-14. Crosstalk Between Any Two Channels (All Types)

Figure 6-15. Crosstalk Between Duals or Triplets

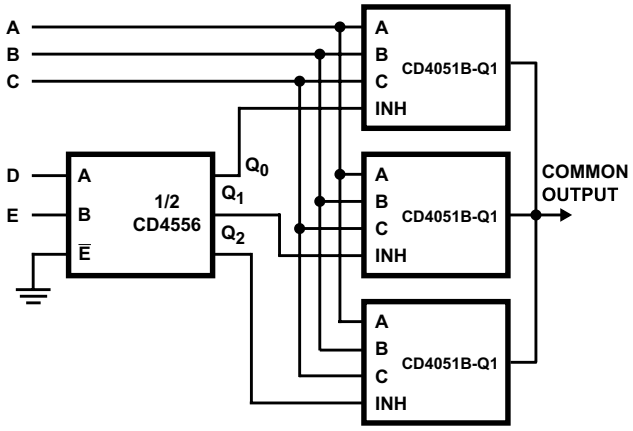


Figure 6-16. 24-to-1MUX Addressing

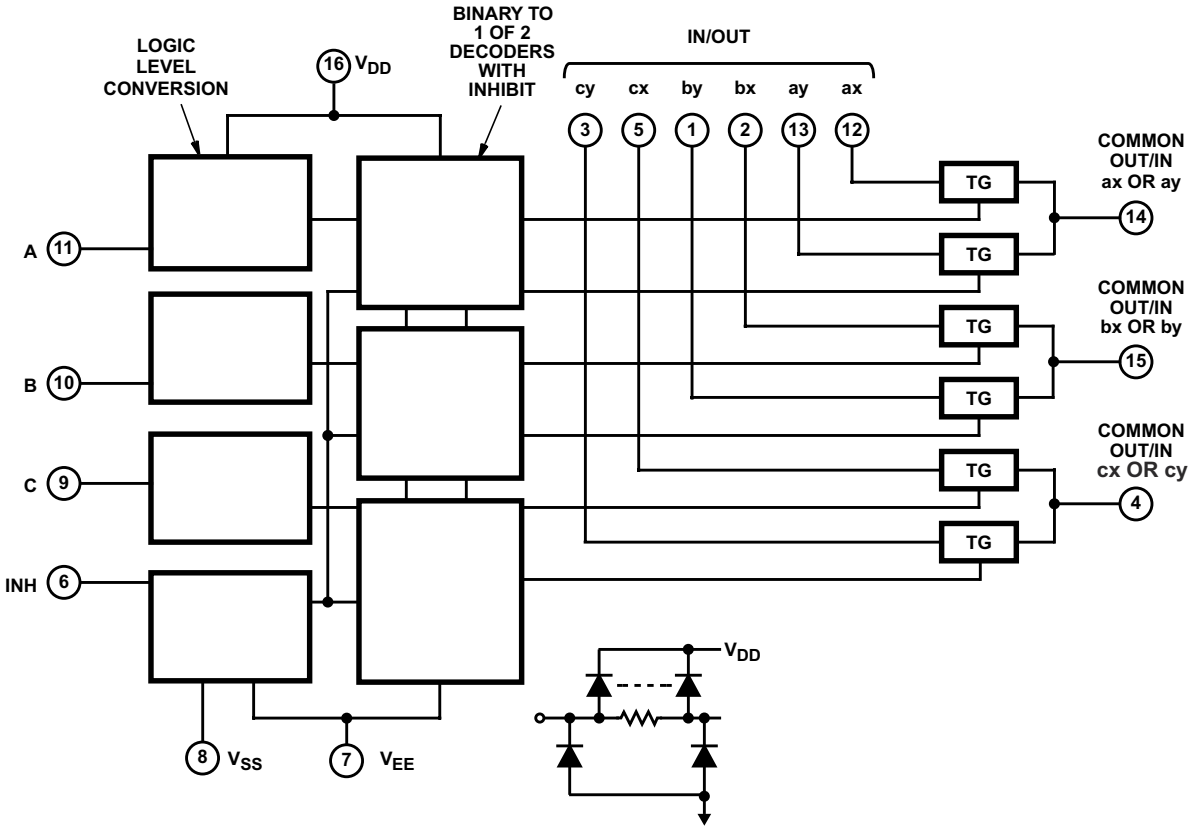
7 Detailed Description

7.1 Overview

The CD4053B-Q1 device is a single 8-channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

When this device is used as a demultiplexer, the CHANNEL IN/OUT terminals are the outputs and the COMMON OUT/IN terminals are the inputs.

7.2 Functional Block Diagrams



All inputs are protected by standard CMOS protection network.

Figure 7-1. Functional Block Diagram, CD4053B-Q1

7.3 Feature Description

The CD4053B-Q1 line of multiplexers and demultiplexers can accept a wide range of digital and analog signal levels. Digital signals range from 3V to 20V, and analog signals are accepted at levels ≤ 20V. The devices have low ON resistance, typically 125Ω over $15V_{P-P}$ signal input range for $V_{DD} – V_{EE}$ = 18V. This feature allows for very little signal loss through the switch.

The CD4053B-Q1 devices also have high OFF resistance, which keeps from the devices from wasting power when the switch is in the OFF position, with typical channel leakage of ±100pA at $V_{DD} – V_{EE}$ = 18V.

Binary address decoding on the chip makes channel selection simple. When channels are changed, a break-before-make system eliminates channel overlap.

7.4 Device Functional Modes

Table 7-1. Truth Table

INPUT STATES (1)				ON CHANNEL(S)
INHIBIT	C	B	A	
CD4053B-Q1				
0	X	X	0	ax
0	X	X	1	ay
0	X	0	X	bx
0	X	1	X	by
0	0	X	X	cx
0	1	X	X	cy
1	X	X	X	None

(1) X = Do not care

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The CD4053B-Q1 multiplexers and demultiplexers can be used for a wide variety of applications.

8.2 Typical Application

One application of the CD4053B-Q1 is to use it in conjunction with a microcontroller to poll a keypad. Figure 8-1 shows the basic schematic for such a polling system. The microcontroller uses the channel select pins to cycle through the different channels while reading the input to see if a user is pressing any of the keys. This application is a very robust setup, allowing for multiple simultaneous key-presses with very little power consumption. This setup also uses very few pins on the microcontroller. The down side of polling is that the microcontroller must continually scan the keys for a press and can do little else during this process.

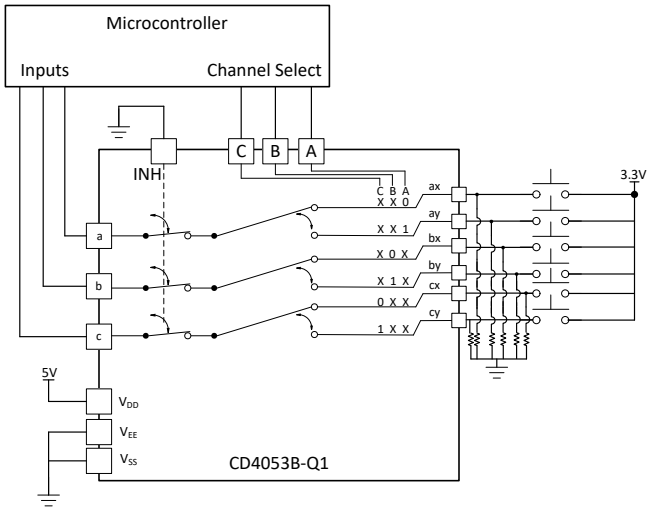


Figure 8-1. The CD4053B-Q1 Being Used to Help Read Button Presses on a Keypad

8.2.1 Design Requirements

These devices use CMOS technology and have balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For switch time specifications, see propagation delay times in Section 5.5.
   - Inputs should not be pushed more than 0.5V above V_{DD} or below V_{EE}.
   - For input voltage level specifications for control inputs, see V_{IH} and V_{IL} in Section 5.5.
2. Recommended Output Conditions:
   - Outputs should not be pulled above V_{DD} or below V_{EE}.
3. Input or output current consideration:
   - The CD405xB-Q1 series of parts do not have internal current drive circuitry and thus cannot sink or source current. Any current will be passed through the device.

8.2.3 Application Curve

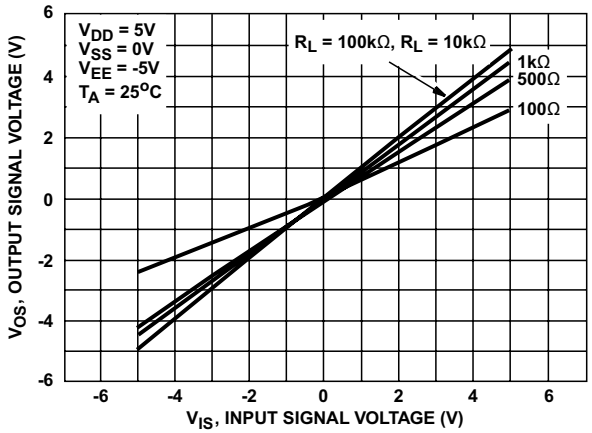


Figure 8-2. ON Characteristics for 1 of 8 Channels

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the Section 5.5.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1µF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01µF or 0.022µF capacitor is recommended for each V_{CC} because the V_{CC} pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1µF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This reflection is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. Figure 8-3 shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

8.4.2 Layout Example

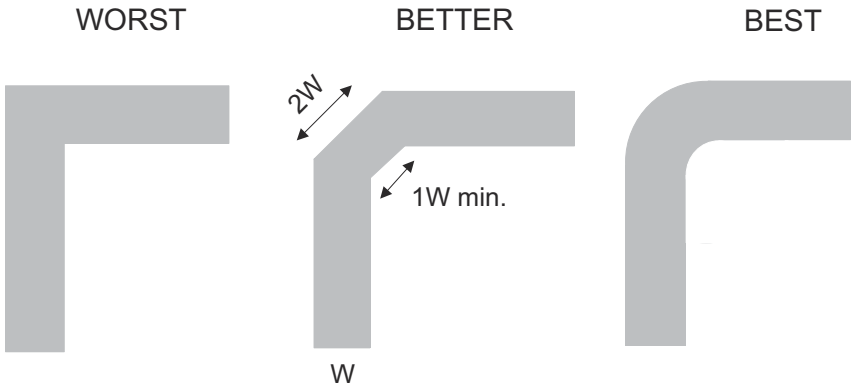


Figure 8-3. Trace Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD4053BQM96G4Q1	NRND	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CD4053Q
CD4053BQM96G4Q1.A	NRND	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CD4053Q
CD4053BQM96Q1	NRND	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CD4053Q
CD4053BQM96Q1.A	NRND	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CD4053Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

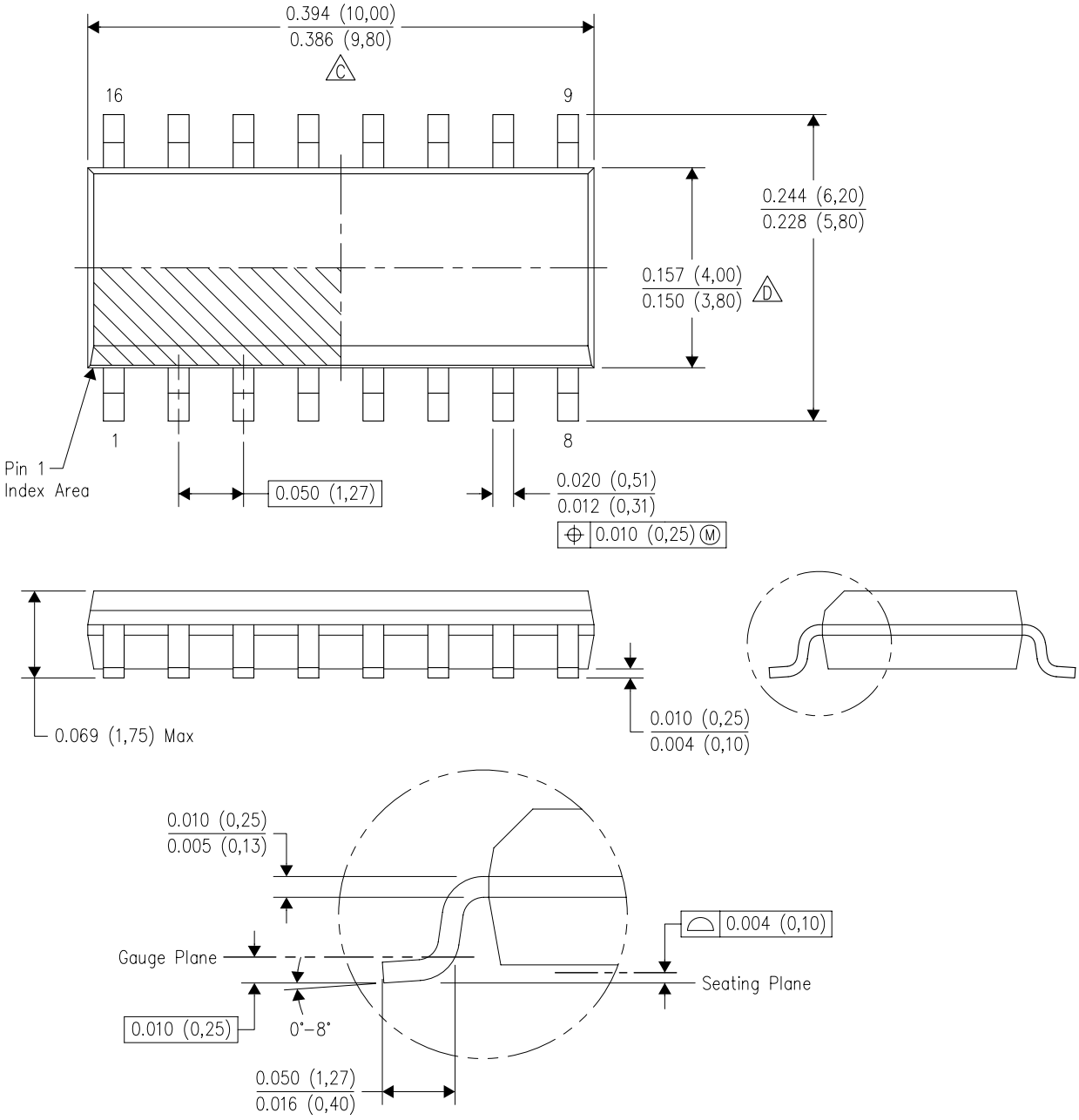
OTHER QUALIFIED VERSIONS OF CD4053B-Q1 :

- Catalog : CD4053B
- Military : CD4053B-MIL

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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