

Data sheet acquired from Harris Semiconductor SCHS036B – Revised July 2003

CMOS 64-Stage Static Shift Register

High-Voltage Types (20-Volt Rating)

■ CD4031B is a static shift register that contains 64 D-type, master-slave flip-flop stages and one stage which is a D-type master flip-flop only (referred to as a 1/2 stage).

The logic level present at the DATA input is transferred into the first stage and shifted one stage at each positive-going clock transition. Maximum clock frequencies up to 12 Megahertz (typical) can be obtained. Because fully static operation is allowed, information can be permanently stored with the clock line in either the low or high state. The CD4031B has a MODE CONTROL input that, when in the high state, allows operation in the recirculating mode. The MODE CON-TROL input can also be used to select between two separate data sources. Register packages can be cascaded and the clock lines driven directly for high-speed operation. Alternatively, a delayed clock output (CLD) is provided that enables cascading register packages while allowing reduced clock drive fan-out and transition-time requirements. A third cascading option makes use of the Q' output from the 1/2 stage, which is available on the next negative-going transition of the clock after the Q output occurs. This delayed output, like the delayed clock CLD, is used with clocks having slow rise and fall times.

The CD4031B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

- Fully static operation: DC to 12 MHz typ. @ V_{DD}-V_{SS} = 15 V
- Standard TTL drive capability on Q output
- Recirculation capability
- Three cascading modes:

Direct clocking for high-speed operation
Delayed clocking for reduced clock drive requirements
Additional 1/2 stage for slow clocks

- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range)

1 V at V_{DD} = 5 V 2 V at V_{DD} = 10 V 2.5 V at V_{DD} = 15 V

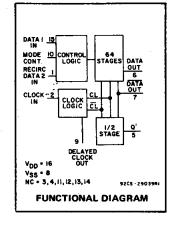
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 138, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Serial shift registers
- Time delay circuits

RECOMMENDED OPERATING CONDITIONS For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

	LIN		
CHARACTERISTIC	Min.	Max.	UNITS
Supply-Voltage Range (For TA=Full Package- Temperature Range)	3	18	٧



INPUT CONTROL CIRCUIT TRUTH TABLE

CD4031B Types

DATA	RECIRC.	MODE	BIT INTO STAGE I
1	X	0	1
0	X	0	0
X	1	1	1
X	0	1	0

TYPICAL STAGE TRUTH TABLE

Deta	CL	Data + 1
0		0
1		1
X		NC

TRUTH TABLE FOR OUTPUT FROM Q' (TERMINAL 5)

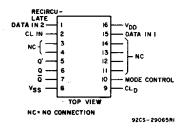
Data + 64	CL	Data + 641/2
0	7	0
1	7	1
X		NC

1 = HIGH LEVEL

0 = LOW LEVEL

X = DON'T CARE

NC = NO CHANGE



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, Absolute-Maximum Values:

STATIC F	LECTRICAL	CHARACTERISTICS

AU	COND	ITION:	S	LIMIT	S AT II	NDICAT	ED TEN	IPERAT	URES (oc)	UNITS
CHARACTERISTIC	Vo	VIN	v_{DD}						+25		
	(V)	(V)	(V)	_ <u>5</u> 5	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device	_	0,5	5	5	5	150	150	_	0.04	5	
Current,	'	0,10	10	10	10	300	300	_	0.04	10	μΑ
IDD Max.		0,15	15	20	20	600	600	- /	0.04	20	
		0,20	20	100	100	3000	3000		0.08	100	
Output Low (Sink)	0.4	0,5	5	2.56	2.44	1.68	1.44	2.04	4	-	
Current IOL Min.	0.5	0,10	10	6.4	6	4.4	3.6	5.2	10.4	-	
u	1.5	0,15	15	16.8	16	11.2	9.6	13.6	27.2	_	
	0.4	0,5	5	0.64	0:61	0.42	0.36	0.51	1	_	1
α, α, crb	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	ł
_	1.5	0,15	15	4.2	4 ·	2.8	2.4	3.4	6.8	-	mA.
Output High (Source)	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	1 .
Current, IOH Min.	2.5	0,5	5	- 2	1.8	1.3	-1.15	-1.6	-3.2.		1
Q, Q, Q', CLD	9.5	0,10	10	-1.6	1.5	-1.1	-0.9	-1.3	-2.6	-	1
	13.5	0,15	15	- 4.2	4	2.8	-2,4	-3.4	-6.8	-	1
Output Voltage:	-	0,5	5			0.05		_	0	0.05	
Low Level.	×:	0,10	10	· ;		0.05		-	0	0.05	1
VOL Max.		0,15	15			0.05		_	. 0	0.05	l v
Output Voltage:	-	0,5				4.95		4.95	5		l '
High Level,	·	0,10				9.95		9.95	10	_	
V _{OH} Min,		0,15				14.95		14.95	15		<u> </u>
Input Low	0.5, 4.5	-	5			1.5		-		1.5	
Voltage	1,9	-	10			3				3	,
V _{IL} Max.	1.5, 13.5	-	15			4				4	V
Input High	0.5, 4.5		5			3.5		3.5	<u> </u>		•
Voltage,	1;9	-	10	ļ		7		7	├ <u>¯</u>		l
V _{IH} Min.	1.5, 13.5		15	ļ		11		11		_	<u> </u>
Input Current I _{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	_	±10-5	±0.1	μΑ

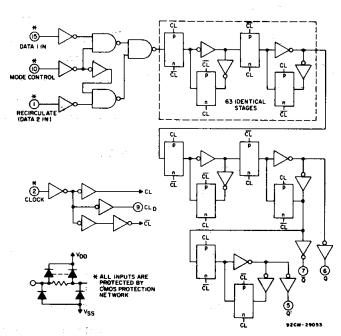


Fig. 1 — Logic diagram.

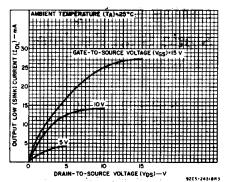


Fig. 2 — Typical output low (sink)

current characteristics (Q sink

current = 4X ordinate).

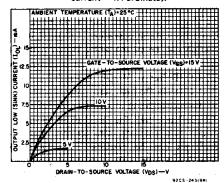


Fig. 3 — Minimum output low (sink)
current characteristics (Q sink
current = 4X ordinate).

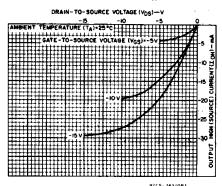


Fig. 4 — Typical output high (source) current characteristics.

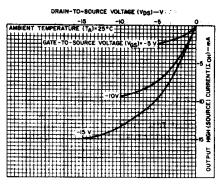


Fig. 5 — Minimum output high (source) current characteristics.

CD4031B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r , t_f = 20 ns, C_L = 50 pF, R_L = 200 k Ω

CHARACTERISTIC	TEST CONDITIONS		LIMIT	S	
CHARACTERISTIC	V _{DD} (V)	Min.	Тур.	Max.	UNITS
Propagation Delay Time:	5	_	250	500	
Clock to Q, tpHL, tpLH;	10	-	110	220	ns
Clock to Q, tPLH	15	_	90	180	
Clock to Q', tpHL, tpLH;	5	-	190	380	``
Clock to Q, tpHL	10	_	80	160	ns
	15		65	130	
,	5	_	100	200	
Clock to CL _D	10		50	100	ns
	15		40	80	
Transition Time t	5		100	200	
Transition Time, t _{THL} , t _{TLH}	10	_	50	100	ns
(Any Output, except Q, t _{THL})	15	_	40	80	
	5	_	50	100	
Q, t _{THL}	10	_	25	50	ns
	15		20	40	
	5	_	30	60	
Minimum Data Setup Time, tS	10	_	15	30	ns ns
	15	-	10	20	
	5	_	30	60	
Minimum Data Hold Time, tH	10	_	15	30	กร
<u>-</u>	15	-	10	20	
	5	_	120	240	
Minimum Clock Pulse Width, tw	10	_	50	100	ns
	15	-	40	80	
Maximum Clark Innut Fre	5	2	4	_	
Maximum Clock Input Frequency,	10	5	10	. —	MHz
fcL**	. 15	6	12	-	
Clock Input Rise or Fall Time,	5	_		1000	
	10		_	1000	μs
trCL/tfCL*	15			200	· ·
Input Capacitance, C _{IN} (Any Input)		_	5	7.5	pF

^{*}If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the propagation delay at 50 pF and the transition time of the output driving stage. **Maximum Clock Frequency for Cascaded Units;



 $f_{\text{max}} = \frac{1}{\text{(n-1) CL}_D \text{ prop. delay + Q prop. delay + set-up time}}$ where n = number of packages

b) Not Using Delayed Clock:

fmax = propagation delay + set-up time

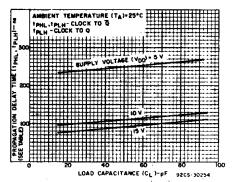


Fig. 6 — Typical propagation delay time as a function of load capacitance (see table).

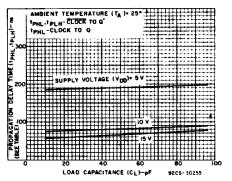


Fig. 7 — Typical propagation delay time as a function of load capacitance (see table).

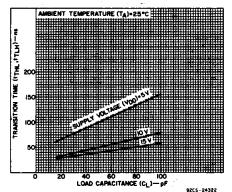


Fig. 8 — Typical transition time as a function of load capacitance (except Q, t_{THL}).

CD4031B Types

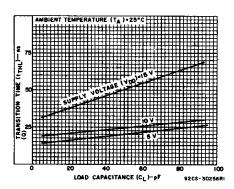


Fig. 9 — Typical transition time as a function of load capacitance (Q, t_{THL}).

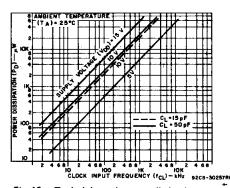


Fig. 10 — Typical dynamic power dissipation as a function of clock input frequency.

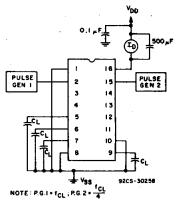


Fig. 11 - Dynamic power dissipation test circuit.

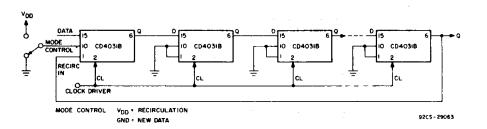


Fig. 12 — Cascading using direct clocking for high-speed operation (see clock rise and fall time requirement).

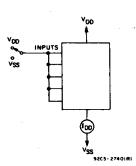


Fig. 13 — Quiescent-devicecurrent test circuit.

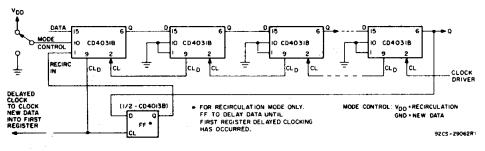


Fig. 14 - Cascading using delayed clocking for reduced clock drive requirements.

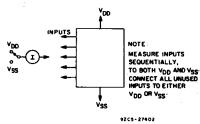


Fig. 15 - Input-leakage current.

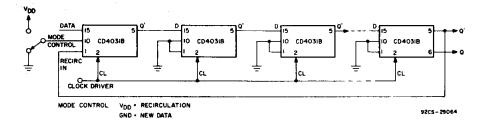


Fig. 16 — Cascading using half-clock-pulse delayed data output (Q^\prime) to permit use of slow rise and fall time clock inputs.

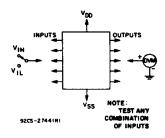
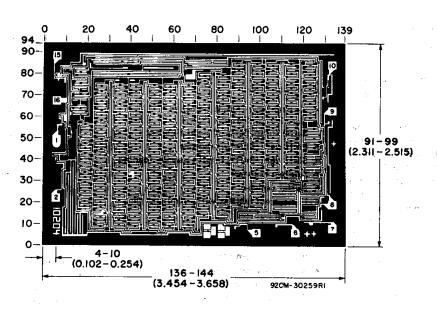


Fig. 17 - Input-voltage test circuit.



Chip dimensions and ped layout for CD4031B

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10⁻³ inch).

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
CD4031BE	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4031BE
CD4031BE.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4031BE
CD4031BF3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4031BF3A
CD4031BF3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4031BF3A
CD4031BPW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-55 to 125	CM031B
CD4031BPWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM031B
CD4031BPWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM031B

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

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OTHER QUALIFIED VERSIONS OF CD4031B, CD4031B-MIL:

• Military : CD4031B-MIL

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

• Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION



TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

	-
A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

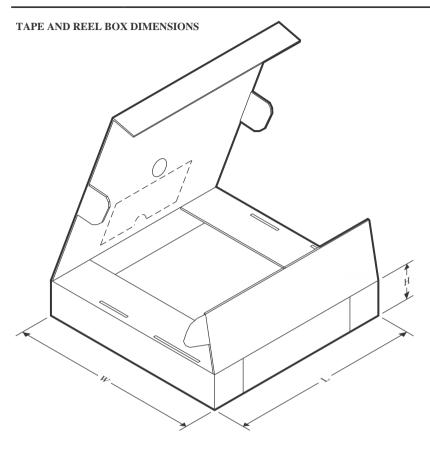


*All dimensions are nominal

	Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	` '	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
١	CD4031BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Ì	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
ı	CD4031BPWR	TSSOP	PW	16	2000	353.0	353.0	32.0	

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD4031BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4031BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4031BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4031BE.A	N	PDIP	16	25	506	13.97	11230	4.32

14 LEADS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



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