

CMOS QUAD LOW-TO-HIGH VOLTAGE SHIFTER

Check for Samples: [CD40109B-Q1](#)

FEATURES

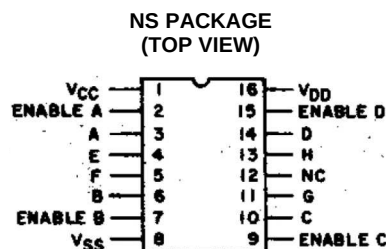
- Qualified for Automotive Applications
- Independent of Power Supply Sequence Considerations
 - V_{CC} Can Exceed V_{DD}
 - Input Signals can Exceed Both V_{CC} and V_{DD}
- Up and Down Level-Shifting Capability
- Three-State Outputs With Separate Enable Controls
- Standardized Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20 V
- Maximum Input Current:
 - 1 μ A at 18 V Over Full Package-Temperature Range
 - 100 nA at 18 V and 25°C
- Noise Margin (Full Package-Temperature Range):
 - 1 V at $V_{CC} = 5$ V, $V_{DD} = 10$ V
 - 2 V at $V_{CC} = 10$ V, $V_{DD} = 15$ V
- 5-V, 10-V, and 15-V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard specifications for

Description of 'B' Series CMOS Devices"

- Latch-Up Performance Meets 50 mA per JESD 78, Class I

APPLICATIONS

- High-or-Low Level-Shifting With Three-State Outputs for Unidirectional or Bidirectional Bussing
- Isolation of Logic Subsystem Using Separate Power Supplies from Supply Sequencing, Supply Loss, and Supply Regulation Considerations



DESCRIPTION

CD40109B contains four low-to-high-voltage level-shifting circuits. Each circuit will shift a low-voltage digital-logic input signal (A, B, C, D) with logical 1 = V_{CC} and logical 0 = V_{SS} to a high-voltage output signal (E, F, G, H) with logical 1 = V_{DD} and logical 0 = V_{SS} .

The RCA-CD40109, unlike other low-to-high level-shifting circuits, does not require the presence of the high-voltage supply (V_{DD}) before the application of either the low-voltage supply (V_{CC}) or the input signals. There are no restrictions on the sequence of application of V_{DD} , V_{CC} , or the input signals. In addition, with one exception there are no restrictions on the relative magnitudes of the supply voltages or input signals within the device maximum ratings, provided that the input signal swings between V_{SS} and at least 0.7 V_{CC} ; V_{CC} may exceed V_{DD} , and input signals may exceed V_{CC} and V_{DD} . When operated in the mode $V_{CC} > V_{DD}$, the CD40109 will operate as a high-to-low level-shifter.

The CD40109 also features individual three-state output capability. A low level on any of the separately enabled three-state output controls produces a high-impedance state in the corresponding output.

ORDERING INFORMATION⁽¹⁾

T_A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – NS	Reel of 2000	CD40109BQNSRQ1	CD40109BQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



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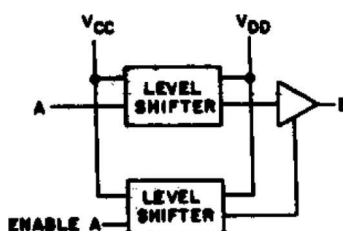
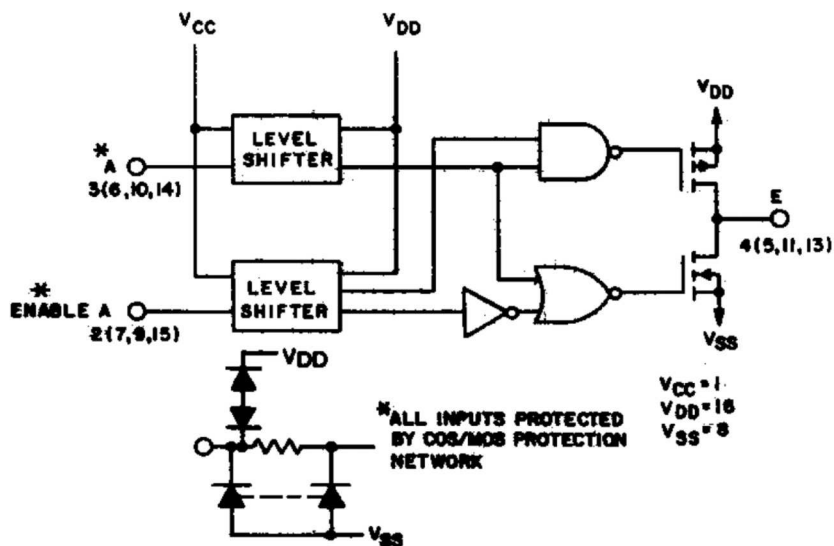
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

TRUTH TABLE⁽¹⁾

INPUTS		OUTPUTS
A, B, C, D	ENABLE A, B, C, D	E, F, G, H
0	1	0
1	1	1
X	0	Z

(1) 0 = V_{SS} , 1 = V_{CC} at inputs and V_{DD} at outputs, X = Don't care, Z = High impedance

Functional Diagram (1 of 4 Units)**Logic Diagram (1 of 4 Units)**

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
V _{DD}	DC supply voltage range	Voltages referenced to V _{SS} terminal	–0.5 to +20	V
	Output voltage range	All outputs	–0.5 to V _{DD} + 0.5	V
	DC input current	Any one input	±10	mA
P _D	Power dissipation per package	T _A = –40°C to + 100°C	500	mW
		T _A = 100°C to + 125°C	Derate linearly at 12 mW/°C to 200 mW	
	Device dissipation per output transistor (for T _A = full package-temperature range, all package types)		100	mW
T _A	Operating-temperature range		–40 to +125	°C
T _{stg}	Storage temperature range		–65 to +150	°C
	Latch-Up Performance per JESD 78, Class I		50	mA

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

	MIN	MAX	UNIT
V _{DD} Supply-voltage range (for T _A = full package-temperature range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

PARAMETER		CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)						
		V _O (V)	V _{IN} (V)	V _{DD} (V)	−40	+85	+125	+25			UNIT
								MIN	TYP	MAX	
I _{DD} Max	Quiescent device current		0, 5	5	1	30	30	0.02	1	μA	
			0, 10	10	2	60	60	0.02	2		
			0, 15	15	4	120	120	0.02	4		
			0, 20	20	20	600	600	0.04	20		
I _{OL} Min	Output low (sink) current	0.4	0, 5	5	0.61	0.42	0.36	0.51	1	mA	
		0.5	0, 10	10	1.5	1.1	0.9	1.3	2.6		
		1.5	0, 15	15	4	2.8	2.4	3.4	6.8		
I _{OH} Min	Output high (source) current	4.6	0, 5	5	−0.61	−0.42	−0.36	−0.51	−1		
		2.5	0, 5	5	−1.8	−1.3	−1.15	−1.6	−3.2		
		9.5	0, 10	10	−1.5	−1.1	−0.9	−1.3	−2.6		
		13.5	0, 15	15	−4	−2.8	−2.4	−3.4	−6.8		
V _{OL} Max	Output voltage: low-level		0, 5	5	0.05			0	0.05	V	
			0, 10	10	0.05			0	0.05		
			0, 15	15	0.05			0	0.05		
V _{OH} Min	Output voltage: high-level		0, 5	5	4.95			4.95	5		
			0, 10	10	9.95			9.95	10		
			0, 15	15	14.95			14.95	15		
I _{IN} Max	Input current		0, 18	18	±0.1	±1	±1	±10 ^{−5}	±0.1	μA	
I _{OUT} Max			0, 18	18	±0.4	±12	±12	±10 ^{−4}	±0.4	μA	
V _{IL} Max	Input low voltage	1, 9	5	10	1.5			1.5		V	
		1.5, 13.5	10	15	3			3			
V _{IH} Min	Input high voltage	1, 9	5	10	3.5			3.5			
		1.5, 13.5	10	15	7			7			

DYNAMIC ELECTRICAL CHARACTERISTICS
 $T_A = 25^\circ\text{C}$, Input $t_r/t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SHIFTING MODE	V_{CC} (V)	V_{DD} (V)	MIN	MAX	UNIT
t_{PHL} Propagation delay time, high-to-low level, data input to output		L – H	5	10	300	600	ns
			5	15	220	440	
			10	15	180	360	
		H – L	10	5	250	500	
			15	5	250	500	
			15	10	120	240	
t_{PLH} Propagation delay time, low-to-high level, data input to output		L – H	5	10	130	260	ns
			5	15	120	240	
			10	15	70	140	
		H – L	10	5	230	460	
			15	5	230	460	
			15	10	80	160	
t_{PHZ} Propagation delay time, 3-state disable, delay, output high to high impedance	$R_L = 1\text{ k}\Omega$	L – H	5	10	60	120	ns
			5	15	75	150	
			10	15	35	70	
		H – L	10	5	200	400	
			15	5	200	400	
			15	10	40	80	
t_{PLZ} Propagation delay time, 3-state disable, delay, output low to high impedance	$R_L = 1\text{ k}\Omega$	L – H	5	10	370	740	ns
			5	15	300	600	
			10	15	250	500	
		H – L	10	5	250	500	
			15	5	250	500	
			15	10	130	260	
t_{PZH} Propagation delay time, 3-state disable, delay, output high impedance to high	$R_L = 1\text{ k}\Omega$	L – H	5	10	320	640	ns
			5	15	230	460	
			10	15	180	360	
		H – L	10	5	300	600	
			15	5	300	600	
			15	10	130	260	
t_{PZL} Propagation delay time, 3-state disable, delay, output high impedance to low	$R_L = 1\text{ k}\Omega$	L – H	5	10	100	200	ns
			5	15	80	160	
			10	15	40	80	
		H – L	10	5	200	400	
			15	5	200	400	
			15	10	40	80	
t_{THL}, t_{TLH} Transition time		L – H	5	10	50	100	ns
			5	15	40	80	
			10	15	40	80	
		H – L	10	5	100	200	
			15	5	100	200	
			15	10	50	100	
C_i Input capacitance			Any input		5	7.5	pF

TYPICAL CHARACTERISTICS

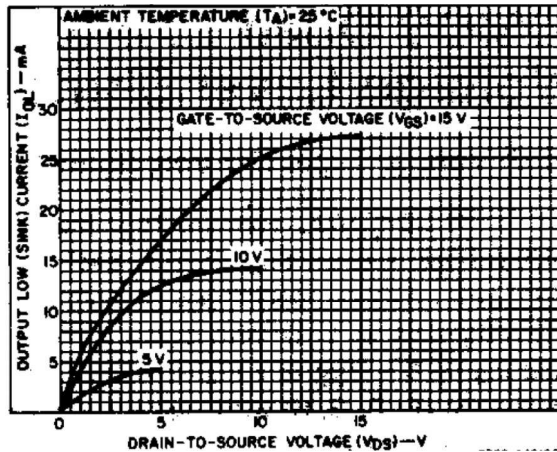


Figure 1. Typical Output Low (Sink) Current Characteristics

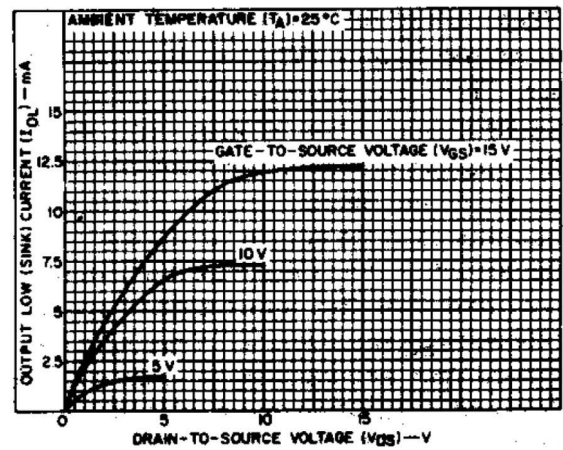


Figure 2. Minimum Output Low (Sink) Current Characteristics

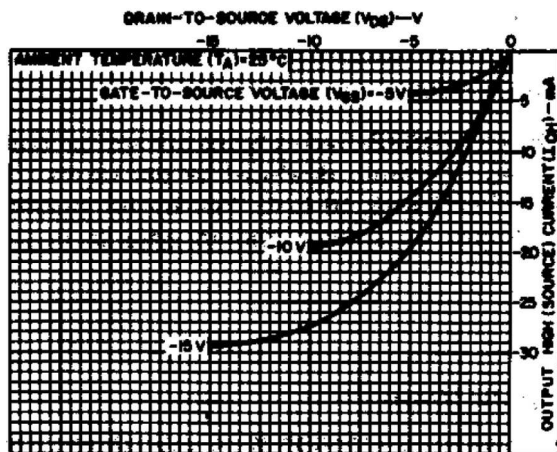


Figure 3. Typical Output High (Source) Current Characteristics

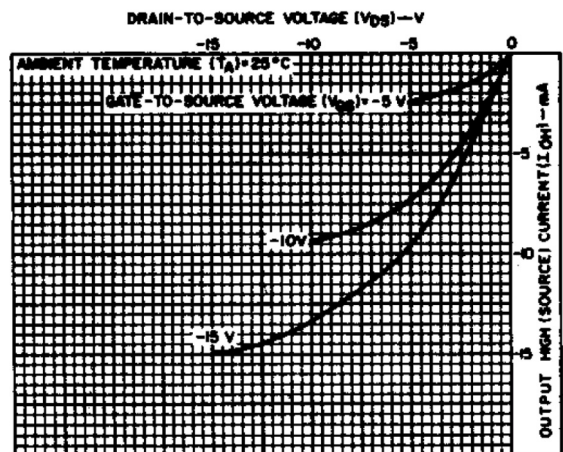


Figure 4. Minimum Output High (Source) Current Characteristics

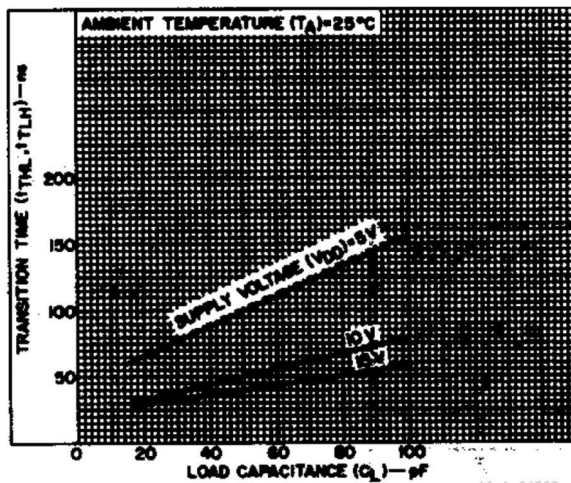


Figure 5. Typical Transition Time as a Function of Load Capacitance

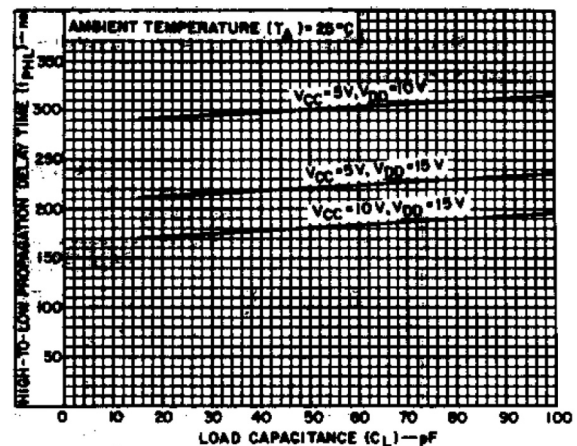


Figure 6. Typical High-to-Low Propagation Delay Time as a Function of Load Capacitance

TYPICAL CHARACTERISTICS (continued)

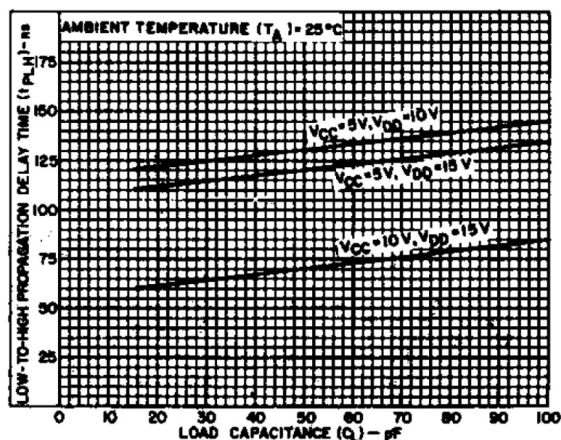


Figure 7. Typical Low-to-High Propagation Delay Time as a Function of Load Capacitance

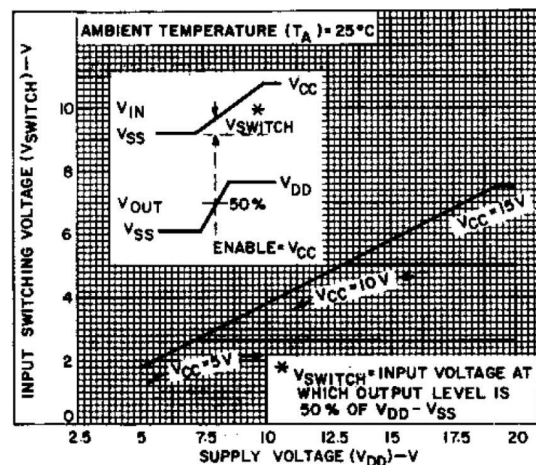


Figure 8. Typical Input Switching as a Function of High-Level Supply Voltage

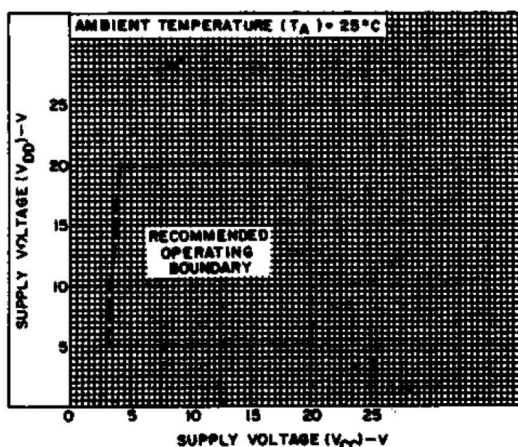


Figure 9. High-Level Supply Voltage vs Low-Level Supply Voltage

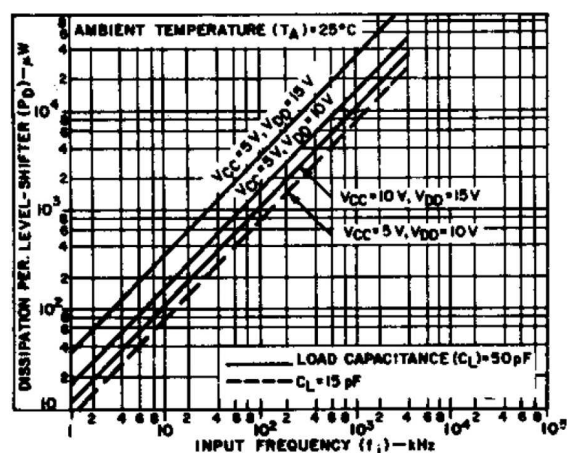


Figure 10. Typical Dynamic Power Dissipation as a Function of Input Frequency

PARAMETER MEASUREMENT INFORMATION

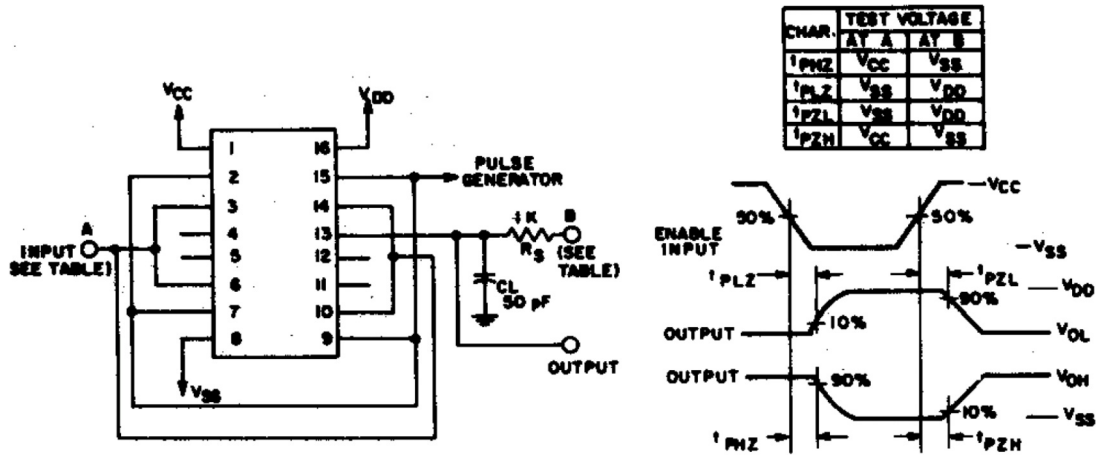


Figure 11. Output Enable Delay Times Test Circuit and Waveforms

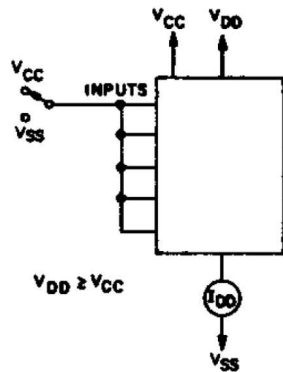


Figure 12. Quiescent Device Current Test Circuit

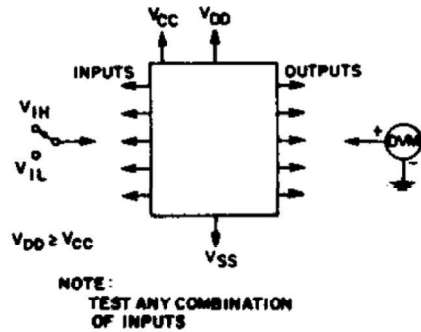


Figure 13. Input Voltage Test Circuit

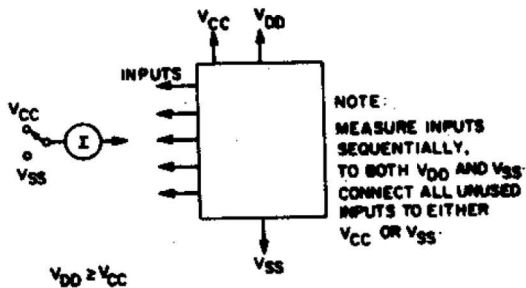


Figure 14. Input Current Test Circuit

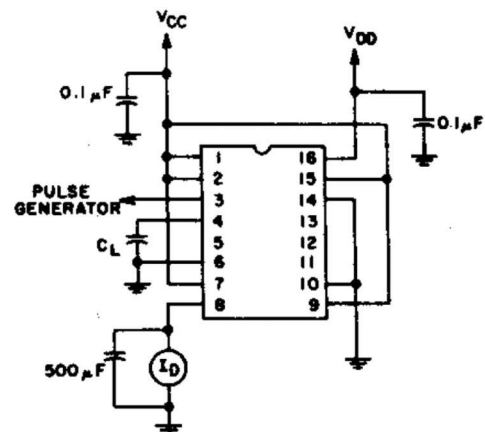
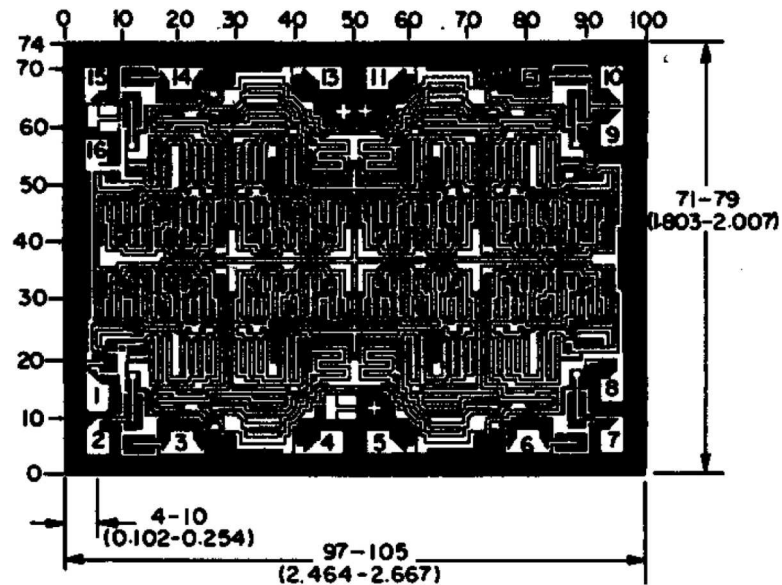


Figure 15. Dynamic Power Dissipation Test Circuit



Note: Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Figure 16. Dimensions and Pad Layout

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD40109BQNSRQ1	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CD40109BQ
CD40109BQNSRQ1.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CD40109BQ

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF CD40109B-Q1 :

- Catalog : [CD40109B](#)

- Military : [CD40109B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

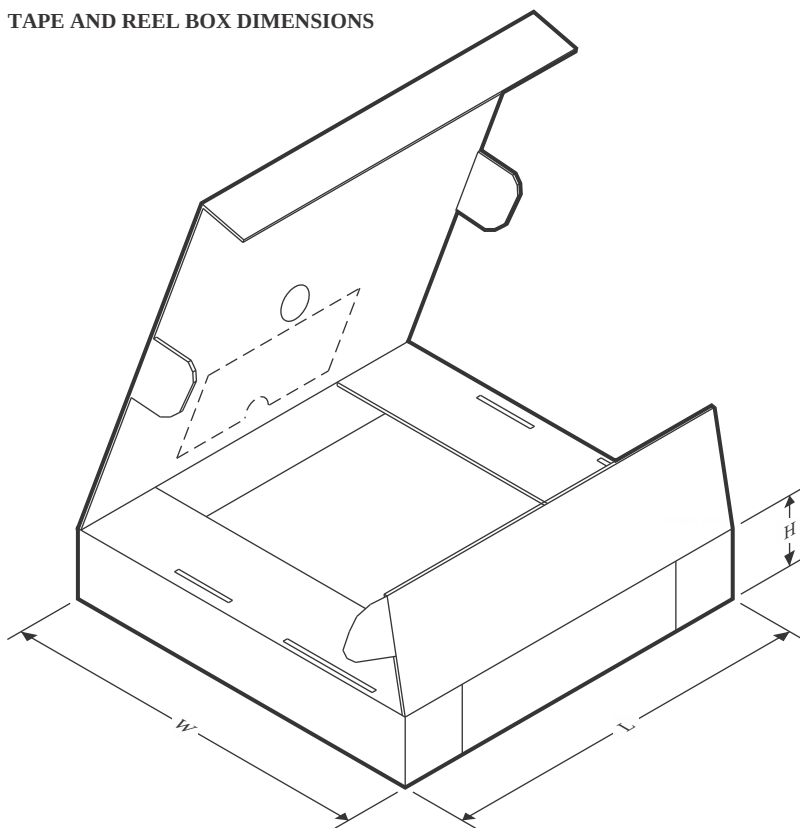
TAPE AND REEL INFORMATION



*All dimensions are nominal

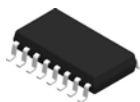
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD40109BQNSRQ1	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD40109BQNSRQ1	SOP	NS	16	2000	353.0	353.0	32.0

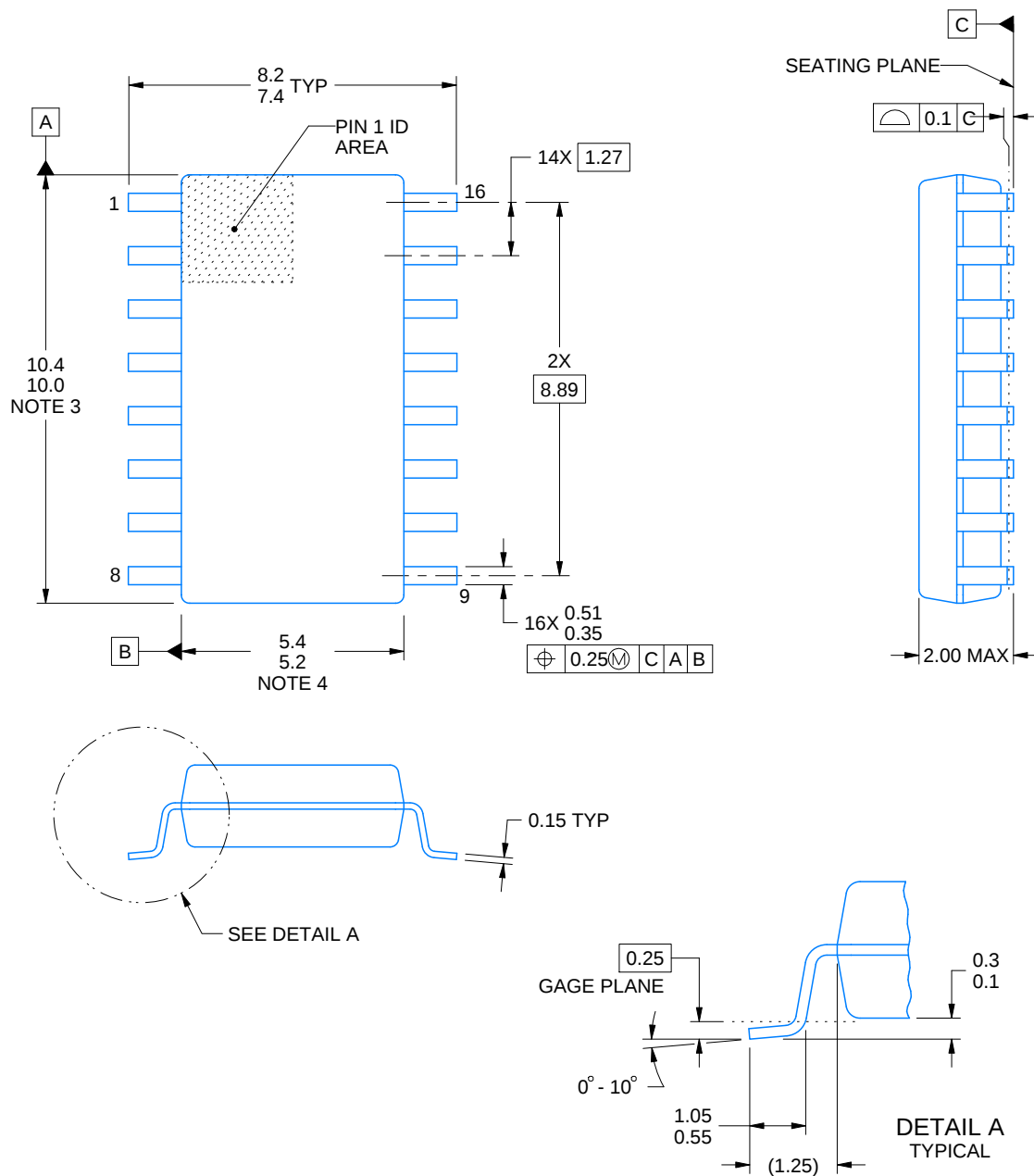


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

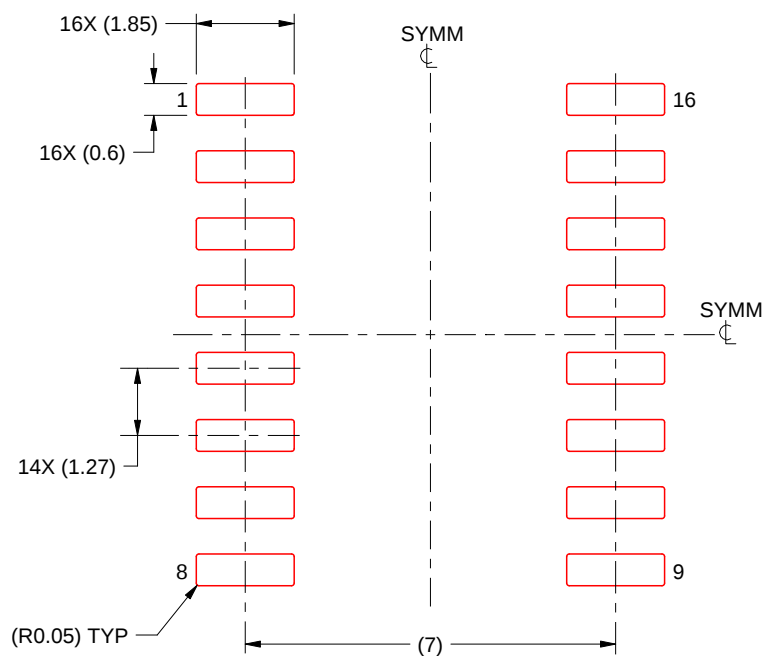
SOP



4220735/A 12/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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