

CC2640R2F-Q1 SimpleLink™ Bluetooth® Low Energy Wireless MCU for Automotive

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
 - Device temperature grade 2: –40°C to +105°C ambient operating temperature range
 - Device HBM ESD Classification Level 2
 - Device CDM ESD Classification Level C3
- Microcontroller
 - Powerful Arm® Cortex®-M3
 - EEMBC CoreMark® Score: 142
 - Up to 48MHz clock speed
 - 275KB nonvolatile memory, including 128KB insystem Programmable Flash
 - Up to 28KB system SRAM, of which 20KB is ultra-low leakage SRAM
 - 8KB SRAM for Cache or system RAM use
 - 2-pin cJTAG and JTAG debugging
 - Supports Over-the-Air (OTA) upgrade
- Ultra-low power sensor controller
 - Can run autonomously from the rest of the system
 - 16-bit architecture
 - 2-KB ultra-low leakage SRAM for code and data
- Efficient code size architecture, placing drivers, Bluetooth Low Energy® Controller, and bootloader in ROM to make more flash available for the application
- RoHS-compliant automotive grade package
 - 7mm × 7mm RGZ VQFN48 with wettable flanks>
- Peripherals
 - 31 GPIOs, all digital peripheral pins can be routed to any GPIO
 - Four general-purpose timer modules (eight 16-bit or four 32-bit timers, PWM each)
 - 12-bit ADC, 200-ksamples/s, 8-channel analog MUX
 - Continuous time comparator
 - Ultra-low power analog comparator
 - Programmable current source
 - UART
 - 2× SSI (SPI, MICROWIRE, TI)
 - I²C, I²S
 - Real-time clock (RTC)
 - AES-128 security module
 - True random number generator (TRNG)
 - Support for eight capacitive-sensing buttons
 - Integrated temperature sensor
- External system
 - On-chip internal DC/DC converter

- Very few external components
- Seamless integration with the SimpleLink™ CC2590 and CC2592 range extenders
- Low power
 - Wide supply voltage range: 1.8V to 3.8V
 - Active mode RX: 6.1mA
 - Active mode TX at 0dBm: 7.0mA
 - Active mode TX at +5dBm: 9.3mA
 - Active mode MCU: 61µA/MHz
 - Active mode MCU: 48.5 CoreMark/mA
 - Active mode sensor controller: $0.4mA + 8.2\mu A/MHz$
 - Standby: 1.3µA (RTC running and RAM/CPU retention)
 - Shutdown: 150nA (wake up on external events)
- RF section
 - 2.4GHz RF transceiver compatible with Bluetooth Low Energy (BLE) 4.2 and 5 specifications
 - Excellent receiver sensitivity (–97dBm for Bluetooth Low Energy 1Mbps), selectivity, and blocking performance
 - Programmable output power up to +5dBm
 - Link budget of 102dB for Bluetooth Low Energy 1Mbps
 - Suitable for systems targeting compliance with worldwide radio frequency regulations
 - ETSI EN 300 328 and EN 300 440 (Europe)
 - FCC CFR47 Part 15 (US)
 - ARIB STD-T66 (Japan)
- Development Tools and Software
 - Full-feature development kits
 - Sensor Controller Studio
 - SmartRF™ Studio
 - IAR Embedded Workbench® for Arm®
 - Code Composer Studio[™] Integrated Development Environment (IDE)
 - Code Composer Studio™ Cloud IDE

2 Applications

- **Automotive**
 - Car access and security systems
 - Passive entry passive start (PEPS)
 - Phone as a key (PaaK)
 - Remote keyless entry (RKE)



- Industrial
 - Factory automation
 - Asset tracking and management

- Human machine interface (HMI)
- Access control

3 Description

The SimpleLink™ *Bluetooth* [®] low energy CC2640R2F-Q1 device is an AEC-Q100 compliant wireless microcontroller (MCU) targeting *Bluetooth* [®] 4.2 and *Bluetooth* [®] 5 low energy automotive applications such as Passive Entry/Passive Start (PEPS), remote keyless entry (RKE), car sharing, piloted parking, cable replacement, and smartphone connectivity.

The CC2640R2F-Q1 device is part of the SimpleLink™ MCU platform from Texas Instruments™. The platform consists of Wi-Fi®, *Bluetooth* ® low energy, Sub-1GHz, Ethernet, Zigbee®, Thread, and host MCUs. These devices all share a common, easy-to-use development environment with a single core software development kit (SDK) and rich tool set. A one-time integration of the SimpleLink™ platform enables users to add any combination of the portfolio's devices into their design, allowing 100 percent code reuse when design requirements change. For more information, visit http://www.ti.com/wireless-connectivity/simplelink-solutions/overview.html.

With very low active RF and MCU current consumption, in addition to flexible low power modes, the CC2640R2F-Q1 provides excellent battery life and allows long-range operation on small coin-cell batteries and a low power-consumption footprint for nodes connected to the car battery. Excellent receiver sensitivity and programmable output power provide industry-leading RF performance that is required for the demanding automotive RF environment.

The CC2640R2F-Q1 wireless MCU contains a 32-bit Arm[®] Cortex[®]-M3 processor that runs at 48MHz as the main application processor and includes the *Bluetooth* [®] 4.2 low energy controller and host libraries embedded in ROM. This architecture improves overall system performance and power consumption and frees up significant amounts of flash memory for the application.

Additionally, the device is AEC-Q100 Qualified at the Grade 2 temperature range (-40°C to +105°C) and is offered in a 7mm × 7mm VQFN packagewith wettable flanks. The wettable flanks help reduce production-line cost and increase the reliability enabled by optical inspection of solder points.

The Bluetooth Low Energy Software Stack is available free of charge from ti.com.

Device Information (1)

| PART NUMBER | PACKAGE | PACKAGE SIZE |
|------------------|--------------------------------|-----------------|
| CC2640R2FTWRGZQ1 | VQFN (48) with Wettable Flanks | 7.00mm × 7.00mm |

(1) For more information, see Mechanical, Packaging, and Orderable Information.

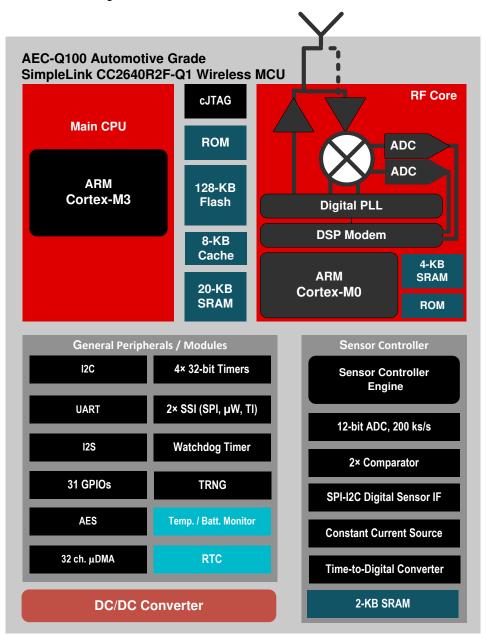
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4 Functional Block Diagram

Block Diagram shows a block diagram for the CC2640R2F-Q1 device.



Block Diagram



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5 Device Comparison

Table 5-1. Device Family Overview

| DEVICE | PHY SUPPORT | FLASH (KB) | RAM (KB) | GPIO | PACKAGE ⁽¹⁾ |
|-----------------------------|--|---------------|-------------|----------------|-------------------------------|
| CC2640R2F-Q1 ⁽²⁾ | Bluetooth Low Energy (Normal, High Speed, Long Range, Automotive) | 128 | 20 | 31 | RGZ (Wettable Flanks), RGZ |
| CC2640R2Fxxx ⁽²⁾ | Bluetooth Low Energy (Normal, High Speed, Long Range) | 128 | 20 | 31, 15, 14, 10 | RGZ, RHB, YFV, RSM |
| CC2650F128xxx | Multi-Protocol ⁽³⁾ | 128 | 20 | 31, 15, 10 | RGZ, RHB, RSM |
| CC2640F128xxx | Bluetooth Low Energy (Normal) | 128 | 20 | 31, 15, 10 | RGZ, RHB, RSM |
| CC2630F128xxx | IEEE 802.15.4 (Zigbee/6LoWPAN) | 128 | 20 | 31, 15, 10 | RGZ, RHB, RSM |
| CC2620F128xxx | IEEE 802.15.4 (RF4CE) | 128 | 20 | 31, 10 | RGZ, RSM |

- (1) Package designator replaces the xxx in device name to form a complete device name, RGZ is 7mm × 7mm VQFN48, RHB is 5mm × 5mm VQFN32, RSM is 4mm × 4mm VQFN32, and YFV is 2.7mm DSBGA.
- (2) CC2640R2F-xxx devices contain Bluetooth 4.2 Host and Controller libraries in ROM, leaving more of the 128KB of flash available for the customer application when used with supported BLE-Stack software protocol stack releases. Actual use of ROM and flash by the protocol stack may vary depending on device software configuration. See Bluetooth Low Energy Stack for more details.
- (3) The CC2650 device supports all PHYs and can be reflashed to run all the supported standards.

Table 5-2. Typical (1) Flash Memory Available for Customer Applications

| DEVICE | SIMPLE BLE PERIPHERAL (BT 4.0) ⁽²⁾ | SIMPLE BLE PERIPHERAL (BT 4.2) ^{(2) (3)} | | |
|---|---|---|--|--|
| CC2640R2Fxxx, CC2640R2F-Q1 ⁽⁴⁾ | 83KB | 80KB | | |
| CC2640F128xxx, CC2650F128xxx | 41KB | 31KB | | |

- (1) Actual use of ROM and flash by the protocol stack will vary depending on the device software configuration. The values in this table are provided as guidance only.
- (2) Application example with two services (GAP and Simple Profile). Compiled using IAR.
- (3) BT4.2 configuration, including Secure Pairing, Privacy 1.2, and Data Length Extension
- (4) Bluetooth Low Energy applications running on the CC2640R2F-Q1 device make use of up to 115KB of system ROM and up to 32KB of RF Core ROM to minimize flash usage. The maximum amount of nonvolatile memory available for Bluetooth Low Energy applications on the CC2640R2F-Q1 device is thus 275KB (128KB flash + 147KB ROM).

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5.1 Related Products

Wireless Connectivity

The wireless connectivity portfolio offers a wide selection of low power RF solutions suitable for a broad range of applications. The offerings range from fully customized solutions to turn key offerings with pre-certified hardware and software (protocol).

TI's SimpleLink™ Sub-1GHz Wireless **MCUs**

Long-range, low-power wireless connectivity solutions are offered in a wide range of Sub-1GHz ISM bands.

Design & development

Review design and development resources that are available for this product.

Wireless MCU LaunchPad™ **Development Kit**

SimpleLink™ CC2640R2 The CC2640R2 LaunchPad™ development kit brings easy Bluetooth Low Energy (BLE) connection to the LaunchPad ecosystem with the SimpleLink ultra-low power CC26xx family of devices. Compared to the CC2650 LaunchPad kit, the CC2640R2 LaunchPad kit provides the following:

- More free flash memory for the user application in the CC2640R2 wireless MCU
- Out-of-the-box support for Bluetooth 4.2 specification
- 4× faster over-the-air download speed compared to Bluetooth 4.1

SimpleLink™

The SensorTag IoT kit invites you to realize your cloud-connected product idea. The SensorTag includes 10 low-power MEMS sensors in a tiny red package, and it is Multistandard SensorTag expandable with DevPacks to make it easy to add your own sensors or actuators.

> TI Reference Design Library is a robust reference design library spanning analog, embedded processor and connectivity. Created by TI experts to help you jump-start your system design, all TI Designs include schematic or block diagrams, BOMs and design files to speed your time to market. Search and download designs at ti.com/ tidesigns.

Bluetooth Low Energy/ Reference Designs for

CC2640

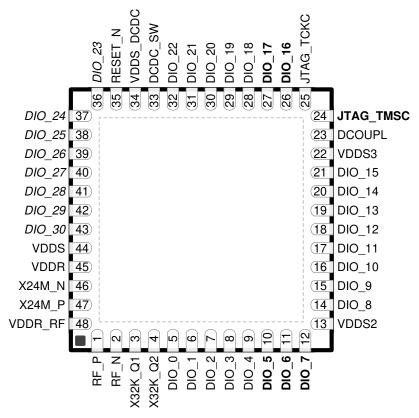
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6 Pin Configuration and Functions

6.1 Pin Diagram—RGZ Package



The following I/O pins marked in **bold** have high-drive capabilities:

- Pin 10: DIO 5
- Pin 11: DIO_6
- Pin 12: DIO 7
- Pin 24: JTAG TMSC
- Pin 26: DIO_16
- Pin 27: DIO_17

The following I/O pins marked in *italics* have analog capabilities:

- Pin 36: DIO 23
- Pin 37: DIO 24
- Pin 38: DIO_25
- Pin 39: DIO_26
- Pin 40: DIO_27
- Pin 41: DIO_28
- Pin 42: DIO 29
- Pin 43: DIO_30

Figure 6-1. 48-Pin RGZ Packagewith Wettable Flanks, 7mm × 7mm Pinout, 0.5mm Pitch (Top View)



6.2 Signal Descriptions—RGZ Package

Table 6-1. Signal Descriptions—RGZ Package

| | T | able 6-1. Signal | Descriptions—RGZ Package |
|-----------|-----|--------------------|--|
| NAME | NO. | TYPE | DESCRIPTION |
| DCDC_SW | 33 | Power | Output from internal DC/DC ⁽¹⁾ |
| DCOUPL | 23 | Power | 1.27V regulated digital-supply decoupling capacitor ⁽²⁾ |
| DIO_0 | 5 | Digital I/O | GPIO, Sensor Controller |
| DIO_1 | 6 | Digital I/O | GPIO, Sensor Controller |
| DIO_2 | 7 | Digital I/O | GPIO, Sensor Controller |
| DIO_3 | 8 | Digital I/O | GPIO, Sensor Controller |
| DIO_4 | 9 | Digital I/O | GPIO, Sensor Controller |
| DIO_5 | 10 | Digital I/O | GPIO, Sensor Controller, high-drive capability |
| DIO_6 | 11 | Digital I/O | GPIO, Sensor Controller, high-drive capability |
| DIO_7 | 12 | Digital I/O | GPIO, Sensor Controller, high-drive capability |
| DIO_8 | 14 | Digital I/O | GPIO |
| DIO_9 | 15 | Digital I/O | GPIO |
| DIO_10 | 16 | Digital I/O | GPIO |
| DIO_11 | 17 | Digital I/O | GPIO |
| DIO_12 | 18 | Digital I/O | GPIO |
| DIO_13 | 19 | Digital I/O | GPIO |
| DIO_14 | 20 | Digital I/O | GPIO |
| DIO_15 | 21 | Digital I/O | GPIO |
| DIO_16 | 26 | Digital I/O | GPIO, JTAG_TDO, high-drive capability |
| DIO_17 | 27 | Digital I/O | GPIO, JTAG_TDI, high-drive capability |
| DIO_18 | 28 | Digital I/O | GPIO |
| DIO_19 | 29 | Digital I/O | GPIO |
| DIO_20 | 30 | Digital I/O | GPIO |
| DIO_21 | 31 | Digital I/O | GPIO |
| DIO_22 | 32 | Digital I/O | GPIO |
| DIO_23 | 36 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_24 | 37 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_25 | 38 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_26 | 39 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_27 | 40 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_28 | 41 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_29 | 42 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_30 | 43 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| JTAG_TMSC | 24 | Digital I/O | JTAG TMSC, high-drive capability |
| JTAG_TCKC | 25 | Digital I/O | JTAG TCKC |
| RESET_N | 35 | Digital input | Reset, active-low. No internal pullup. |
| RF_P | 1 | RF I/O | Positive RF input signal to LNA during RX Positive RF output signal to PA during TX |
| RF_N | 2 | RF I/O | Negative RF input signal to LNA during RX Negative RF output signal to PA during TX |
| VDDR | 45 | Power | Connect to output of internal DC/DC ⁽²⁾ (3) |
| VDDR_RF | 48 | Power | Connect to output of internal DC/DC ⁽²⁾ (4) |

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Table 6-1. Signal Descriptions—RGZ Package (continued)

| NAME | NO. | TYPE | DESCRIPTION |
|-----------|-----|------------|--|
| VDDS | 44 | Power | 1.8V to 3.8V main chip supply ⁽¹⁾ |
| VDDS2 | 13 | Power | 1.8V to 3.8V DIO supply ⁽¹⁾ |
| VDDS3 | 22 | Power | 1.8V to 3.8V DIO supply ⁽¹⁾ |
| VDDS_DCDC | 34 | Power | 1.8V to 3.8V DC/DC supply |
| X32K_Q1 | 3 | Analog I/O | 32kHz crystal oscillator pin 1 |
| X32K_Q2 | 4 | Analog I/O | 32kHz crystal oscillator pin 2 |
| X24M_N | 46 | Analog I/O | 24MHz crystal oscillator pin 1 |
| X24M_P | 47 | Analog I/O | 24MHz crystal oscillator pin 2 |
| EGP | | Power | Ground—Exposed Ground Pad |

- (1) See the technical reference manual listed in Section 10.3 for more details.
- Do not supply external circuitry from this pin.
- If internal DC/DC is not used, this pin is supplied internally from the main LDO.
- If internal DC/DC is not used, this pin must be connected to VDDR for supply from the main LDO.

6.3 Wettable Flanks

The automotive industry requires original equipment manufacturers (OEMs) to perform 100% automated visual inspection (AVI) post-assembly to ensure that cars meet the current demands for safety and high reliability. Standard quad-flat no-lead (VQFN) packages do not have solderable or exposed pins/terminals that are easily viewed. It is therefore difficult to determine visually whether or not the package is successfully soldered onto the printed circuit board (PCB). To resolve the issue of side-lead wetting of leadless packaging for automotive and commercial component manufacturers, the wettable-flank process was developed. The wettable flanks on the VQFN package provide a visual indicator of solderability and thereby lower the inspection time and manufacturing costs.

The CC2640R2F-Q1 device is assembled using an automotive-grade VQFN package with wettable flanks.



7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

| | | MIN | MAX | UNIT |
|---|---|------|---------------------|------|
| Supply voltage, VDDS ⁽³⁾ | VDDR supplied by internal DC/DC regulator or internal GLDO. VDDS_DCDC connected to VDDS on PCB. | -0.3 | 4.1 | V |
| Voltage on any digital pin ^{(4) (5)} | | -0.3 | VDDS + 0.3, max 4.1 | V |
| Voltage on crystal oscillator pins | crystal oscillator pins, X32K_Q1, X32K_Q2, X24M_N and X24M_P —0.3 VDDR + 0.3, max 2.25 | | V | |
| | Voltage scaling enabled | -0.3 | VDDS | |
| Voltage on ADC input (V _{in}) | Voltage scaling disabled, internal reference | -0.3 | 1.49 | V |
| | Voltage scaling disabled, VDDS as reference | -0.3 | VDDS / 2.9 | |
| Input RF level | | | 5 | dBm |
| T _{stg} | Storage temperature | -40 | 150 | °C |

- (1) All voltage values are with respect to ground, unless otherwise noted.
- (2) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (3) VDDS2 and VDDS3 need to be at the same potential as VDDS.
- (4) Including analog-capable DIO.
- (5) Injection current is not supported on any GPIO pin.

7.2 ESD Ratings

| | | | | VALUE | UNIT |
|-----|-------------------------|---|------------------|-------|------|
| | | Human Body Model (HBM), per AEC Q100-002 ^{(1) (2)} | All pins | ±2000 | |
| VES | Electrostatic discharge | Charged Device Model (CDM), per AEC Q100-011 ⁽³⁾ | XOCS pins 46, 47 | ±250 | V |
| | | | All other pins | ±500 | |

- (1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
- (2) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (3) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|--------------------------------|--|-----|------|------|
| Ambient temperature | | -40 | 105 | °C |
| Operating supply voltage, VDDS | For operation in battery-powered and 3.3V systems (internal DC/DC can be used to minimize power consumption) | 1.8 | 3.8 | V |
| GPIO Input Voltage | | 0 | VDDS | V |



7.4 Power Consumption Summary

Measured on the TI CC2640Q1EM-7ID reference design with T_c = 25°C, V_{DDS} = 3.0V with internal DC/DC converter, unless otherwise noted.

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|-------------------|-----------------------------|---|--------------------------|-----|-----|------|--|
| | | Reset. RESET_N pin asserted or VDDS below power-on-reset (POR) threshold | | 100 | | nA | |
| | | Shutdown. No clocks running, no retention | | 150 | | | |
| | | Standby. With RTC, CPU, RAM and (partial) register retention. RCOSC_LF | | 1.3 | | | |
| | | Standby. With RTC, CPU, RAM and (partial) register retention. XOSC_LF | | 1.5 | | | |
| I _{core} | Core current consumption | Standby. With Cache, RTC, CPU, RAM and (partial) register retention. RCOSC_LF | | 3.4 | | μA | |
| | | Standby. With Cache, RTC, CPU, RAM and (partial) register retention. XOSC_LF | | 3.6 | | | |
| | | Idle. Supply Systems and RAM powered. | | 650 | | 1 | |
| | | Active. Core running CoreMark | 1.45mA + 31µA/MHz | | | | |
| | | Radio RX | | 6.1 | | mA | |
| | | Radio TX, 0dBm output power | | 7.0 | | | |
| | | Radio TX, 5dBm output power | | 9.3 | | | |
| Periph | eral Current Consumption (A | dds to core current l _{core} for each peripheral unit a | ctivated) ⁽¹⁾ | ı | | | |
| | Peripheral power domain | Delta current with domain enabled | | 20 | | μΑ | |
| | Serial power domain | Delta current with domain enabled | | 13 | | μΑ | |
| | RF Core | Delta current with power domain enabled, clock enabled, RF core idle | | 237 | | μΑ | |
| | μDMA | Delta current with clock enabled, module idle | | 130 | | μΑ | |
| I _{peri} | Timers | Delta current with clock enabled, module idle | | 113 | | μΑ | |
| | I ² C | Delta current with clock enabled, module idle | | 12 | | μΑ | |
| | 12S | Delta current with clock enabled, module idle | | 36 | | μA | |
| | SSI | Delta current with clock enabled, module idle | | 93 | | μA | |
| | UART | Delta current with clock enabled, module idle | | 164 | | μA | |

⁽¹⁾ I_{peri} is not supported in Standby or Shutdown.

7.5 General Characteristics

 T_c = 25°C, V_{DDS} = 3.0V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | | | |
|--|--|------|------|------|-------------------|--|--|--|
| FLASH MEMORY | | | | | | | | |
| Supported flash erase cycles before failure | | 100 | | | k Cycles | | | |
| Maximum number of write operations per row before erase ⁽¹⁾ | | | | 83 | write operations | | | |
| Flash retention | 105°C | 11.4 | | | Years at 105°C | | | |
| Flash page/sector erase current | Average delta current | | 12.6 | | mA | | | |
| Flash page/sector size | | | 4 | | KB | | | |
| Flash page/sector erase time ⁽²⁾ | Zero cycles | | 8 | | ms | | | |
| Flash page/sector erase time (2) | 30 000 cycles | | | 4000 | ms | | | |
| Flash write current | Average delta current, 4 bytes at a time | | 8.15 | | mA | | | |



7.5 General Characteristics (continued)

 T_c = 25°C, V_{DDS} = 3.0V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|-------------------|-----|-----|-----|------|
| Flash write time | 4 bytes at a time | | 8 | | μs |

- Each row is 2048 bits (or 256 bytes) wide.
- This number is dependent on Flash aging and will increase over time and erase cycles.

7.6 1Mbps GFSK (Bluetooth Low Energy Technology)—RX

Measured on the TI CC2640Q1EM-7ID reference design with T_c = 25°C, V_{DDS} = 3.0V, f_{RF} = 2440MHz, unless otherwise

| PARAMETER | TEST CONDITIONS | MIN TYP | MAX | UNIT |
|---|---|----------------------------|-----|------|
| Receiver sensitivity | Differential mode. Measured at the CC2640Q1EM-7ID SMA connector, BER = 10^{-3} | -97 | | dBm |
| Receiver saturation | Differential mode. Measured at the CC2640Q1EM-7ID SMA connector, BER = 10 ⁻³ | 4 | | dBm |
| Frequency error tolerance | Difference between the incoming carrier frequency and the internally generated carrier frequency | -350 | 350 | kHz |
| Data rate error tolerance | Difference between incoming data rate and the internally generated data rate | –750 | 750 | ppm |
| Co-channel rejection ⁽³⁾ | Wanted signal at –67dBm, modulated interferer in channel, BER = 10 ⁻³ | -6 | | dB |
| Selectivity, ±1MHz ⁽³⁾ | Wanted signal at –67dBm, modulated interferer at ±1MHz, BER = 10 ⁻³ | 7 / 2 ⁽¹⁾ | | dB |
| Selectivity, ±2MHz ⁽³⁾ | Wanted signal at –67dBm, modulated interferer at ±2MHz, Image frequency is at –2MHz, BER = 10 ⁻³ | 39 / 17 ^{(2) (1)} | | dB |
| Selectivity, ±3MHz ⁽³⁾ | Wanted signal at –67dBm, modulated interferer at ±3MHz, BER = 10 ⁻³ | 38 / 30(1) | | dB |
| Selectivity, ±4MHz ⁽³⁾ | Wanted signal at –67dBm, modulated interferer at ±4MHz, BER = 10 ⁻³ | 42 / 36 ⁽¹⁾ | | dB |
| Selectivity, ±5MHz or more ⁽³⁾ | Wanted signal at –67dBm, modulated interferer at ≥ ±5MHz, BER = 10 ⁻³ | 32 | | dB |
| Selectivity, Image frequency ⁽³⁾ | Wanted signal at –67dBm, modulated interferer at image frequency, BER = 10 ⁻³ | 17 | | dB |
| Selectivity, Image frequency ±1MHz ⁽³⁾ | Wanted signal at –67dBm, modulated interferer at ±1MHz from image frequency, BER = 10 ⁻³ | 2 / 30 ⁽¹⁾ | | dB |
| Out-of-band blocking (4) | 30MHz to 2000MHz | -20 | | dBm |
| Out-of-band blocking | 2003MHz to 2399MHz | - 5 | | dBm |
| Out-of-band blocking | 2484MHz to 2997MHz | -8 | | dBm |
| Out-of-band blocking | 3000MHz to 12.75GHz | -8 | | dBm |
| Intermodulation | Wanted signal at 2402MHz, –64dBm. Two interferers at 2405 and 2408MHz respectively, at the given power level | -34 | | dBm |
| Spurious emissions, 30MHz to 1000MHz | Conducted measurement in a 50Ω single-ended load. Suitable for systems targeting compliance with EN 300 328, EN 300 440, FCC CFR47, Part 15 and ARIB STD-T-66 | -65 | | dBm |
| Spurious emissions, 1GHz to 12.75 GHz | Conducted measurement in a 50Ω single-ended load. Suitable for systems targeting compliance with EN 300 328, EN 300 440, FCC CFR47, Part 15 and ARIB STD-T-66 | -52 | | dBm |
| RSSI dynamic range | | 70 | | dB |
| RSSI accuracy | | ±4 | | dB |

- (1) X / Y, where X is +N MHz and Y is -N MHz.
- +2MHz selectivity is reduced to 33dB when using radio FW supporting 2Mbps and Coded PHYs (2)
- Numbers given as I/C dB.

(4) Excluding one exception at F_{wanted} / 2, per Bluetooth Specification.

7.7 1Mbps GFSK (Bluetooth Low Energy Technology)—TX

Measured on the TI CC2640Q1EM-7ID reference design with T_c = 25°C, V_{DDS} = 3.0V, f_{RF} = 2440MHz, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|--|-----|-----|-----|------|
| Output power, highest setting | Differential mode, delivered to a single-ended 50Ω load through a balun | | 5 | | dBm |
| Output power, lowest setting | Delivered to a single-ended 50Ω load through a balun | | -21 | | dBm |
| | f < 1GHz, outside restricted bands | | -44 | | dBm |
| Spurious emission conducted | f < 1GHz, restricted bands ETSI | | -62 | | dBm |
| measurement ⁽¹⁾ | f < 1GHz, restricted bands FCC | | -62 | | dBm |
| | f > 1GHz, including harmonics | | -55 | | dBm |

⁽¹⁾ Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

7.8 24MHz Crystal Oscillator (XOSC_HF)

 $T_c = 25$ °C, $V_{DDS} = 3.0$ V, unless otherwise noted. (1)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|-----|---------------------------------|-----|------|
| ESR Equivalent series resistance ⁽²⁾ | 6pF < C _L ≤ 9pF | | 20 | 60 | Ω |
| ESR Equivalent series resistance ⁽²⁾ | 5pF < C _L ≤ 6pF | | | 80 | Ω |
| L _M Motional inductance ⁽²⁾ | Relates to load capacitance (C _L in Farads) | | $< 1.6 \times 10^{-24} / C_L^2$ | | Н |
| C _L Crystal load capacitance ⁽²⁾ | | 5 | | 9 | pF |
| Crystal frequency ^{(2) (3)} | | | 24 | | MHz |
| Crystal frequency tolerance ^{(2) (4)} | | -40 | | 40 | ppm |
| Start-up time ^{(3) (5)} | | | 150 | | μs |

- (1) Probing or otherwise stopping the crystal while the DC/DC converter is enabled may cause permanent damage to the device.
- (2) The crystal manufacturer's specification must satisfy this requirement
- (3) Measured on the TI CC2640Q1EM-7ID reference design with $T_c = 25$ °C, $V_{DDS} = 3.0V$
- (4) Includes initial tolerance of the crystal, drift over temperature, ageing and frequency pulling due to incorrect load capacitance, as per Bluetooth specification.
- (5) Kick-started based on a temperature and aging compensated RCOSC_HF using precharge injection.

7.9 32.768kHz Crystal Oscillator (XOSC_LF)

 T_c = 25°C, V_{DDS} = 3.0V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-----------------|------|--------|-----|------|
| Crystal frequency ⁽¹⁾ | | | 32.768 | | kHz |
| Crystal frequency tolerance, Bluetooth low-energy applications ⁽¹⁾ (2) | | -500 | | 500 | ppm |
| ESR Equivalent series resistance ⁽¹⁾ | | | 30 | 100 | kΩ |
| C _L Crystal load capacitance ⁽¹⁾ | | 6 | | 12 | pF |

- 1) The crystal manufacturer's specification must satisfy this requirement.
- (2) Includes initial tolerance of the crystal, drift over temperature, ageing and frequency pulling due to incorrect load capacitance, as per Bluetooth specification.

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7.10 48MHz RC Oscillator (RCOSC_HF)

Measured on the TI CC2640Q1EM-7ID reference design with $T_c = 25$ °C, $V_{DDS} = 3.0$ V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN TYI | P MAX | UNIT |
|--|-----------------|---------|----------|------|
| Frequency | | 4 | 3 | MHz |
| Uncalibrated frequency accuracy | | ±19 | 6 | |
| Calibrated frequency accuracy ⁽¹⁾ | | ±0.25% | 6 | |
| Start-up time | | | 5 | μs |

⁽¹⁾ Accuracy relative to the calibration source (XOSC_HF).

7.11 32kHz RC Oscillator (RCOSC_LF)

Measured on the TI CC2640Q1EM-7ID reference design with T_c = 25°C, V_{DDS} = 3.0V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------------|-----------------|-----|------|-----|--------|
| Calibrated frequency ⁽¹⁾ | | | 32.8 | | kHz |
| Temperature coefficient | | | 50 | | ppm/°C |

⁽¹⁾ The frequency accuracy of the real time clock (RTC) is not directly dependent on the frequency accuracy of the 32kHz RC oscillator. The RTC can be calibrated by measuring the frequency error of RCOSC_LF relative to XOSC_HF and compensating the RTC tick speed.

7.12 ADC Characteristics

 $T_c = 25^{\circ}C$, $V_{DDS} = 3.0V$ without internal DC/DC converter and with voltage scaling enabled, unless otherwise noted. (1)

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|-----------------------------|--|-----|------------|------|------|
| | Input voltage range | | 0 | | VDDS | V |
| | Resolution | | | 12 | | Bits |
| | Sample rate | | | | 200 | ksps |
| | Offset | Internal 4.3V equivalent reference ⁽²⁾ | | 2 | | LSB |
| | Gain error | Internal 4.3V equivalent reference ⁽²⁾ | | 2.4 | | LSB |
| DNL ⁽³⁾ | Differential nonlinearity | | | >–1 | | LSB |
| INL ⁽⁴⁾ | Integral nonlinearity | | | ±3 | | LSB |
| | | Internal 4.3V equivalent reference ⁽²⁾ , 200ksps, 9.6kHz input tone | | 9.8 | | |
| ENOB | Effective number of bits | VDDS as reference, 200ksps, 9.6kHz input tone | | 10 | | Bits |
| | | Internal 1.44V reference, voltage scaling disabled, 32 samples average, 200ksps, 300Hz input tone | | | | |
| | | Internal 4.3V equivalent reference ⁽²⁾ , 200ksps, 9.6kHz input tone | | -65 | | |
| THD | Total harmonic distortion | VDDS as reference, 200ksps, 9.6kHz input tone | | -69 | | dB |
| | | Internal 1.44V reference, voltage scaling disabled, 32 samples average, 200ksps, 300Hz input tone | | –71 | | |
| | Signal-to-noise | Internal 4.3V equivalent reference ⁽²⁾ , 200ksps, 9.6kHz input tone | | 60 | | |
| SINAD, SNDR | and | VDDS as reference, 200ksps, 9.6kHz input tone | | 63 | | dB |
| ONDIX | Distortion ratio | Internal 1.44V reference, voltage scaling disabled, 32 samples average, 200ksps, 300Hz input tone | | 69 | | |
| | | Internal 4.3V equivalent reference ⁽²⁾ , 200ksps, 9.6kHz input tone | | 67 | | |
| SFDR | Spurious-free dynamic range | VDDS as reference, 200ksps, 9.6kHz input tone | | 72 | | dB |
| | lango | Internal 1.44V reference, voltage scaling disabled, 32 samples average, 200ksps, 300Hz input tone | | 73 | | |

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 $T_c = 25$ °C, $V_{DDS} = 3.0$ V without internal DC/DC converter and with voltage scaling enabled, unless otherwise noted. (1)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|---|-----|-------------------------------|-----|------------------|
| Conversion time | Serial conversion, time-to-output, 24MHz clock | | 50 | | clock- cycles |
| Current consumption | Internal 4.3V equivalent reference ⁽²⁾ | | 0.66 | | mA |
| Current consumption | VDDS as reference | | 0.75 | | mA |
| Reference voltage | Equivalent fixed internal reference (input voltage scaling enabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API to include the gain/offset compensation factors stored in FCFG1. | 4 | .3 ^{(2) (5)} | | V |
| Reference voltage | Fixed internal reference (input-voltage scaling disabled). For the best accuracy, the ADC conversion should be initiated through the TI-RTOS API to include the gain/ offset compensation factors stored in FCFG1. This value is derived from the scaled value (4.3V) as follows. $V_{ref} = 4.3V \times 1408 / 4095$ | | 1.48 | | V |
| Reference voltage | VDDS as reference (also known as <i>RELATIVE</i>) (input voltage scaling enabled) | | VDDS | | V |
| Reference voltage | VDDS as reference (also known as <i>RELATIVE</i>) (input voltage scaling disabled) | \ | /DDS / 2.82 ⁽⁵⁾ | | V |
| Input Impedance | 200ksps, voltage scaling enabled. Capacitive input, input impedance depends on sampling frequency and sampling time | | >1 | | ΜΩ |

- Using IEEE Std 1241[™]-2010 for terminology and test methods.
- Input signal scaled down internally before conversion, as if voltage range was 0V to 4.3V. (2)
- (3) No missing codes. Positive DNL typically varies from +0.3 to +3.5, depending on the device (see Figure 7-21).
- (4) For a typical example, see Figure 7-22.
- Applied voltage must be within absolute maximum ratings at all times (see Section 7.1).

7.13 Temperature Sensor

Measured on the TI CC2640Q1EM-7ID reference design with $T_c = 25^{\circ}C$, $V_{DDS} = 3.0V$, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-----------------|-----|-----|-----|------|
| Resolution | | | 4 | | °C |
| Range | | -40 | | 105 | °C |
| Accuracy | | | ±5 | | °C |
| Supply voltage coefficient ⁽¹⁾ | | | 3.2 | | °C/V |

⁽¹⁾ Automatically compensated when using supplied driver libraries.

7.14 Battery Monitor

Measured on the TI CC2640Q1EM-7ID reference design with $T_c = 25^{\circ}C$, $V_{DDS} = 3.0V$, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------|-----------------|-----|-----|-----|------|
| Resolution | | | 50 | | mV |
| Range | | 1.8 | | 3.8 | V |
| Accuracy | | | 13 | | mV |

7.15 Continuous Time Comparator

 $T_c = 25$ °C, $V_{DDS} = 3.0$ V, unless otherwise noted.

| , , , | | | | | |
|----------------------------|---------------------|-----|------|------|------|
| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| Input voltage range | | 0 | | VDDS | V |
| External reference voltage | | 0 | | VDDS | V |
| Internal reference voltage | DCOUPL as reference | | 1.27 | | V |
| Offset | | | 3 | | mV |

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 T_c = 25°C, V_{DDS} = 3.0V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-------------------------|-----|------|-----|------|
| Hysteresis | | | <2 | | mV |
| Decision time | Step from –10mV to 10mV | | 0.72 | | μs |
| Current consumption when enabled ⁽¹⁾ | | | 8.6 | | μA |

(1) Additionally, the bias module must be enabled when running in standby mode.



7.16 Low-Power Clocked Comparator

 $T_c = 25$ °C, $V_{DDS} = 3.0$ V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-------------------------|-----|-----------|------|-------------|
| Input voltage range | | 0 | | VDDS | V |
| Clock frequency | | | 32 | | kHz |
| Internal reference voltage, VDDS / 2 | | | 1.49–1.51 | | V |
| Internal reference voltage, VDDS / 3 | | | 1.01-1.03 | | V |
| Internal reference voltage, VDDS / 4 | | | 0.78-0.79 | | V |
| Internal reference voltage, DCOUPL / 1 | | | 1.25–1.28 | | V |
| Internal reference voltage, DCOUPL / 2 | | | 0.63-0.65 | | V |
| Internal reference voltage, DCOUPL / 3 | | | 0.42-0.44 | | V |
| Internal reference voltage, DCOUPL / 4 | | | 0.33-0.34 | | V |
| Offset | | | <2 | | mV |
| Hysteresis | | | <5 | | mV |
| Decision time | Step from -50mV to 50mV | | <1 | | clock-cycle |
| Current consumption when enabled | | | 362 | | nA |

7.17 Programmable Current Source

 T_c = 25°C, V_{DDS} = 3.0V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|-----|---------|-----|------|
| Current source programmable output range | | | 0.25–20 | | μΑ |
| Resolution | | | 0.25 | | μA |
| Current consumption ⁽¹⁾ | Including current source at maximum programmable output | | 23 | | μΑ |

⁽¹⁾ Additionally, the bias module must be enabled when running in standby mode.

7.18 Synchronous Serial Interface (SSI)

 T_c = 25°C, V_{DDS} = 3.0V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|-----|-----|-------|----------------------|
| S1 ⁽¹⁾ t _{clk_per} (SSIClk period) | Device operating as SLAVE | 12 | | 65024 | system clocks |
| S2 ⁽¹⁾ t _{clk_high} (SSIClk high time) | Device operating as SLAVE | | 0.5 | | t _{clk_per} |
| S3 ⁽¹⁾ t _{clk_low} (SSIClk low time) | Device operating as SLAVE | | 0.5 | | t _{clk_per} |
| S1 (TX only) ⁽¹⁾ t _{clk_per} (SSIClk period) | One-way communication to SLAVE: Device operating as MASTER | 4 | | 65024 | system clocks |
| S1 (TX and RX) ⁽¹⁾ t _{clk_per} (SSIClk period) | Normal duplex operation: Device operating as MASTER | 8 | | 65024 | system clocks |
| S2 ⁽¹⁾ t _{clk_high} (SSIClk high time) | Device operating as MASTER | | 0.5 | | t _{clk_per} |
| S3 ⁽¹⁾ t _{clk_low} (SSIClk low time) | Device operating as MASTER | | 0.5 | | t _{clk_per} |

⁽¹⁾ Refer to SSI timing diagrams Figure 7-1, Figure 7-2, and Figure 7-3.



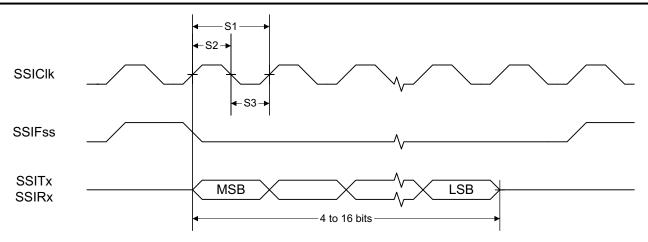


Figure 7-1. SSI Timing for TI Frame Format (FRF = 01), Single Transfer Timing Measurement

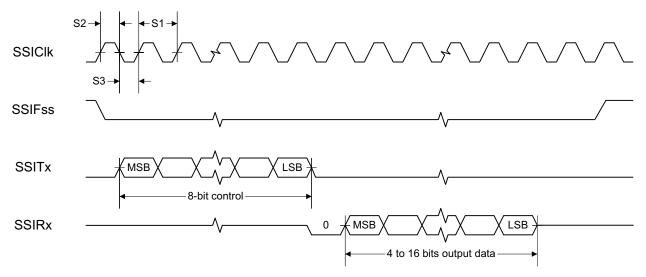


Figure 7-2. SSI Timing for MICROWIRE Frame Format (FRF = 10), Single Transfer

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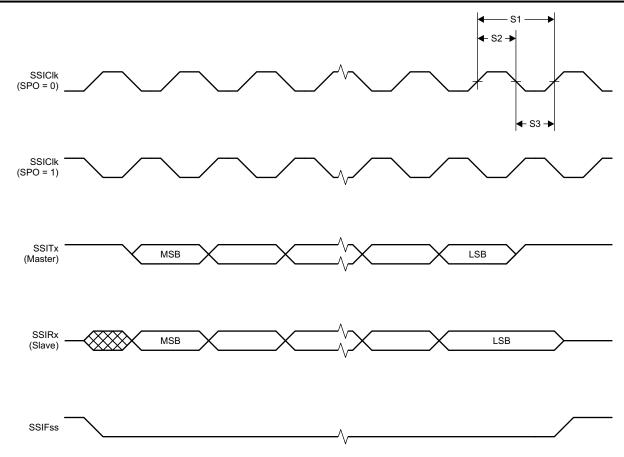


Figure 7-3. SSI Timing for SPI Frame Format (FRF = 00), With SPH = 1

7.19 DC Characteristics

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|------|------|------|------|
| $T_A = 25^{\circ}C, V_{DDS} = 1.8V$ | | | | | |
| GPIO V _{OH} at 8mA load | IOCURR = 2, high-drive GPIOs only | 1.32 | 1.54 | | V |
| GPIO V _{OL} at 8mA load | IOCURR = 2, high-drive GPIOs only | | 0.26 | 0.32 | V |
| GPIO V _{OH} at 4mA load | IOCURR = 1 | 1.32 | 1.58 | | V |
| GPIO V _{OL} at 4mA load | IOCURR = 1 | | 0.21 | 0.32 | V |
| GPIO pullup current | Input mode, pullup enabled, V _(pad) = 0V | | 71.7 | | μA |
| GPIO pulldown current | Input mode, pulldown enabled, V _(pad) = VDDS | | 21.1 | | μΑ |
| GPIO high/low input transition, no hysteresis | I _H = 0, transition between reading 0 and reading 1 | | 0.88 | | V |
| GPIO low-to-high input transition, with hysteresis | I_H = 1, transition voltage for input read as $0 \rightarrow 1$ | | 1.07 | | V |
| GPIO high-to-low input transition, with hysteresis | $I_H = 1$, transition voltage for input read as $1 \rightarrow 0$ | | 0.74 | | V |
| GPIO input hysteresis | I_H = 1, difference between 0 \rightarrow 1 and 1 \rightarrow 0 points | | 0.33 | | V |



| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|----------------------------------|------|-----|---------------------|
| T _A = 25°C, V _{DDS} = 3.0V | | | | | |
| GPIO V _{OH} at 8mA load | IOCURR = 2, high-drive GPIOs only | | 2.68 | | V |
| GPIO V _{OL} at 8mA load | IOCURR = 2, high-drive GPIOs only | | 0.33 | | V |
| GPIO V _{OH} at 4mA load | IOCURR = 1 | | 2.72 | | V |
| GPIO V _{OL} at 4mA load | IOCURR = 1 | | 0.28 | | V |
| T _A = 25°C, V _{DDS} = 3.8V | | | | | |
| GPIO pullup current | Input mode, pullup enabled, $V_{(pad)} = 0V$ | | 277 | | μΑ |
| GPIO pulldown current | Input mode, pulldown enabled, V _(pad) = VDDS | | 113 | | μA |
| GPIO high/low input transition, no hysteresis | I _H = 0, transition between reading 0 and reading 1 | | 1.67 | | V |
| GPIO low-to-high input transition, with hysteresis | $I_H = 1$, transition voltage for input read as $0 \rightarrow 1$ | | 1.94 | | V |
| GPIO high-to-low input transition, with hysteresis | $I_H = 1$, transition voltage for input read as $1 \rightarrow 0$ | | 1.54 | | V |
| GPIO input hysteresis | I_H = 1, difference between 0 \rightarrow 1 and 1 \rightarrow 0 points | | 0.4 | | V |
| T _A = 25°C | | | | | |
| V _(IH) | Lowest GPIO input voltage reliably interpreted as a «High» | | | 0.8 | VDDS ⁽¹⁾ |
| $V_{(IL)}$ | Highest GPIO input voltage reliably interpreted as a «Low» | ge reliably interpreted as a 0.2 | | | VDDS ⁽¹⁾ |

⁽¹⁾ Each GPIO is referenced to a specific VDDS pin. See the technical reference manual listed in Section 10.3 for more details.

7.20 Thermal Resistance Characteristics for RGZ Package

over operating free-air temperature range (unless otherwise noted)

| NAME | DESCRIPTION | (°C/W) ⁽¹⁾ (2) |
|-----------------------|--|---------------------------|
| Rθ _{JA} | Junction-to-ambient thermal resistance | 29.6 |
| Rθ _{JC(top)} | Junction-to-case (top) thermal resistance | 15.7 |
| Rθ _{JB} | Junction-to-board thermal resistance | 6.2 |
| Psi _{JT} | Junction-to-top characterization parameter | 0.3 |
| Psi _{JB} | Junction-to-board characterization parameter | 6.2 |
| Rθ _{JC(bot)} | Junction-to-case (bottom) thermal resistance | 1.9 |

- (1) °C/W = degrees Celsius per watt.
- (2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [Rθ_{JC}] value, which is based on a JEDEC-defined 1S0P system) and will change based on the environment as well as application. For more information, see the following EIA/JEDEC standards:
 - JESD51-2, Integrated Circuits Thermal Test Method Environmental Conditions Natural Convection (Still Air)
 - JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
 - JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
 - JESD51-9, Test Boards for Area Array Surface Mount Package Thermal Measurements

Power dissipation of 2W and an ambient temperature of 70°C is assumed.



7.21 Timing Requirements

| | | MIN | NOM | MAX | UNIT |
|--|--|-----|-----|-----|-------|
| Rising supply-voltage slew rate | | 0 | | 100 | mV/μs |
| Falling supply-voltage slew rate | | 0 | | 20 | mV/μs |
| Falling supply-voltage slew rate, with low-power flash settings ⁽¹⁾ | | | | 3 | mV/μs |
| Positive temperature gradient in standby ⁽³⁾ | No limitation for negative temperature gradient, or outside standby mode | | | 5 | °C/s |
| CONTROL INPUT AC CHARACTERISTICS(2) | | | | ' | |
| RESET_N low duration | | 1 | | | μs |

⁽¹⁾ For smaller coin cell batteries, with high worst-case end-of-life equivalent source resistance, a 22µF VDDS input capacitor (see Figure 9-1) must be used to ensure compliance with this slew rate.

7.22 Switching Characteristics

Measured on the TI CC2640Q1EM-7ID reference design with T_c = 25°C, V_{DDS} = 3.0V, unless otherwise noted.

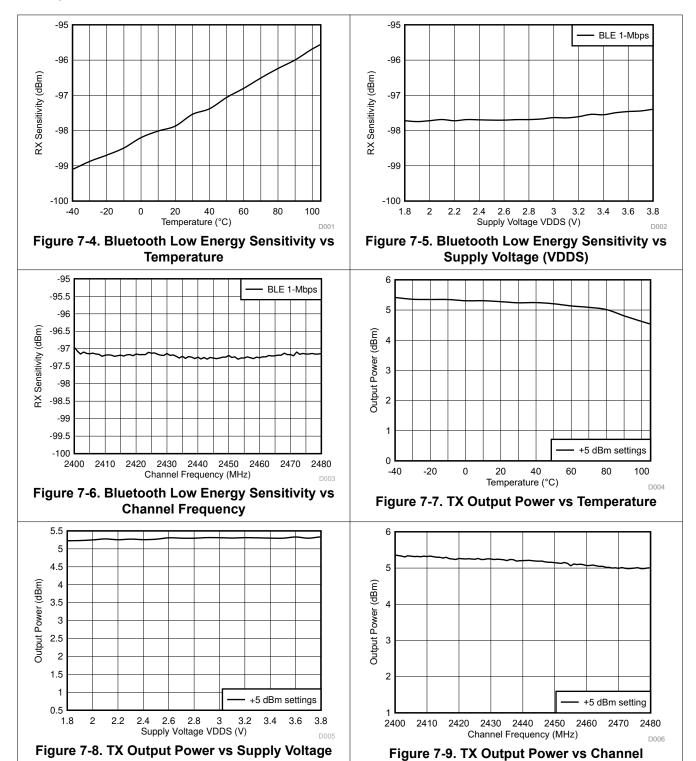
| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------|-----------------|-----|------|-----|------|
| WAKEUP and TIMING | | | | | |
| Idle → Active | | | 14 | | μs |
| Standby → Active | | | 151 | | μs |
| Shutdown → Active | | | 1015 | | μs |

⁽²⁾ $T_A = -40^{\circ}\text{C}$ to +105°C, $V_{DDS} = 1.8\text{V}$ to 3.8V, unless otherwise noted.

⁽³⁾ Applications using RCOSC_LF as a sleep timer must also consider the drift in frequency caused by a change in temperature. See Section 7.11



7.23 Typical Characteristics



(VDDS)

Frequency



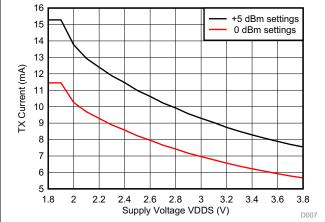


Figure 7-10. TX Current Consumption vs Supply Voltage (VDDS)

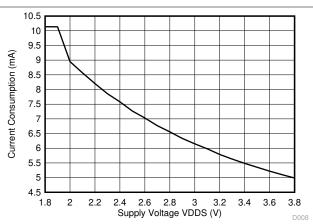


Figure 7-11. RX Mode Current vs Supply Voltage (VDDS)

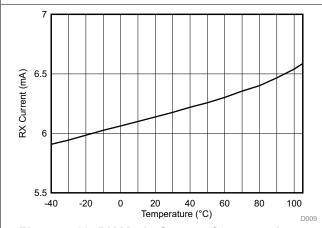


Figure 7-12. RX Mode Current Consumption vs
Temperature

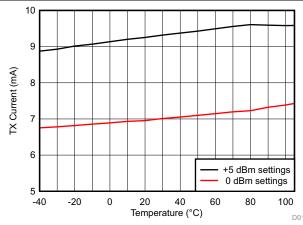


Figure 7-13. TX Mode Current Consumption vs
Temperature

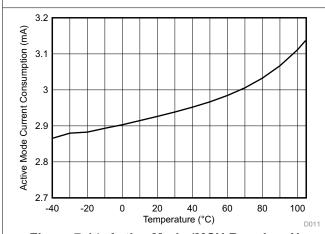


Figure 7-14. Active Mode (MCU Running, No Peripherals) Current Consumption vs Temperature

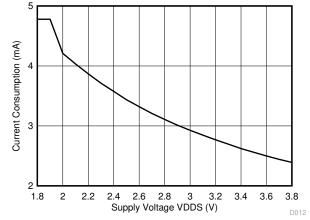


Figure 7-15. Active Mode (MCU Running, No Peripherals) Current Consumption vs Supply Voltage (VDDS)



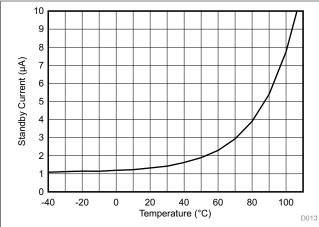


Figure 7-16. Standby Mode Current Consumption vs Temperature

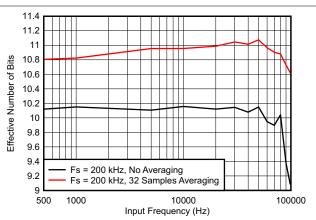


Figure 7-17. SoC ADC Effective Number of Bits vs Input Frequency (Internal Reference, No Scaling)

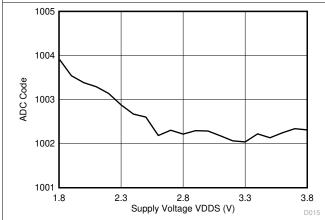


Figure 7-18. SoC ADC Output vs Supply Voltage (Fixed Input, Internal Reference, No Scaling)

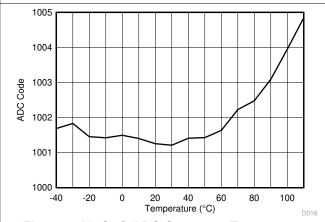


Figure 7-19. SoC ADC Output vs Temperature (Fixed Input, Internal Reference, No Scaling)

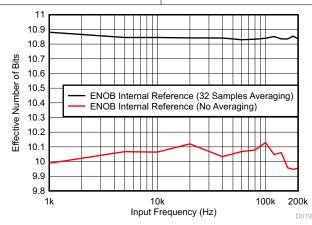
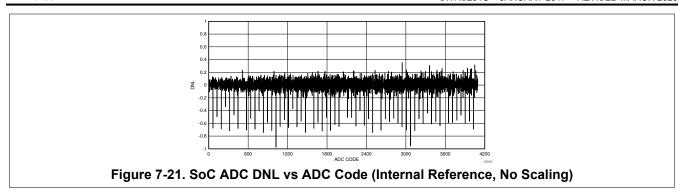
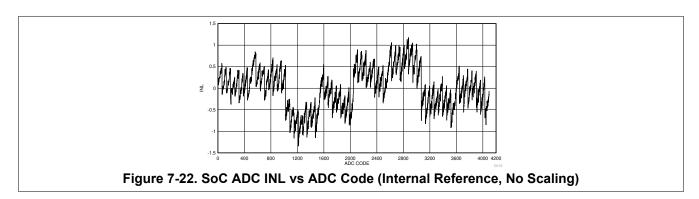


Figure 7-20. SoC ADC ENOB vs Sampling Frequency (Input Frequency = FS / 10)

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8 Detailed Description

8.1 Overview

Section 4 shows the core modules of the CC26xx product family.

8.2 Main CPU

The automotive grade SimpleLink™ CC2640R2F-Q1 Wireless MCU contains an Arm® Cortex®-M3 (CM3) 32-bit CPU, which runs the application and the higher layers of the protocol stack.

The Cortex®-M3 processor provides a high-performance, low-cost platform that meets the system requirements of minimal memory implementation, and low-power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

Cortex-M3 features include the following:

- 32-bit Arm® Cortex®-M3 architecture optimized for small-footprint embedded applications
- · Outstanding processing performance combined with fast interrupt handling
- Arm Thumb®-2 mixed 16- and 32-bit instruction set delivers the high performance expected of a 32-bit Arm core in a compact memory size usually associated with 8- and 16-bit devices, typically in the range of a few kilobytes of memory for microcontroller-class applications:
 - Single-cycle multiply instruction and hardware divide
 - Atomic bit manipulation (bit-banding), delivering maximum memory use and streamlined peripheral control
 - Unaligned data access, enabling data to be efficiently packed into memory
- · Fast code execution permits slower processor clock or increases sleep mode time
- Harvard architecture characterized by separate buses for instruction and data
- Efficient processor core, system, and memories
- Hardware division and fast digital-signal-processing oriented multiply accumulate
- · Saturating arithmetic for signal processing
- Deterministic, high-performance interrupt handling for time-critical applications
- Enhanced system debug with extensive breakpoint and trace capabilities
- Serial wire trace reduces the number of pins required for debugging and tracing
- Migration from the ARM7[™] processor family for better performance and power efficiency
- · Optimized for single-cycle flash memory use
- Ultra-low power consumption with integrated sleep modes
- 1.25 DMIPS per MHz

8.3 RF Core

The RF Core contains an Arm Cortex-M0 processor that interfaces the analog RF and base-band circuitries, handles data to and from the system side, and assembles the information bits in a given packet structure. The RF core offers a high-level, command-based API to the main CPU.

The RF core is capable of autonomously handling the time-critical aspects of the radio protocols (*Bluetooth* [®] low energy), thus offloading the main CPU and leaving more resources for the user application.

The RF core has a dedicated 4KB SRAM block and runs initially from separate ROM memory. The Arm Cortex-M0 processor is not programmable by customers.

8.4 Sensor Controller

The Sensor Controller contains circuitry that can be selectively enabled in standby mode. The peripherals in this domain may be controlled by the Sensor Controller Engine, which is a proprietary power-optimized CPU. This CPU can read and monitor sensors or perform other tasks autonomously, thereby significantly reducing power consumption and offloading the main Cortex-M3 CPU.

The Sensor Controller is set up using a PC-based configuration tool, called Sensor Controller Studio, and potential use cases may be (but are not limited to):

- Analog sensors using integrated ADC
- Digital sensors using GPIOs, bit-banged I²C, and SPI
- UART communication for sensor reading or debugging
- · Capacitive sensing
- Waveform generation
- · Pulse counting
- Keyboard scan
- · Quadrature decoder for polling rotation sensors
- Oscillator calibration

Note

Texas Instruments provides application examples for some of these use cases, but not for all of them.

The peripherals in the Sensor Controller include the following:

- The low-power clocked comparator can be used to wake the device from any state in which the comparator
 is active. A configurable internal reference can be used in conjunction with the comparator. The output of the
 comparator can also be used to trigger an interrupt or the ADC.
- Capacitive sensing functionality is implemented through the use of a constant current source, a time-to-digital converter, and a comparator. The continuous time comparator in this block can also be used as a higher-accuracy alternative to the low-power clocked comparator. The Sensor Controller will take care of baseline tracking, hysteresis, filtering and other related functions.
- The ADC is a 12-bit, 200-ksamples/s ADC with eight inputs and a built-in voltage reference. The ADC can be triggered by many different sources, including timers, I/O pins, software, the analog comparator, and the RTC.
- The Sensor Controller also includes a SPI–I²C digital interface.
- The analog modules can be connected to up to eight different GPIOs.

The peripherals in the Sensor Controller can also be controlled from the main application processor.



Table 8-1. GPIOs Connected to the Sensor Controller (1)

| ANALOG CAPABLE | 7 × 7 RGZ DIO NUMBER |
|----------------|-------------------------|
| Y | 30 |
| Y | 29 |
| Y | 28 |
| Y | 27 |
| Y | 26 |
| Y | 25 |
| Y | 24 |
| Y | 23 |
| N | 7 |
| N | 6 |
| N | 5 |
| N | 4 |
| N | 3 |
| N | 2 |
| N | 1 |
| N | 0 |

⁽¹⁾ Up to 16 pins can be connected to the Sensor Controller. Up to 8 of these pins can be connected to analog modules.

8.5 Memory

The flash memory provides nonvolatile storage for code and data. The flash memory is in-system programmable.

The SRAM (static RAM) can be used for both storage of data and execution of code and is split into two 4-KB blocks and two 6-KB blocks. Retention of the RAM contents in standby mode can be enabled or disabled individually for each block to minimize power consumption. In addition, if flash cache is disabled, the 8KB cache can be used as a general-purpose RAM.

The ROM provides preprogrammed embedded TI-RTOS kernel, Driver Library, and lower layer protocol stack software (*Bluetooth* [®] low energy Controller). It also contains a bootloader that can be used to reprogram the device using SPI or UART.

8.6 Debug

The on-chip debug support is done through a dedicated cJTAG (IEEE 1149.7) or JTAG (IEEE 1149.1) interface.

8.7 Power Management

To minimize power consumption, the CC2640R2F-Q1 device supports a number of power modes and power management features (see Table 8-2).

SOFTWARE CONFIGURABLE POWER MODES **RESET PIN** MODE **HELD ACTIVE** IDLE **STANDBY SHUTDOWN CPU** Off Active Off Off Off Flash On Available Off Off Off SRAM On On On Off Off Radio Available Available Off Off Off Off Off Supply System On On **Duty Cycled** Current 1.45 mA + 31 µA/MHz 650 µA 1.3 µA $0.15 \mu A$ 0.1 µA Wake-up Time to CPU Active(1) 14 µs 151 µs 1015 µs 1015 µs Register Retention Full Full Partial No No SRAM Retention Full Full Full No No XOSC HF or XOSC HF or High-Speed Clock Off Off Off RCOSC HF RCOSC HF XOSC LF or XOSC LF or XOSC LF or Low-Speed Clock Off Off RCOSC LF RCOSC LF RCOSC LF Peripherals Available Available Off Off Off Sensor Controller Available Available Available Off Off Available Off Wake up on RTC Available Available Off Wake up on Pin Edge Available Available Available Available Off Wake up on Reset Pin Available Available Available Available Available Brown Out Detector (BOD) Active Off N/A Active **Duty Cycled** Power On Reset (POR) Active Active Active Active N/A

Table 8-2. Power Modes

(1) Not including RTOS overhead

In active mode, the application Cortex-M3 CPU is actively executing code. Active mode provides normal operation of the processor and all of the peripherals that are currently enabled. The system clock can be any available clock source (see Table 8-2).

In idle mode, all active peripherals can be clocked, but the Application CPU core and memory are not clocked and no code is executed. Any interrupt event will bring the processor back into active mode.

In standby mode, only the always-on domain (AON) is active. An external wake event, RTC event, or sensor-controller event is required to bring the device back to active mode. MCU peripherals with retention do not need to be reconfigured when waking up again, and the CPU continues execution from where it went into standby mode. All GPIOs are latched in standby mode.

In shutdown mode, the device is turned off entirely, including the AON domain and the Sensor Controller. The I/Os are latched with the value they had before entering shutdown mode. A change of state on any I/O pin defined as a *wake from Shutdown pin* wakes up the device and functions as a reset trigger. The CPU can differentiate between a reset in this way, a reset-by-reset pin, or a power-on-reset by reading the reset status register. The only state retained in this mode is the latched I/O state and the Flash memory contents.

The Sensor Controller is an autonomous processor that can control the peripherals in the Sensor Controller independently of the main CPU, which means that the main CPU does not have to wake up, for example, to execute an ADC sample or poll a digital sensor over SPI. The main CPU saves both current and wake-up time that would otherwise be wasted. The Sensor Controller Studio enables the user to configure the sensor controller and choose which peripherals are controlled and which conditions wake up the main CPU.



8.8 Clock Systems

The CC2640R2F-Q1 device supports two external and two internal clock sources.

A 24MHz crystal is required as the frequency reference for the radio. This signal is doubled internally to create a 48MHz clock.

The 32kHz crystal is optional. *Bluetooth* [®] low energy requires a slow-speed clock with better than ±500 ppm accuracy if the device is to enter any sleep mode while maintaining a connection. The internal 32kHz RC oscillator can, in some use cases, be compensated to meet the requirements. The low-speed crystal oscillator is designed for use with a 32kHz watch-type crystal.

The internal high-speed oscillator (48MHz) can be used as a clock source for the CPU subsystem.

The internal low-speed oscillator (32.768kHz) can be used as a reference if the low-power crystal oscillator is not used.

The 32kHz clock source can be used as an external clocking reference through GPIO.

8.9 General Peripherals and Modules

The I/O controller controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a flexible manner. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull or open-drain. Five GPIOs have high drive capabilities (marked in **bold** in Section 6).

The SSIs are synchronous serial interfaces that are compatible with SPI, MICROWIRE, and synchronous serial interfaces from Texas Instruments[™]. The SSIs support both SPI master and slave up to 4 MHz.

The UART implements a universal asynchronous receiver/transmitter function. It supports flexible baud-rate generation up to a maximum of 3 Mbps and is compatible with the *Bluetooth* [®] HCl specifications.

Timer 0 is a general-purpose timer module (GPTM), which provides two 16-bit timers. The GPTM can be configured to operate as a single 32-bit timer, dual 16-bit timers or as a PWM module.

Timer 1, Timer 2, and Timer 3 are also GPTMs. Each of these timers is functionally equivalent to Timer 0.

In addition to these four timers, the RF core has its own timer to handle timing for RF protocols; the RF timer can be synchronized to the RTC.

The I^2C interface is used to communicate with devices compatible with the I^2C standard. The I^2C interface is capable of 100kHz and 400kHz operation, and can serve as both I^2C master and I^2C slave.

The TRNG module provides a true, nondeterministic noise source for the purpose of generating keys, initialization vectors (IVs), and other random number requirements. The TRNG is built on 24 ring oscillators that create unpredictable output to feed a complex nonlinear combinatorial circuit.

The watchdog timer is used to regain control if the system fails due to a software error after an external device fails to respond as expected. The watchdog timer can generate an interrupt or a reset when a predefined time-out value is reached.

The device includes a direct memory access (μ DMA) controller. The μ DMA controller provides a way to offload data transfer tasks from the Cortex-M3 CPU, allowing for more efficient use of the processor and the available bus bandwidth. The μ DMA controller can perform transfer between memory and peripherals. The μ DMA controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory as the peripheral is ready to transfer more data. Some features of the μ DMA controller include the following (this is not an exhaustive list):

- Highly flexible and configurable channel operation of up to 32 channels
- Transfer modes:
 - Memory-to-memory
 - Memory-to-peripheral
 - Peripheral-to-memory
 - Peripheral-to-peripheral
- Data sizes of 8, 16, and 32 bits

The AON domain contains circuitry that is always enabled, except in Shutdown mode (where the digital supply is off). This circuitry includes the following:

- The RTC can be used to wake the device from any state where it is active. The RTC contains three compare
 and one capture registers. With software support, the RTC can be used for clock and calendar operation. The
 RTC is clocked from the 32kHz RC oscillator or crystal. The RTC can also be compensated to tick at the
 correct frequency even when the internal 32kHz RC oscillator is used instead of a crystal.
- The battery monitor and temperature sensor are accessible by software and give a battery status indication as well as a coarse temperature measure.

8.10 System Architecture

Depending on the product configuration, the CC2640R2F-Q1 device can function either as a wireless network processor (WNP—a device running the wireless protocol stack with the application running on a separate MCU), or as a system-on-chip (SoC), with the application and protocol stack running on the Arm Cortex-M3 core inside the device.

In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.

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9 Application, Implementation, and Layout

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

Very few external components are required for the operation of the CC2640R2F-Q1 device. This section provides general information about the differential configuration when using the CC2640R2F-Q1 device in an application, and an example application circuit with schematics and layout is shown in Figure 9-1, Figure 9-2, Figure 9-3, and Figure 9-4. This is only a small selection of the many application circuit examples available as complete reference designs from the product folder on www.ti.com.

Figure 9-1 shows the differential RF front-end configuration option with internal biasing. See the CC2640Q1EM-7ID reference design for this option.

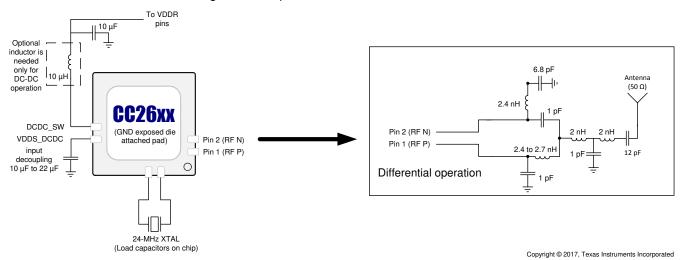


Figure 9-1. CC2640R2F-Q1 Application Circuit

Figure 9-2 shows the various supply voltage configuration options for the CC2640R2F-Q1 device. Not all power supply decoupling capacitors or digital I/Os are shown. For a detailed overview of power supply decoupling and wiring, see the TI reference designs and the CC13x0, CC26x0 SimpleLink Wireless MCU Technical Reference Manual.

Internal DC-DC Regulator

Internal LDO Regulator

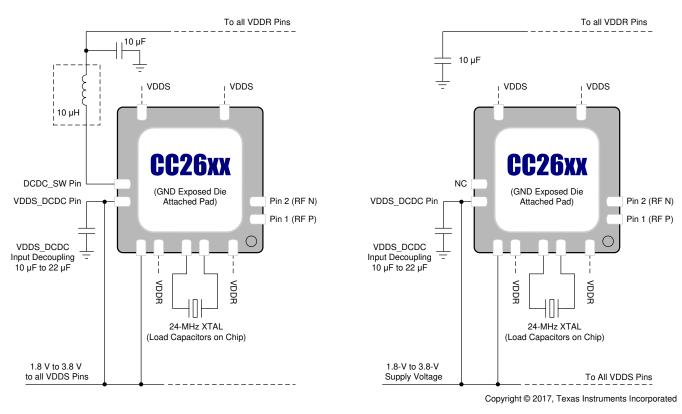


Figure 9-2. Supply Voltage Configurations



9.2 7 × 7 Internal Differential (7ID) Application Circuit

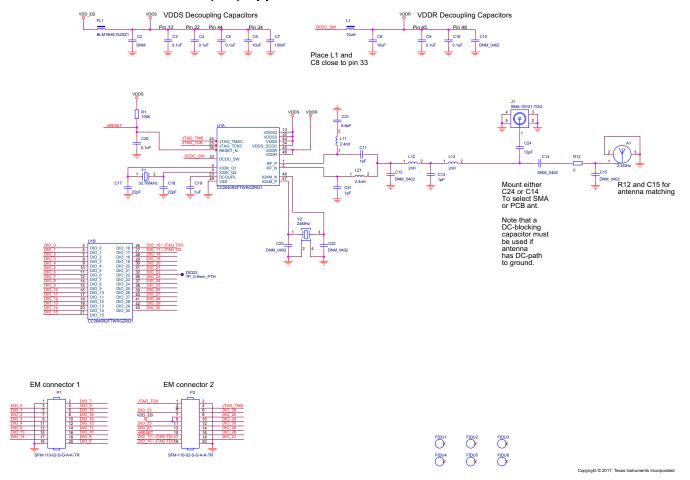


Figure 9-3. 7 × 7 Internal Differential (7ID) Application Circuit

Product Folder Links: CC2640R2F-Q1

34



9.2.1 Layout

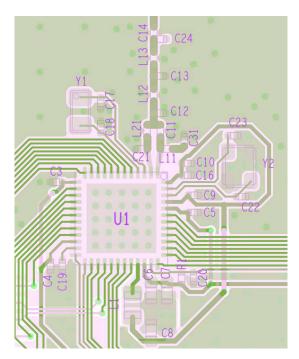


Figure 9-4. Layout

10 Device and Documentation Support

10.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to all part numbers and date-code. Each device has one of three prefixes/identifications: X, P, or null (no prefix) (for example, CC2640R2F-Q1 is in production; therefore, no prefix/identification is assigned).

Device development evolutionary flow:

- **X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
- **P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Production devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. Tl's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, *RGZ*).

For orderable part numbers of the *CC2640R2F-Q1* device package types, see the Package Option Addendum of this document, the TI website (www.ti.com), or contact your TI sales representative.

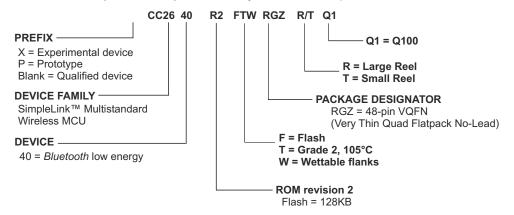


Figure 10-1. Device Nomenclature

Product Folder Links: CC2640R2F-Q1

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10.2 Tools and Software

TI offers an extensive line of development tools, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development of the CC2640R2F-Q1 device applications:

Software Tools:

SmartRF Studio 7 is a PC application that helps designers of radio systems to easily evaluate the RF-IC at an early stage in the design process.

- Test functions for sending and receiving radio packets, continuous wave transmit and receive
- · Evaluate RF performance on custom boards by wiring it to a supported evaluation board or debugger
- Can also be used without any hardware, but then only to generate, edit and export radio configuration settings
- Can be used in combination with several development kits for TI's CCxxxx RF-ICs

Sensor Controller Studio provides a development environment for the CC26xx Sensor Controller. The Sensor Controller is a proprietary, power-optimized CPU in the CC26xx, which can perform simple background tasks autonomously and independent of the System CPU state.

- Allows for Sensor Controller task algorithms to be implemented using a C-like programming language
- Outputs a Sensor Controller Interface driver, which incorporates the generated Sensor Controller machine code and associated definitions
- Allows for rapid development by using the integrated Sensor Controller task testing and debugging functionality. This allows for live visualization of sensor data and algorithm verification.

IDEs and Compilers:

Code Composer Studio[™] Integrated Development Environment (IDE):

- Integrated development environment with project management tools and editor
- Code Composer Studio (CCS) 6.1 and later has built-in support for the CC26xx device family
- Best support for XDS debuggers; XDS100v3, XDS110 and XDS200
- High integration with TI-RTOS with support for TI-RTOS Object View

IAR Embedded Workbench® for Arm®:

- · Integrated development environment with project management tools and editor
- IAR EWARM 7.30.3 and later has built-in support for the CC26xx device family
- Broad debugger support, supporting XDS100v3, XDS200, IAR I-Jet and Segger J-Link
- Integrated development environment with project management tools and editor
- RTOS plugin available for TI-RTOS

For a complete listing of development-support tools for the CC2640R2F-Q1 platform, visit the Texas Instruments website at www.ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.



10.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com (CC2640R2F-Q1). In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the CC2640R2F-Q1 devices, related peripherals, and other technical collateral is listed in the following.

Technical Reference Manual

CC13x0, CC26x0 SimpleLink™ Wireless MCU Technical Reference Manual

Errata

CC2640R2F-Q1 SimpleLink™ Wireless MCU Errata

10.4 Texas Instruments Low-Power RF Website

Texas Instruments' Low-Power RF website has all the latest products, application and design notes, FAQ section, news and events updates. Go to www.ti.com/lprf.

10.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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10.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.8 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

10.9 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.



11 Revision History

| Changes from Revision B (October 2020) to Revision C (March 2025) | Page | | | | | |
|--|----------------|--|--|--|--|--|
| Added recommended GPIO Input Voltage in Recommended Operating Conditions | | | | | | |
| Changes from Revision A (August 2017) to Revision B (October 2020) | Page | | | | | |
| Updated the numbering for sections, tables, figures, and cross-references throughout the doc | cument 1 | | | | | |
| Changed Development Tools and Software in Section 1 | 1 | | | | | |
| Changed Section 2 | | | | | | |
| Changed Section 3 | | | | | | |
| Added note to Section 7.1 about injection current and associated this note with the "Voltage of the control of th | on any digital | | | | | |
| pin" specification | | | | | | |
| Removed the flash write time specification's association with note 2 in Section 7.5 | | | | | | |
| Added "Zero cycles" as the test condition for flash page/sector erase time in Section 7.5 | 11 | | | | | |
| Added new flash page/sector erase time at 30 000 cycles in Section 7.5 | 11 | | | | | |



12 Mechanical, Packaging, and Orderable Information

12.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

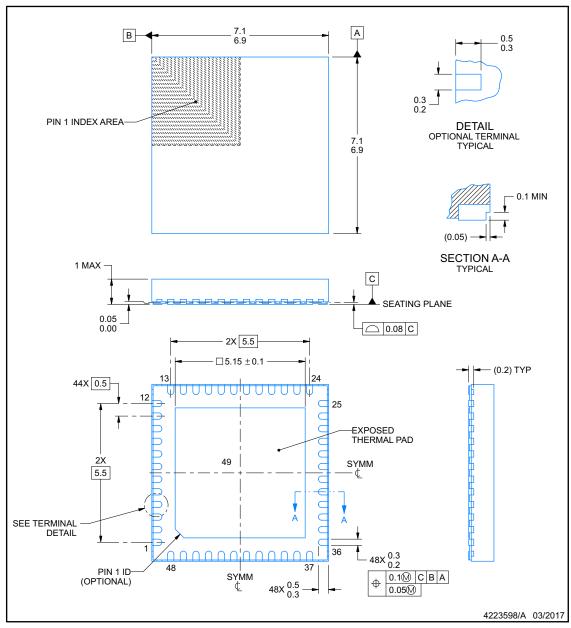


RGZ0048N

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.





EXAMPLE BOARD LAYOUT

RGZ0048N

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD $(\Box 5.15)$ SYMM 48X (0.6) 36 48X (0.25) 6X (1.065)0 0 0 44X (0.5) 10X (1.26)49 SYMM (6.8)(R0.05) (Ø 0.2) TYP VIA 12 24 6X (1.065) 10X (1.26) (6.8)LAND PATTERN EXAMPLE EXPOSED METAL SHOWN SCALE:12X 0.07 MAX 0.07 MIN ALL AROUND ALL AROUND SOLDER MASK -MFTAI **OPENING EXPOSED METAL EXPOSED METAL** SOLDER MASK METAL UNDER **OPENING** SOLDER MASK NON SOLDER MASK SOLDER MASK DEFINED DEFINED (PREFERRED) SOLDER MASK DETAILS

NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



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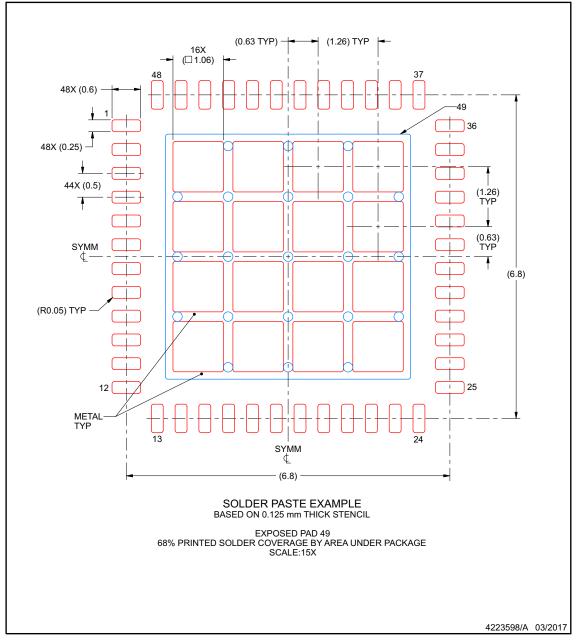


EXAMPLE STENCIL DESIGN

RGZ0048N

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



www.ti.com 7-Nov-2025

PACKAGING INFORMATION

| Orderable part number | Status | Material type | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material | MSL rating/ Peak reflow | Op temp (°C) | Part marking (6) |
|-----------------------|--------|---------------|-----------------|-----------------------|----------|-------------------------------|----------------------------|--------------|------------------|
| | | | | | | (4) | (5) | | |
| CC2640R2FTWRGZRQ1 | Active | Production | VQFN (RGZ) 48 | 2500 LARGE T&R | Yes | Call TI Sn | Level-3-260C-168 HR | -40 to 105 | CC2640Q1 R2F |
| CC2640R2FTWRGZRQ1.A | Active | Production | VQFN (RGZ) 48 | 2500 LARGE T&R | Yes | Call TI | Level-3-260C-168 HR | -40 to 105 | CC2640Q1 R2F |
| CC2640R2FTWRGZRQ1.B | Active | Production | VQFN (RGZ) 48 | 2500 LARGE T&R | Yes | Call TI | Level-3-260C-168 HR | -40 to 105 | CC2640Q1 R2F |
| CC2640R2FTWRGZTQ1 | Active | Production | VQFN (RGZ) 48 | 250 SMALL T&R | Yes | Call TI Sn | Level-3-260C-168 HR | -40 to 105 | CC2640Q1 R2F |
| CC2640R2FTWRGZTQ1.A | Active | Production | VQFN (RGZ) 48 | 250 SMALL T&R | Yes | Call TI | Level-3-260C-168 HR | -40 to 105 | CC2640Q1 R2F |
| CC2640R2FTWRGZTQ1.B | Active | Production | VQFN (RGZ) 48 | 250 SMALL T&R | Yes | Call TI | Level-3-260C-168 HR | -40 to 105 | CC2640Q1 R2F |

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

www.ti.com 7-Nov-2025

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OTHER QUALIFIED VERSIONS OF CC2640R2F-Q1:

Catalog : CC2640R2F

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

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