System-on-Chip for 2.4-GHz USB Applications

FEATURES

- RF section
  - Single-Chip 2.4-GHz RF Transceiver and MCU
  - Data Rates and Modulation Formats:
    - 2-Mbps GFSK, 320-kHz Deviation
    - 2-Mbps GFSK, 500-kHz Deviation
    - 1-Mbps GFSK, 160-kHz Deviation
    - 1-Mbps GFSK, 250-kHz Deviation
    - 500-kbps MSK
    - 250-kbps GFSK, 160-kHz Deviation
    - 250-kbps MSK
  - Excellent Link Budget, Enabling Long Range Without External Front-Ends
  - Programmable Output Power up to 4 dBm
  - Excellent Receiver Sensitivity (–88 dBm at 2 Mbps)
  - Suitable for Systems Targeting Compliance With Worldwide Radio Frequency Regulations: ETSI EN 300 328 and EN 300 440 Category 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan)
  - Accurate RSSI Function
- Layout
  - Few External Components
  - Reference Designs Available
  - 32-pin 5-mm × 5-mm QFN (8 General I/O Pins) Package
- Low Power
  - Active Mode RX: 22.5 mA
  - Active Mode TX (0 dBm): 27 mA
  - Power Mode 1 (4-µs Wake-Up): 1 mA
  - Wide Supply-Voltage Range
    - 3.3V LDO Output
    - Supply Range: 2 V–3.6 V
    - USB 5-V Regulator: 4 V–5.45 V
- Microcontroller
  - High-Performance and Low-Power 8051 Microcontroller Core With Code Prefetch
  - 32-KB Flash Program Memory
  - 2 KB SRAM
  - Hardware Debug Support
  - Extensive Baseband Automation, Including Auto-Acknowledgement and Address Decoding
- Peripherals
  - Full Speed USB 2.0
    - 6 Endpoints (Endpoint 0 and 5 IN/OUT Endpoints)
    - Internal Pullup for D+
    - 5-V to 3.3-V Regulator
  - Powerful Two-Channel DMA
  - General-Purpose Timers (One 16-Bit, Two 8-Bit)
  - Radio Timer, 40-Bit
  - IR Generation Circuitry
  - Several Oscillators:
    - 32-MHz XOSC
    - 16-MHz RCOSC
    - 32-kHz RCOSC
  - 32-kHz Sleep Timer With Capture
  - AES Security Coprocessor
  - UART/SPI Serial Interface
  - 8 General-Purpose I/O pins (6 × 4-mA and 2 × 20-mA Drive Strength)
  - Watchdog Timer
  - True Random-Number Generator

APPLICATIONS

- Proprietary 2.4-GHz Systems
- Human Interface Devices (USB Dongle)
- Consumer Electronics

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION

The CC2544 is an optimized system-on-chip (SoC) solution for USB applications with datarates upto 2Mbps built with low bill-of-material cost. The CC2544 combines the excellent performance of a leading RF transceiver with a single-cycle 8051 compliant CPU, 32-KB in-system programmable flash memory, up to 2-KB RAM, and many other powerful features.

The CC2544 is compatible with the CC2541/CC2543/CC2545. It comes in a 5-mm × 5-mm QFN32 package, with SPI/UART/USB interface. The CC2544 comes complete with reference designs from Texas Instruments.

The devices target wireless consumer and HID applications. The CC2544 is ideal for USB dongle applications.

For block diagram, see Figure 7

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Supply voltage VBUS		–0.3	5.5	V
Supply voltage VDD	All supply pins must have the same voltage	–0.3	≤3.9	V
Voltage on any digital pin		–0.3	≤3.9	V
Input RF level			10	dBm
Storage temperature range		–40	125	°C
ESD(2)	All pins, according to human-body model, JEDEC STD 22, method A114 (HBM)		2	kV
	According to charged-device model, JEDEC STD 22, method C101 (CDM)		750	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) **CAUTION**: ESD sensitive device. Precautions should be used when handing the device in order to prevent permanent damage.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Operating ambient temperature range, T_A		–40	85	°C
Operating supply voltage VBUS	Optional to use this regulator	4	5.45	V
Operating supply voltage VDD	All supply pins must have same voltage	2	3.6	V

ELECTRICAL CHARACTERISTICS

Measured on Texas Instruments CC2544EM reference design with T_A = 25°C and VDD = 3.3 V, VBUS tied to 5 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
2 Mbps, GFSK, 320-kHz Deviation, 0.1% BER					
I_{core}– Core current consumption	RX mode, no peripherals active, low MCU activity		22.5		mA
	TX mode, 0-dBm output power, no peripherals active, low MCU activity		27		mA
	TX mode, 4-dBm output power, no peripherals active, low MCU activity		30		mA
	Active mode, 16-MHz RCOSC, Low MCU activity		4		mA
	Active mode, 32-MHz clock frequency, low MCU activity		7		mA
	Power mode 0, CPU clock halted, all peripherals on, no clock division, 32-MHz crystal selected		6		mA
	Power mode 0, CPU clock halted, all peripherals on, clock division at max. (Limits max. speed in peripherals except radio), 32-MHz crystal selected		3.5		mA
	Power mode 1. Digital regulator on; 16-MHz RCOSC and 32-MHz crystal oscillator off; 32.753-kHz RCOSC, POR, BOD, and sleep timer active; RAM and register retention		1		mA
I_{peri}– Peripheral current consumption (Adds to core current I_{core} for each peripheral unit activated)	Timer 1 (16-bit). Timer running, 32-MHz XOSC used		90		µA
	Radio timer(40 bit). Timer running, 32-MHz XOSC used		90		µA
	Timer 3 (8-bit). Timer running, 32-MHz XOSC used		60		µA
	Timer 4 (8-bit). Timer running, 32-MHz XOSC used		70		µA
	Sleep timer. Including 32.753-kHz RCOSC		0.6		µA

GENERAL CHARACTERISTICS

Measured on Texas Instruments CC2544EM reference design with T_A = 25°C and VDD = 3.3 V, VBUS tied to 5 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
WAKE-UP AND TIMING					
Power mode 1 → Active	Digital regulator on, 16-MHz RCOSC and 32-MHz crystal oscillator off. Start-up of 16-MHz RCOSC.		4		µs
Active → TX or RX	Crystal ESR = 16 Ω. Initially running on 16-MHz RCOSC, with 32-MHz XOSC OFF.		410		µs
	With 32-MHz XOSC initially on.		160		µs
RX/TX turnaround			130		µs
RADIO PART					
RF frequency range	Programmable in 1-MHz steps	2380		2495	MHz
Data rates and modulation formats	2 Mbps, GFSK 320-kHz deviation 2-Mbps, GFSK 500 kHz deviation 1-Mbps, GFSK 160 kHz deviation 1-Mbps, GFSK 250 kHz deviation 500 kbps, MSK 250 kbps, GFSK 160 kHz deviation 250 kbps, MSK				

RF RECEIVE SECTION

Measured on Texas Instruments CC2544EM reference design with T_A = 25°C, VDD = 3.3 V, VBUS tied to 5 V, and f_C = 2440 MHz, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
2 Mbps, GFSK, 320-kHz Deviation, 0.1% BER					
Receiver sensitivity			–84		dBm
Saturation(1)			0		dBm
Co-channel rejection	Wanted signal at -67 dBm		–15		dB
In-band blocking rejection	±2-MHz offset, wanted signal –67 dBm		–5		dB
	±4-MHz offset, wanted signal –67 dBm		30		
	±6-MHz offset, wanted signal –67 dBm		40		
	>12-MHz offset, wanted signal –67 dBm		42		
Out-of-band blocking rejection	1-MHz resolution. Wanted signal –67 dBm, f < 2 GHz Two exception frequencies with poorer performance		–35		dBm
	1-MHz resolution. Wanted signal –67 dBm, 2 GHz > f < 3 GHz Two exception frequencies with poorer performance		–36		
	1-MHz resolution. Wanted signal –67 dBm, f > 3GHz Two exception frequencies with poorer performance		–12		
Intermodulation	Wanted signal –64 dBm, 1st interferer is CW, 2nd interferer is GFSK-modulated signal. Offsets of interferers are: 6 and 12 MHz 8 and 16 MHz 10 and 20 MHz		–43		dBm
Frequency error tolerance(2)	Including both initial tolerance and drift. Limit set to minimum sensitivity of –70dBm, 250K byte payload	–300		300	kHz
Symbol rate error tolerance(3)	Limit set to minimum sensitivity of –70 dBm, 250K byte payload	–120		120	ppm
2 Mbps, GFSK, 500-kHz Deviation, 0.1% BER					
Receiver sensitivity			–88		dBm
Saturation(1)			3		dBm
Co-channel rejection	Wanted signal at -67 dBm		-9		dB
In-band blocking rejection	±2-MHz offset, wanted signal –67 dBm		-3		dB
	±4-MHz offset, wanted signal –67 dBm		33		
	±6-MHz offset, wanted signal –67 dBm		49		
	>12-MHz offset, wanted signal –67 dBm		40		
Frequency error tolerance(2)	Including both initial tolerance and drift. Sensitivity better than –70 dBm. 250-byte payload	–300		300	kHz
Symbol-rate error tolerance(3)	Sensitivity better than –70 dBm. 250-byte payload	–120		120	ppm
1 Mbps, GFSK, 250-kHz Deviation, 0.1% BER					
Receiver sensitivity			-91		dBm
Saturation(1)			5		dBm
Co-channel rejection	Wanted signal at –67 dBm		-6		dB
In-band blocking rejection	±2-MHz offset, wanted signal –67 dBm		28		dB
	±4-MHz offset, wanted signal –67 dBm		31		
	±6-MHz offset, wanted signal –67 dBm		40		
	>12-MHz offset, wanted signal –67 dBm		49		
Frequency error tolerance(2)	Including both initial tolerance and drift. Sensitivity better than –70 dBm. 250-byte payload	–250		250	kHz
Symbol-rate error tolerance(3)	Sensitivity better than –70 dBm. 250-byte payload	–80		80	ppm

(1) AGC enabled
(2) Difference between center frequency of the received RF signal and local oscillator frequency
(3) Difference between incoming symbol rate and the internally generated symbol rate

RF RECEIVE SECTION (continued)

Measured on Texas Instruments CC2544EM reference design with T_A = 25°C, VDD = 3.3 V, VBUS tied to 5 V, and f_C = 2440 MHz, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
1 Mbps, GFSK, 160-kHz Deviation, 0.1% BER					
Receiver sensitivity			-87		dBm
Saturation(1)			5		dBm
Co-channel rejection	Wanted signal at -67 dBm		-9		dB
In-band blocking rejection	±2-MHz offset, wanted signal –67 dBm		26		dB
	±4-MHz offset, wanted signal –67 dBm		30		
	±6-MHz offset, wanted signal –67 dBm		40		
	>12-MHz offset, wanted signal –67 dBm		46		
Frequency error tolerance(2)	Including both initial tolerance and drift. Sensitivity better than –70 dBm. 250-byte payload	–250		250	kHz
Symbol-rate error tolerance(3)	Sensitivity better than –70 dBm. 250-byte payload	–80		80	ppm
500 kbps, MSK, 0.1% BER					
Receiver sensitivity			-96		dBm
Saturation(4)			5		dBm
Co-channel rejection	Wanted signal at -67 dBm		-5		dB
In-band blocking rejection	±2-MHz offset, wanted signal –67 dBm		31		dB
	±4-MHz offset, wanted signal –67 dBm		31		
	±6-MHz offset, wanted signal –67 dBm		45		
	>12-MHz offset, wanted signal –67 dBm		54		
Frequency error tolerance(5)	Including both initial tolerance and drift. Sensitivity better than –70 dBm. 250-byte payload	–150		150	kHz
Symbol-rate error tolerance(6)	Sensitivity better than –70 dBm. 250-byte payload	–60		60	ppm

(4) AGC enabled
(5) Difference between center frequency of the received RF signal and local oscillator frequency
(6) Difference between incoming symbol rate and the internally generated symbol rate

RF RECEIVE SECTION (continued)

Measured on Texas Instruments CC2544EM reference design with T_A = 25°C, VDD = 3.3 V, VBUS tied to 5 V, and f_C = 2440 MHz, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
250 kbps, GFSK, 160-kHz Deviation, 0.1% BER					
Receiver sensitivity			-95		dBm
Saturation(7)			5		dBm
Co-channel rejection	Wanted signal at –67 dBm		-9		dB
In-band blocking rejection	±2-MHz offset, wanted signal –67 dBm		31		dB
	±4-MHz offset, wanted signal –67 dBm		31		
	±6-MHz offset, wanted signal –67 dBm		55		
	>12-MHz offset, wanted signal –67 dBm		53		
Frequency error tolerance(8)	Including both initial tolerance and drift. Sensitivity better than –70 dBm. 250-byte payload	–150		150	kHz
Symbol-rate error tolerance(9)	Sensitivity better than –70 dBm. 250-byte payload	–60		60	ppm
250 kbps, MSK, 0.1% BER					
Receiver sensitivity			–95		dBm
Saturation(7)			5		dBm
Co-channel rejection	Wanted signal at –67 dBm		–5		dB
In-band blocking rejection	±2-MHz offset, wanted signal –67 dBm		31		dB
	±4-MHz offset, wanted signal –67 dBm		31		
	±6-MHz offset, wanted signal –67 dBm		45		
	>12-MHz offset, wanted signal –67 dBm		54		
Frequency error tolerance(8)	Including both initial tolerance and drift. Sensitivity better than –70 dBm. 250-byte payload	–150		150	kHz
Symbol-rate error tolerance(9)	Sensitivity better than –70 dBm. 250-byte payload	–60		60	ppm
ALL RATES/FORMATS					
Spurious emission in RX. Conducted measurement	f < 1 GHz		–67		dBm
Spurious emission in RX. Conducted measurement	f > 1 GHz		–57		dBm

(7) AGC enabled
(8) Difference between center frequency of the received RF signal and local oscillator frequency
(9) Difference between incoming symbol rate and the internally generated symbol rate

RF TRANSMIT SECTION

Measured on Texas Instruments CC2544EM reference design with T_A = 25°C, VDD = 3.3 V, VBUS tied to 5 V, and f_C = 2440 MHz, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output power, maximum setting	Delivered to a single-ended 50-Ω load through a balun using maximum recommended output power setting.		4		dBm
Output power, minimum setting	Delivered to a single-ended 50-Ω load through a balun using minimum recommended output power setting.		–20		dBm
Programmable output power range	Delivered to a single-ended 50-Ω load through a balun.		24		dB
Spurious emission in TX. Conducted measurement.	f < 1 GHz		–46		dBm
Spurious emission in TX. Conducted measurement.	f > 1 GHz		–44		dBm
Optimum load impedance	Differential impedance as seen from the RF port (RF_P and RF_N) toward the antenna		70 + j30		Ω

32-MHz CRYSTAL OSCILLATOR

Measured on Texas Instruments CC2544EM reference design with T_A = 25°C, VDD = 3.3 V, VBUS tied to 5 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Crystal frequency			32		MHz
Crystal frequency accuracy requirement	2-Mbps data rate	–60		60	ppm
Equivalent series resistance		6		60	Ω
Crystal shunt capacitance		1		7	pF
Crystal load capacitance		10		16	pF
Start-up time			0.25		ms
Power-down guard time	The crystal oscillator must be in power down for a guard time before it is used again. This requirement is valid for all modes of operation. The need for power-down guard time can vary with crystal type and load.	3			ms

32-kHz RC OSCILLATOR

Measured on Texas Instruments CC2544EM reference design with T_A = 25°C, VDD = 3.3 V, VBUS tied to 5 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Calibrated frequency(1)			32.753		kHz
Frequency accuracy after calibration			±0.2%		
Temperature coefficient(2)			0.4		%/ºC
Supply-voltage coefficient(3)			3		%/V
Calibration time(4)			2		ms

(1) The calibrated 32-kHz RC oscillator frequency is the 32-MHz XTAL frequency divided by 977.
(2) Frequency drift when temperature changes after calibration
(3) Frequency drift when supply voltage changes after calibration
(4) The 32-kHz RC oscillator is calibrated when a switch from the 16-MHz RC oscillator to the 32-MHz crystal oscillator is performed, while SLEEPCMD.OSC32K_CALDIS is set to 0.

16-MHz RC OSCILLATOR

Measured on Texas Instruments CC2544EM reference design with T_A = 25°C, VDD = 3.3 V, VBUS tied to 5 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Calibrated frequency			16		MHz
Uncalibrated frequency accuracy			±18%		
Frequency accuracy after calibration(1)			±0.6%		
Start-up time			10		µs
Initial calibration time			50		µs

(1) The calibrated 16-MHz RC oscillator frequency is the 32-MHz XTAL frequency divided by 2.

RSSI CHARACTERISTICS

Measured on Texas Instruments CC2544 EM reference design with T_A = 25°C and VDD = 3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
2 Mbps, GFSK, 320-kHz Deviation, 0.1% BER and 2 Mbps, GFSK, 500-kHz Deviation, 0.1% BER					
RSSI range(1)			60		dB
RSSI offset(1)			97		dBm
Absolute uncalibrated accuracy(1)			±6		dB
Step size (LSB value)			1		dB
All Other Rates/Formats					
RSSI range(1)			60		dB
RSSI offset(1)			101		dBm
Absolute uncalibrated accuracy(1)			±3		dB
Step size (LSB value)			1		dB

(1) Assuming CC2544 EM reference design. Other RF designs give an offset from the reported value.

FREQUENCY SYNTHESIZER CHARACTERISTICS

Measured on Texas Instruments CC2544EM reference design with T_A = 25°C, VDD = 3.3 V, VBUS tied to 5 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase noise, unmodulated carrier	At ±1 MHz from carrier		–112		dBc/Hz
	At ±2 MHz from carrier		–119		
	At ±5 MHz from carrier		–124		

USB BUS 5-V to 3.3-V REGULATOR

Measured on Texas Instruments CC2544EM reference design with T_A = 25°C, VDD = 3.3 V, VBUS tied to 5 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage, typical minimum			4		V
Input voltage, typical maximum			5.45		V
Current limit			100		mA
Start-up time			0.8		ms
Output voltage			3.3		V

DC CHARACTERISTICS

Measured on Texas Instruments CC2544EM reference design with T_A = 25°C, VDD = 3.3 V, VBUS tied to 5 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic-0 input voltage				0.5	V
Logic-1 input voltage		2.5			V
Logic-0 input current		–50		50	nA
Logic-1 input current		–50		50	nA
I/O pin pullup and pulldown resistors			20		kΩ
Logic-0 output voltage 4-mA pins	Output load 4 mA			0.5	V
Logic-1 output voltage 4-mA pins	Output load 4 mA	2.4			V
Logic-0 output voltage 20-mA pins	Output load 20 mA			0.5	V
Logic-1 output voltage, 20-A pins	Outpu load 20 mA	2.4			V

CONTROL INPUT AC CHARACTERISTICS

T_A = –40°C to 85°C, VDD = 2 V to 3.6 V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System clock, f_{SYSCLK} t_{SYSCLK} = 1/ f_{SYSCLK}	The undivided system clock is 32 MHz when crystal oscillator is used. The undivided system clock is 16 MHz when calibrated 16-MHz RC oscillator is used.	16		32	MHz
RESET_N low duration	See item 1, Figure 1. This is the shortest pulse that is recognized as a complete reset pin request. Note that shorter pulses may be recognized but do not lead to complete reset of all modules within the chip.	1			µs
Interrupt pulse duration	See item 2, Figure 1.This is the shortest pulse that is recognized as an interrupt request.	20			ns

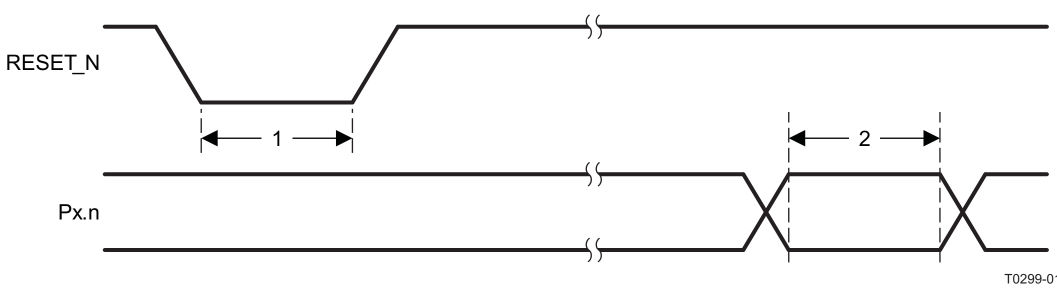


Figure 1. Control Input AC Characteristics

SPI AC CHARACTERISTICS

T_A = –40°C to 85°C, VDD = 2 V to 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	SCK period	Master, RX and TX	250			ns
		Slave, RX and TX	250			
	SCK duty cycle	Master		50%		
t_2	SSN low to SCK, Figure 2 and Figure 3	Master	63			ns
		Slave	63			
t_3	SCK to SSN high	Master	63			ns
		Slave	63			
t_4	MOSI early out	Master, load = 10 pF			7	ns
t_5	MOSI late out	Master, load = 10 pF			10	ns
t_6	MISO setup	Master	90			ns
t_7	MISO hold	Master	10			ns

SPI AC CHARACTERISTICS (continued)

T_A = –40°C to 85°C, VDD = 2 V to 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	SCK duty cycle	Slave		50%		ns
t_{10}	MOSI setup	Slave	35			ns
t_{11}	MOSI hold	Slave	10			ns
t_8	MISO early out	Slave, load = 10 pF			0	ns
t_9	MISO late out	Slave, load = 10 pF			95	ns
	Operating frequency	Master, TX only			8	MHz
		Master, RX and TX			4	
		Slave, RX only			8	
		Slave, RX and TX			4	

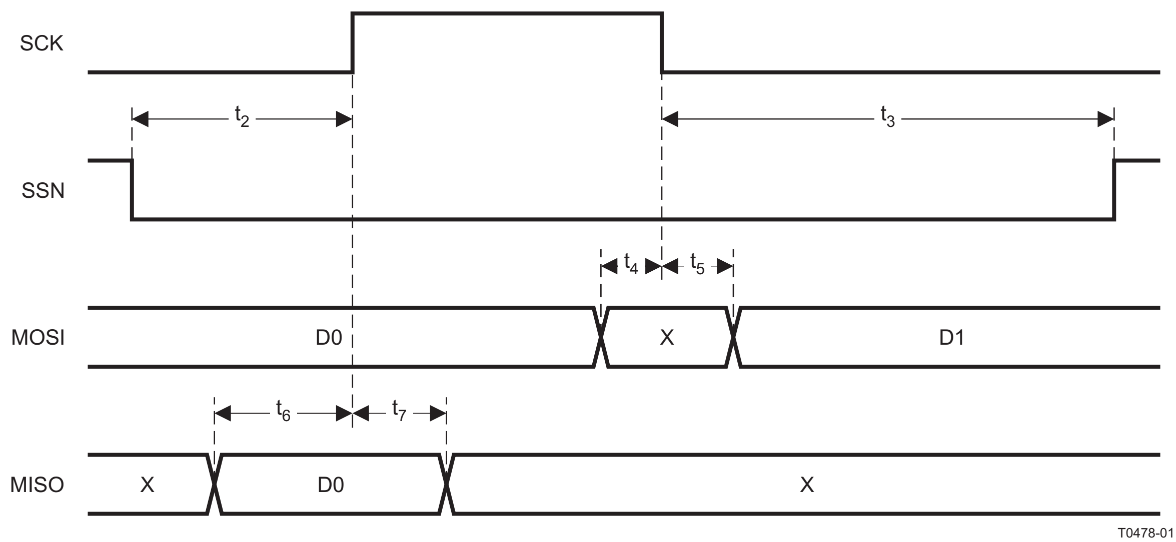


Figure 2. SPI Master AC Characteristics

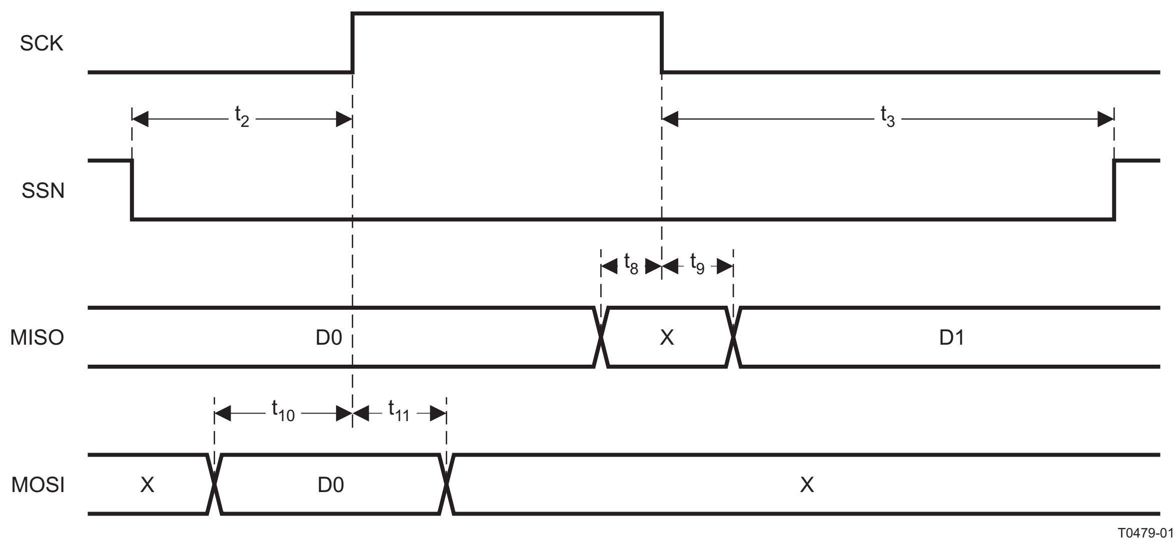


Figure 3. SPI Slave AC Characteristics

DEBUG INTERFACE AC CHARACTERISTICS

T_A = –40°C to 85°C, VDD = 2 V to 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clk_dbg}	Debug clock frequency (see Figure 4)				12	MHz
t_1	Allowed high pulse on clock (see Figure 4)		35			ns
t_2	Allowed low pulse on clock (see Figure 4)		35			ns
t_3	EXT_RESET_N low to first falling edge on debug clock (see Figure 5)		167			ns
t_4	Falling edge on clock to EXT_RESET_N high (see Figure 5)		83			ns
t_5	EXT_RESET_N high to first debug command (see Figure 5)		83			ns
t_6	Debug data setup (see Figure 6)		2			ns
t_7	Debug data hold (see Figure 6)		4			ns
t_8	Clock-to-data delay (see Figure 6)	Load = 10 pF			30	ns

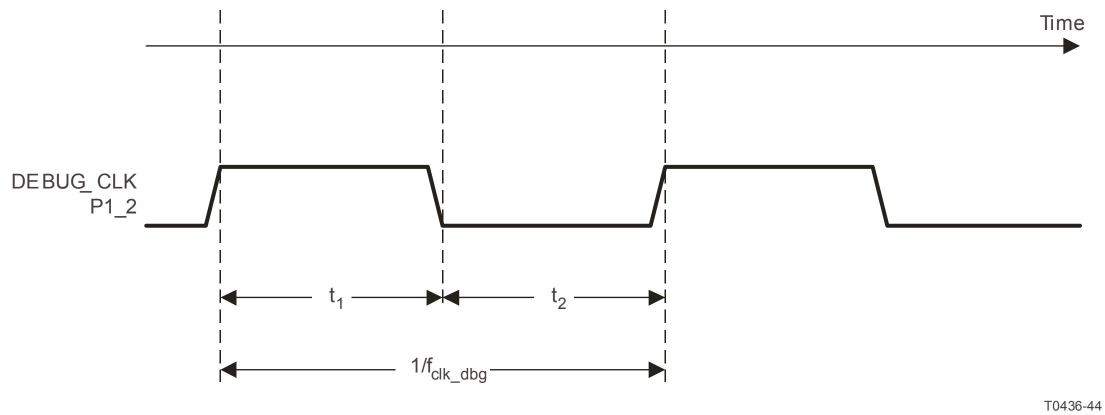


Figure 4. Debug Clock – Basic Timing

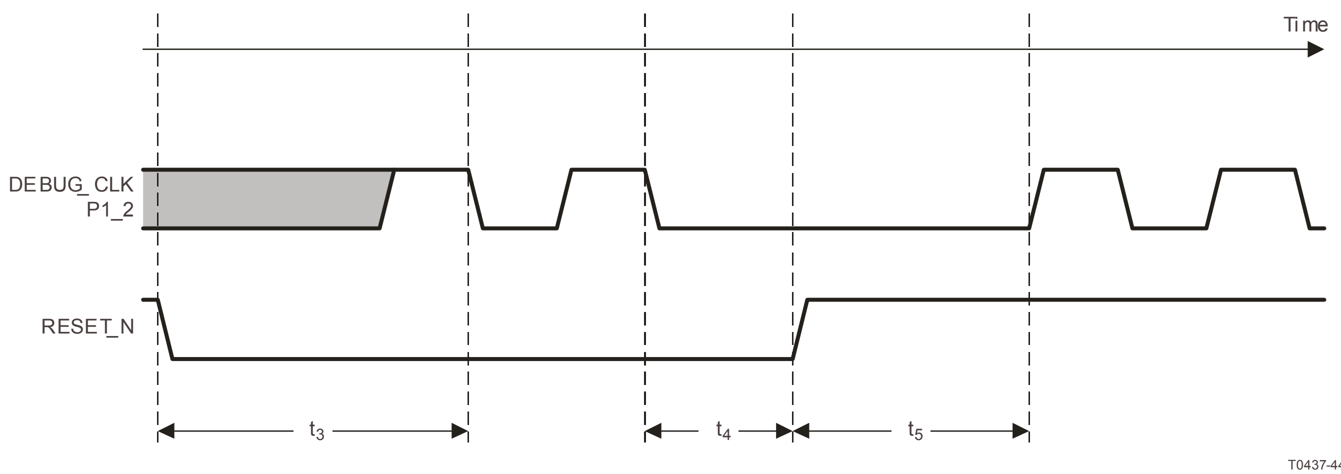


Figure 5. Debug Enable Timing

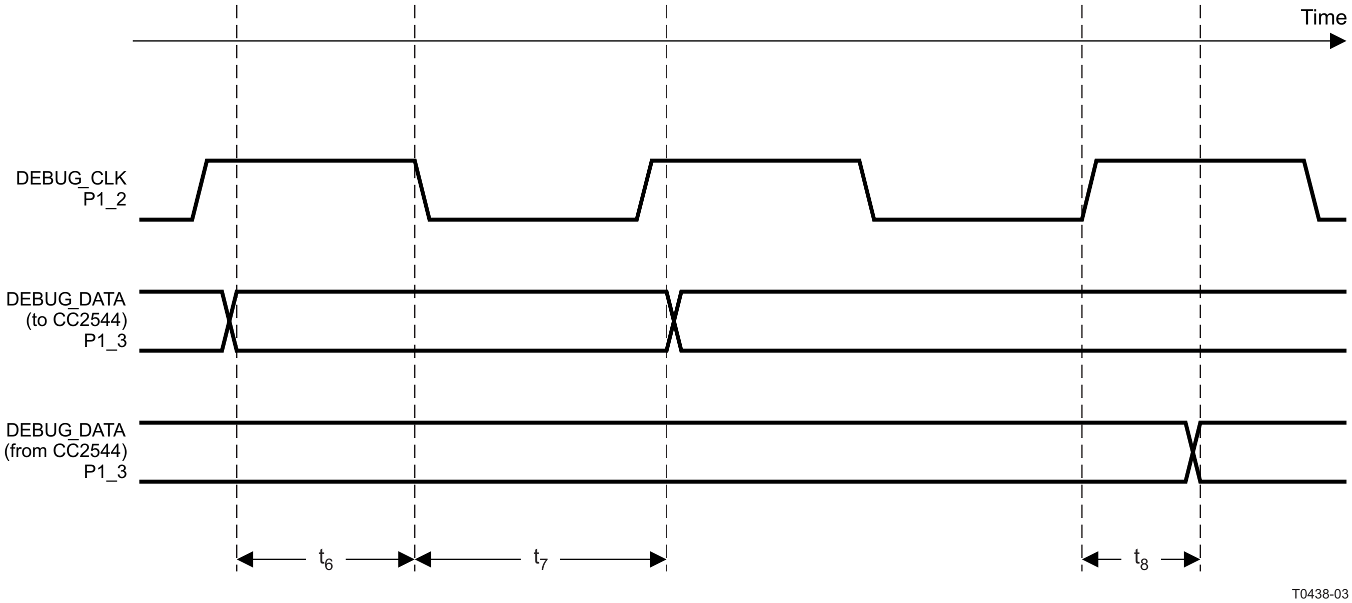


Figure 6. Data Setup and Hold Timing

TIMER INPUTS AC CHARACTERISTICS

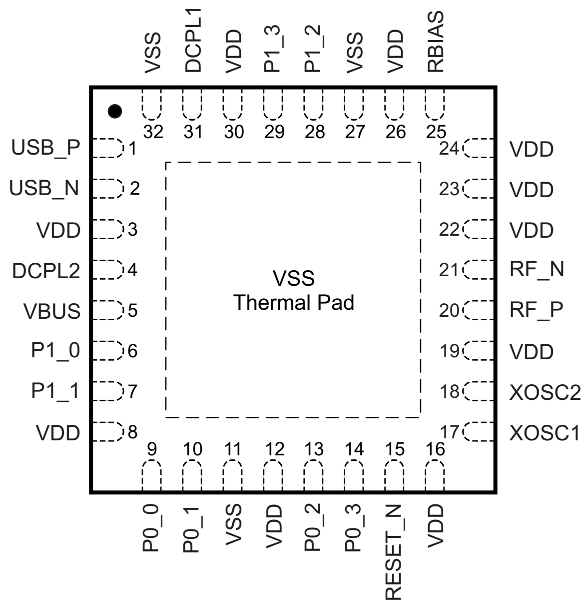
T_A = –40°C to 85°C, VDD = 2 V to 3.6 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input capture pulse duration	Synchronizers determine the shortest input pulse that can be recognized. The synchronizers operate at the current system clock rate (16 MHz or 32 MHz).	1.5			t_{SYSCLK}

DEVICE INFORMATION

PIN DESCRIPTIONS

CC2544
RHB Package
(Top View)



NOTE: The exposed ground pad must be connected to a solid ground plane; this is the **main** ground connection for the chip.

Table 1. Pin Description Table

NAME	PIN	DESCRIPTION
DCPL1	31	1.8-V reg. decouple
DCPL2	4	3.3-V reg. decouple
P0_0	9	GPIO
P0_1	10	GPIO
P0_2	13	GPIO
P0_3	14	GPIO
P1_0	6	GPIO/20 mA
P1_1	7	GPIO/20 mA
P1_2	28	GPIO/debug clock
P1_3	29	GPIO/debug data
RBIAS	25	External precision bias resistor for reference current
RESET_N	15	Reset, active-low
RF_N	21	Negative RF input signal to LNA during RX Negative RF output signal from PA during TX
RF_P	20	Positive RF input signal to LNA during RX Positive RF output signal from PA during TX
USB_P	1	USB module
USB_N	2	USB module
VBUS	5	5-V power
VDD	3	AVDD
VDD	8, 12	IOVDD
VDD	16, 19, 22, 23, 24	AVDD

Table 1. Pin Description Table (continued)

NAME	PIN	DESCRIPTION
VDD	26	AVDD_GUARD
VDD	30	IOVDD
VSS	11, 27	Optional IOVSS
VSS	32	USB ground
VSS	Ground pad	Must be connected to solid ground as this is the main ground connection for the chip.
XOSC1	17	32-MHz crystal oscillator pin 1or external-clock input
XOSC2	18	32-MHz crystal oscillator pin 2

BLOCK DIAGRAM

A block diagram of the CC2544 is shown in Figure 7. The modules can be roughly divided into one of three categories: CPU-related modules; modules related to power, test, and clock distribution; and radio-related modules. In the following subsections, a short description of each module is given. For more details, see the CC2543/44/45 User's Guide (SWRU283).

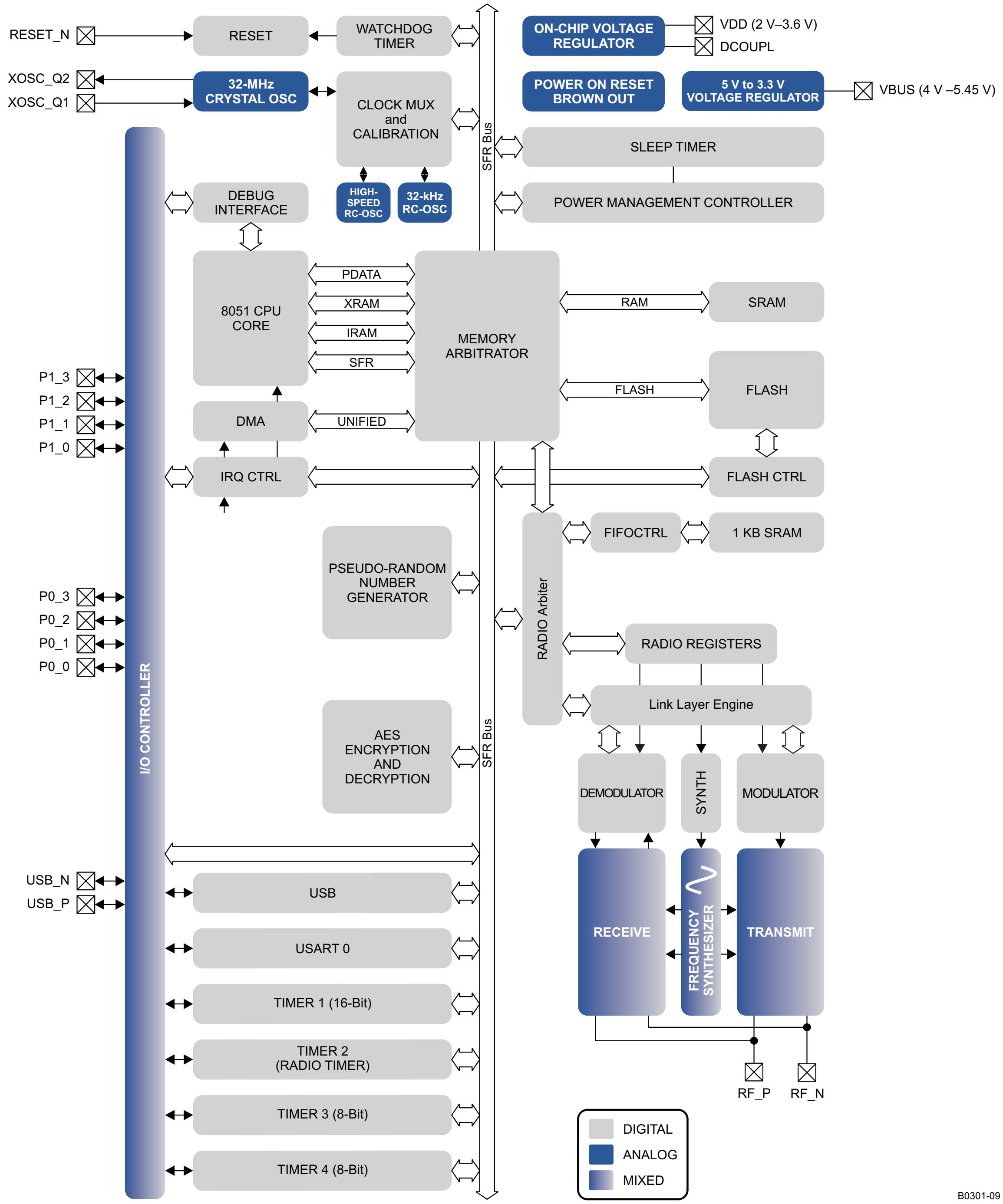


Figure 7. CC2544 Block Diagram

BLOCK DESCRIPTIONS

CPU and Memory

The **8051 CPU core** is a single-cycle 8051-compatible core. It has three different memory access busses (SFR, DATA, and CODE/XDATA), a debug interface, and an 15-input extended interrupt unit.

The **memory arbiter** is at the heart of the system, as it connects the CPU and DMA controller with the physical memories and all peripherals through the SFR bus. The memory arbiter has four memory-access points, access of which can map to one of three physical memories: an SRAM, flash memory, and XREG/SFR registers. It is responsible for performing arbitration and sequencing between simultaneous memory accesses to the same physical memory.

The **SFR bus** is drawn conceptually in Figure 7 as a common bus that connects all hardware peripherals to the memory arbiter. The SFR bus in the block diagram also provides access to the radio registers in the radio register bank, even though these are indeed mapped into XDATA memory space.

The **2-KB SRAM** maps to the DATA memory space and to parts of the XDATA memory spaces.

The **32-KB flash block** provides in-circuit programmable non-volatile program memory for the device, and maps into the CODE and XDATA memory spaces.

Peripherals

Writing to the flash block is performed through a **flash controller** that allows page-wise erasure and 4-bytewise programming. See User Guide for details on the flash controller.

A versatile two-channel **DMA controller** is available in the system, accesses memory using the XDATA memory space, and thus has access to all physical memories. Each channel (trigger, priority, transfer mode, addressing mode, source and destination pointers, and transfer count) is configured with DMA descriptors that can be located anywhere in memory. Many of the hardware peripherals (AES core, flash controller, USART, timers, etc.) can be used with the DMA controller for efficient operation by performing data transfers between a single SFR or XREG address and flash/SRAM.

The **interrupt controller** services a total of 15 interrupt sources, divided into six interrupt groups, each of which is associated with one of four interrupt priorities. Any interrupt service request is serviced also when the device is in idle mode by going back to active mode. Some interrupts can also wake up the device from sleep mode (when in sleep mode, the device is in low-power mode PM1).

The **debug interface** implements a proprietary two-wire serial interface that is used for in-circuit debugging. Through this debug interface, it is possible to perform an erasure of the entire flash memory, control which oscillators are enabled, stop and start execution of the user program, execute supplied instructions on the 8051 core, set code breakpoints, and single-step through instructions in the code. Using these techniques, it is possible to perform in-circuit debugging and external flash programming elegantly.

The **I/O controller** is responsible for all general-purpose I/O pins. The CPU can configure whether peripheral modules control certain pins or whether they are under software control, and if so, whether each pin is configured as an input or output and if a pullup or pulldown resistor in the pad is connected. Each peripheral that connects to the I/O pins can choose between several different I/O pin locations to ensure flexibility in various applications.

The **sleep timer** is an ultralow-power timer that uses an internal 32.753-kHz RC oscillator. The sleep timer runs continuously in all operating modes. Typical applications of this timer are as a real-time counter or as a wake-up timer to get out of power mode 1.

A built-in **watchdog timer** allows the CC2544 to reset itself if the firmware hangs. When enabled by software, the watchdog timer must be cleared periodically; otherwise, it resets the device when it times out.

Timer 1 is a 16-bit timer with timer/counter/PWM functionality. It has a programmable prescaler, a 16-bit period value, and five individually programmable counter/capture channels, each with a 16-bit compare value. Each of the counter/capture channels can be used as a PWM output or to capture the timing of edges on input signals. It can also be configured in IR generation mode, where it counts timer 3 periods and the output is ANDed with the output of timer 3 to generate modulated consumer IR signals with minimal CPU interaction.

Timer 2 is a 40-bit timer used by the Radio. It has a 16-bit counter with a configurable timer period and a 24-bit overflow counter that can be used to keep track of the number of periods that have transpired. A 40-bit capture register is also used to record the exact time at which a start-of-frame delimiter is received/transmitted or the exact time at which a packet ends. There are two 16-bit timer-compare registers and two 24-bit overflow-compare registers that can be used to give exact timing for start of RX or TX to the radio or general interrupts.

Timer 3 and timer 4 are 8-bit timers with timer/counter/PWM functionality. They have a programmable prescaler, an 8-bit period value, and one programmable counter channel with an 8-bit compare value. Each of the counter channels can be used as PWM output.

USART 0 is configurable as either an SPI master/slave or a UART. It provides double buffering on both RX and TX and hardware flow control and is thus well suited to high-throughput full-duplex applications. The USART has its own high-precision baud-rate generator, thus leaving the ordinary timers free for other uses. When configured as SPI slaves, the USART samples the input signal using SCK directly instead of using some oversampling scheme, and are thus well-suited for high data rates.

The **AES encryption/decryption core** allows the user to encrypt and decrypt data using the AES algorithm with 128-bit keys. The AES core also supports ECB, CBC, CFB, OFB, CTR, and CBC-MAC, as well as hardware support for CCM.

TYPICAL CHARACTERISTICS

RX CURRENT vs TEMPERATURE

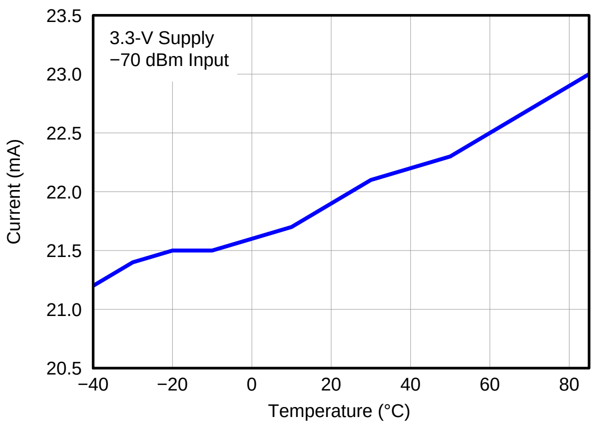


Figure 8.

TX CURRENT vs TEMPERATURE

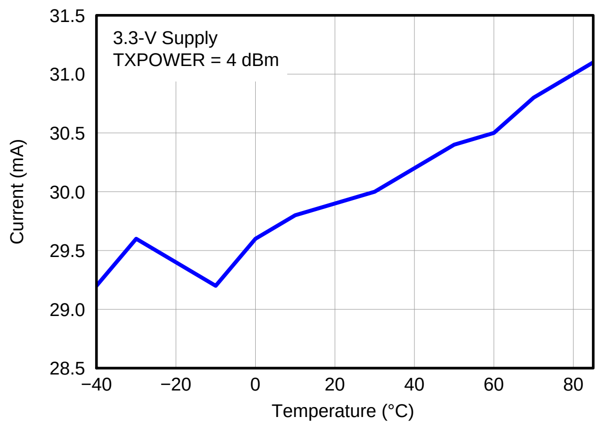


Figure 9.

RX SENSITIVITY vs TEMPERATURE

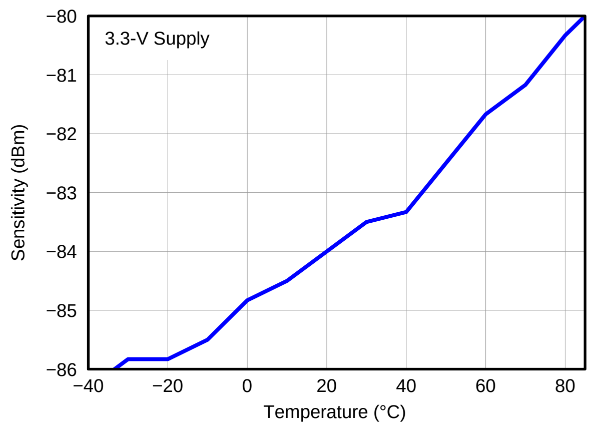


Figure 10.

TX POWER vs TEMPERATURE

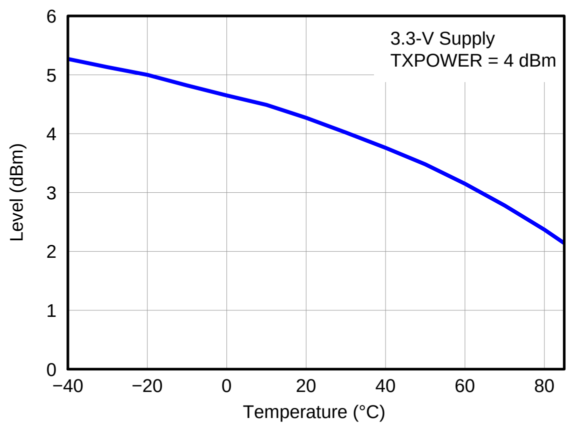


Figure 11.

TYPICAL CHARACTERISTICS (continued)

RX CURRENT vs SUPPLY VOLTAGE

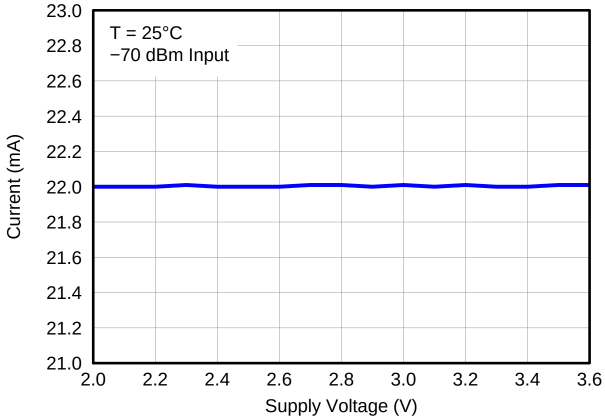


Figure 12.

TX CURRENT vs SUPPLY VOLTAGE

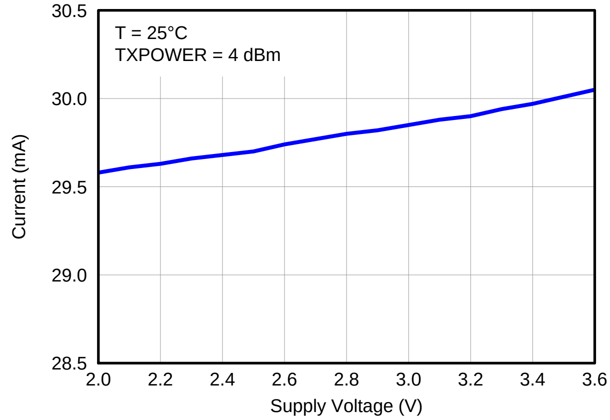


Figure 13.

RX SENSITIVITY vs SUPPLY VOLTAGE

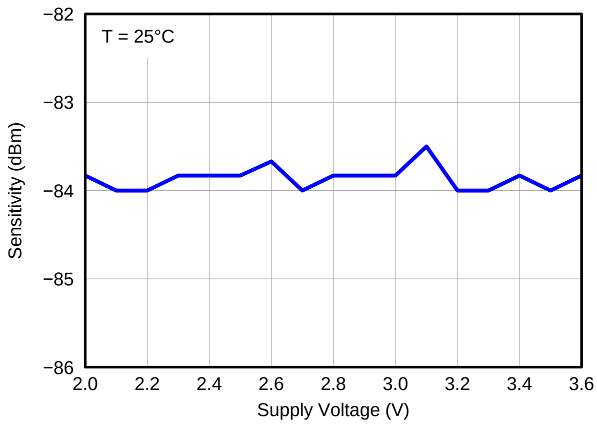


Figure 14.

TX POWER vs SUPPLY VOLTAGE

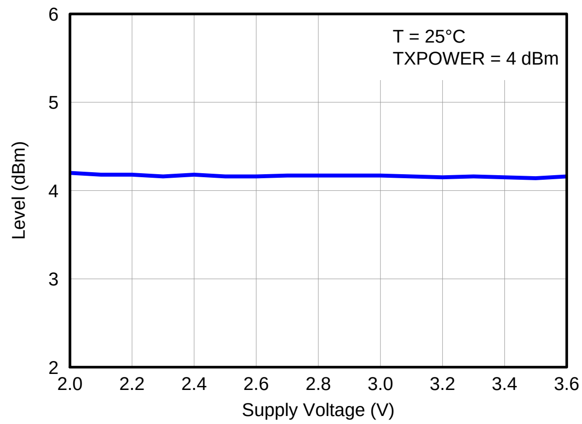


Figure 15.

TYPICAL CHARACTERISTICS (continued)

RX SENSITIVITY vs FREQUENCY

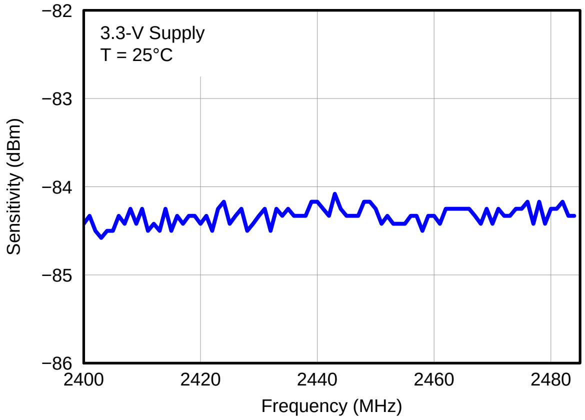


Figure 16.

TX POWER vs FREQUENCY

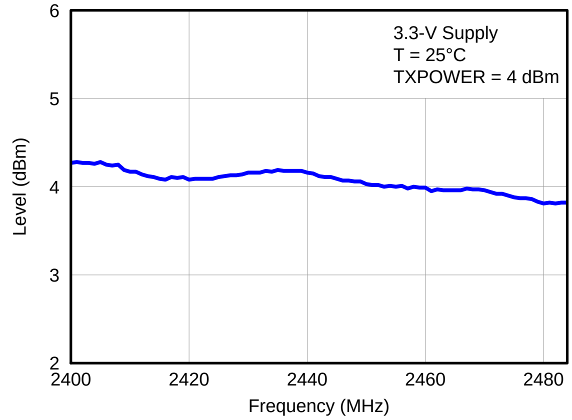


Figure 17.

RX INTERFERER REJECTION (SELECTIVITY) vs INTERFERER FREQUENCY

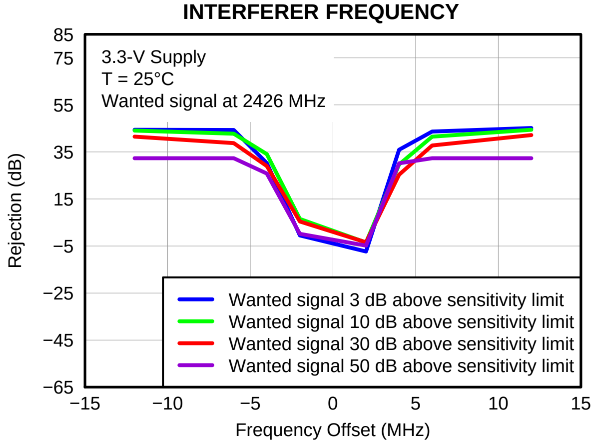


Figure 18.

APPLICATION INFORMATION

Few external components are required for the operation of the CC2544. A typical application circuit is shown in Figure 19. For suggestions of component values other than those listed in Table 2, see reference design CC2544EM. The performance stated in this data sheet is only valid for the CC2544EM reference design. To obtain similar performance, the reference design should be copied as closely as possible.

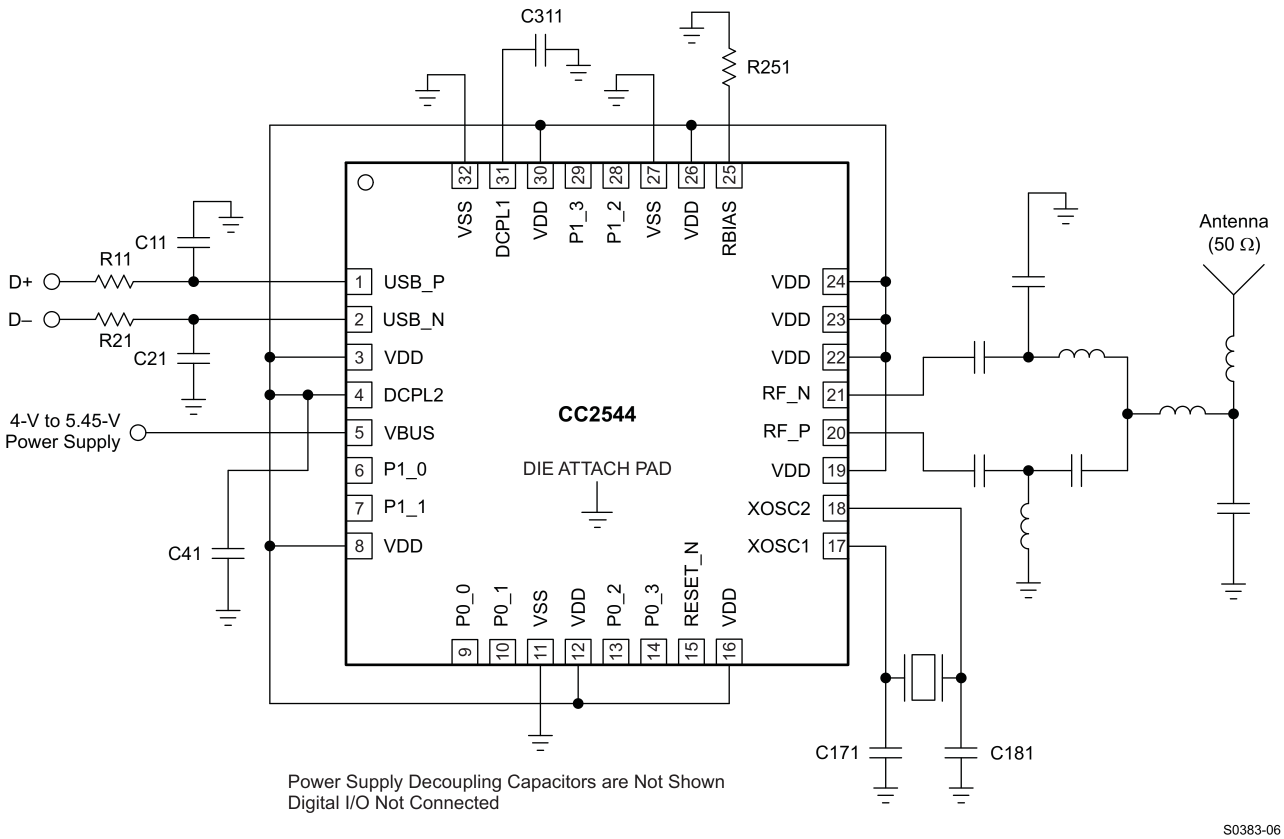


Figure 19. CC2544 Application Circuit

Table 2. Overview of External Components (Excluding Balun, Crystal and Supply Decoupling Capacitors)

Component	Description	Value
C11	USB D+ decoupling	47 pF
C21	USB D– decoupling	47 pF
C41	Decoupling capacitor for the internal 5V-3.3V digital voltage regulator	1 µF
C311	Decoupling capacitor for the internal 1.8V digital voltage regulator	1 µF
R11	USB D+ series resistor	33 Ω
R21	USB D– series resistor	33 Ω
R251	Precision resistor ±1%, used for internal biasing	56 kΩ

Input/Output Matching

When using an unbalanced antenna such as a monopole, a balun should be used to optimize performance. The balun can be implemented using low-cost discrete inductors and capacitors. See reference design, CC2544EM, for recommended balun.

Crystal

An external 32-MHz crystal with two loading capacitors is used for the 32-MHz crystal oscillator. The load capacitance seen by the 32-MHz crystal is given by:

$$C_L = \frac{1}{\frac{1}{C_{171}} + \frac{1}{C_{181}}} + C_{parasitic} \quad (1)$$

A series resistor may be used to comply with ESR requirement.

On-Chip 1.8-V Voltage Regulator Decoupling

The 1.8-V on-chip voltage regulator supplies the 1.8-V digital logic. This regulator requires a decoupling capacitor (C311) for stable operation.

On-Chip 5-V to 3.3-V USB Voltage Regulator Decoupling

The 5-V to 3.3-V on-chip voltage regulator supplies the 1.8-V on-chip voltage regulator. This regulator requires a decoupling capacitor (C41) for stable operation.

Power-Supply Decoupling and Filtering

Proper power-supply decoupling must be used for optimum performance. The placement and size of the decoupling capacitors and the power supply filtering are very important to achieve the best performance in an application. TI provides a compact reference design that should be followed very closely.

REVISION HISTORY

Changes from Original (June 2011) to Revision A **Page**

- Changes to the Product Preview data sheet 1

Changes from Revision A (March 2012) to Revision B **Page**

- Changed From: (–84 dBm at 2 Mbps) To: (–88 dBm at 2 Mbps) 1

Changes from Revision B (April 2012) to Revision C **Page**

- Changed the device From: Preview To: Production 1

Changes from Revision C (April 2012) to Revision D **Page**

- Added the Description 2

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CC2544RHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 125	CC2544
CC2544RHBR.A	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	CC2544
CC2544RHBR.B	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	CC2544
CC2544RHBT	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 125	CC2544
CC2544RHBT.A	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	CC2544
CC2544RHBT.B	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	CC2544

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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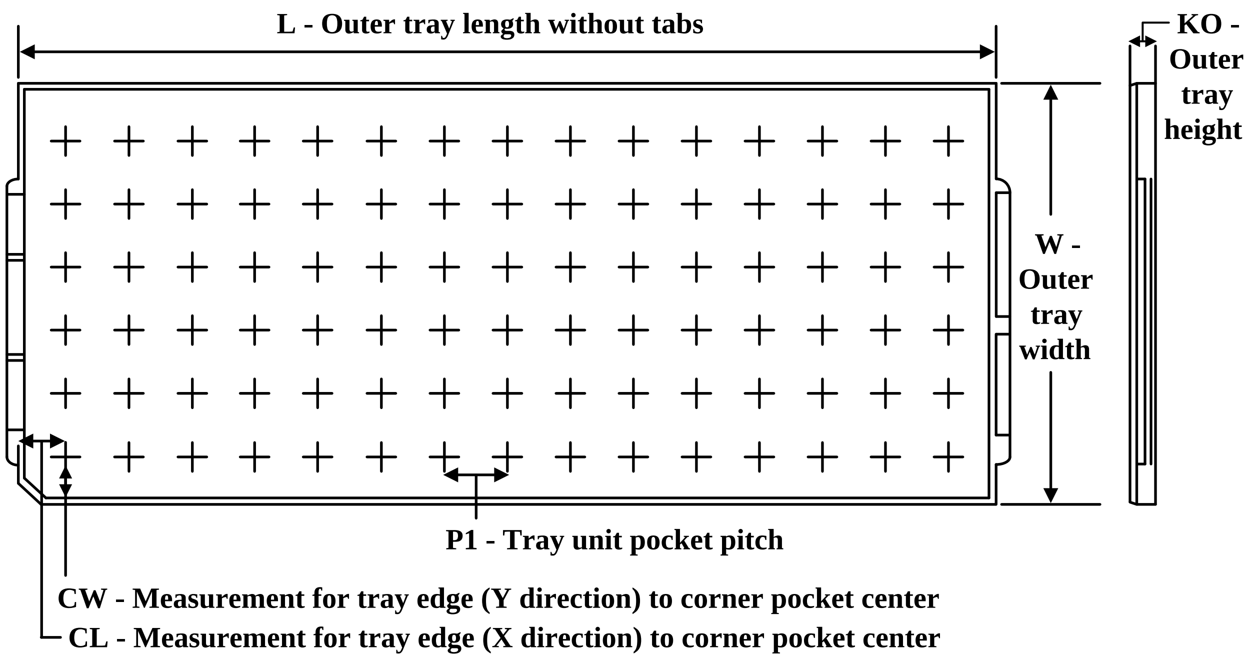
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

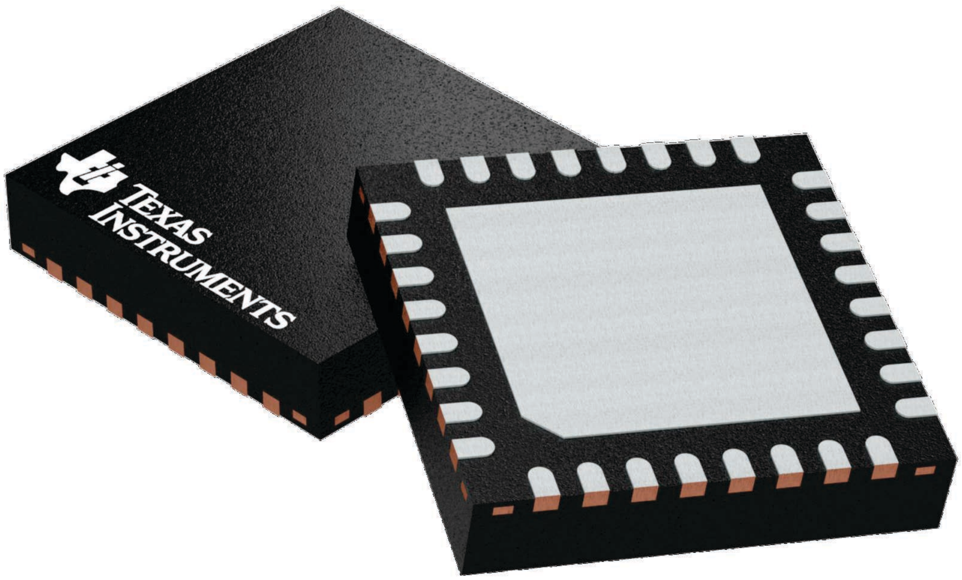
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
CC2544RHBR	RHB	VQFN	32	3000	14 x 35	150	315	135.9	7620	8.8	7.9	8.15
CC2544RHBR.A	RHB	VQFN	32	3000	14 x 35	150	315	135.9	7620	8.8	7.9	8.15
CC2544RHBR.B	RHB	VQFN	32	3000	14 x 35	150	315	135.9	7620	8.8	7.9	8.15
CC2544RHBT	RHB	VQFN	32	250	14 x 35	150	315	135.9	7620	8.8	7.9	8.15
CC2544RHBT.A	RHB	VQFN	32	250	14 x 35	150	315	135.9	7620	8.8	7.9	8.15
CC2544RHBT.B	RHB	VQFN	32	250	14 x 35	150	315	135.9	7620	8.8	7.9	8.15

RHB 32

VQFN - 1 mm max height

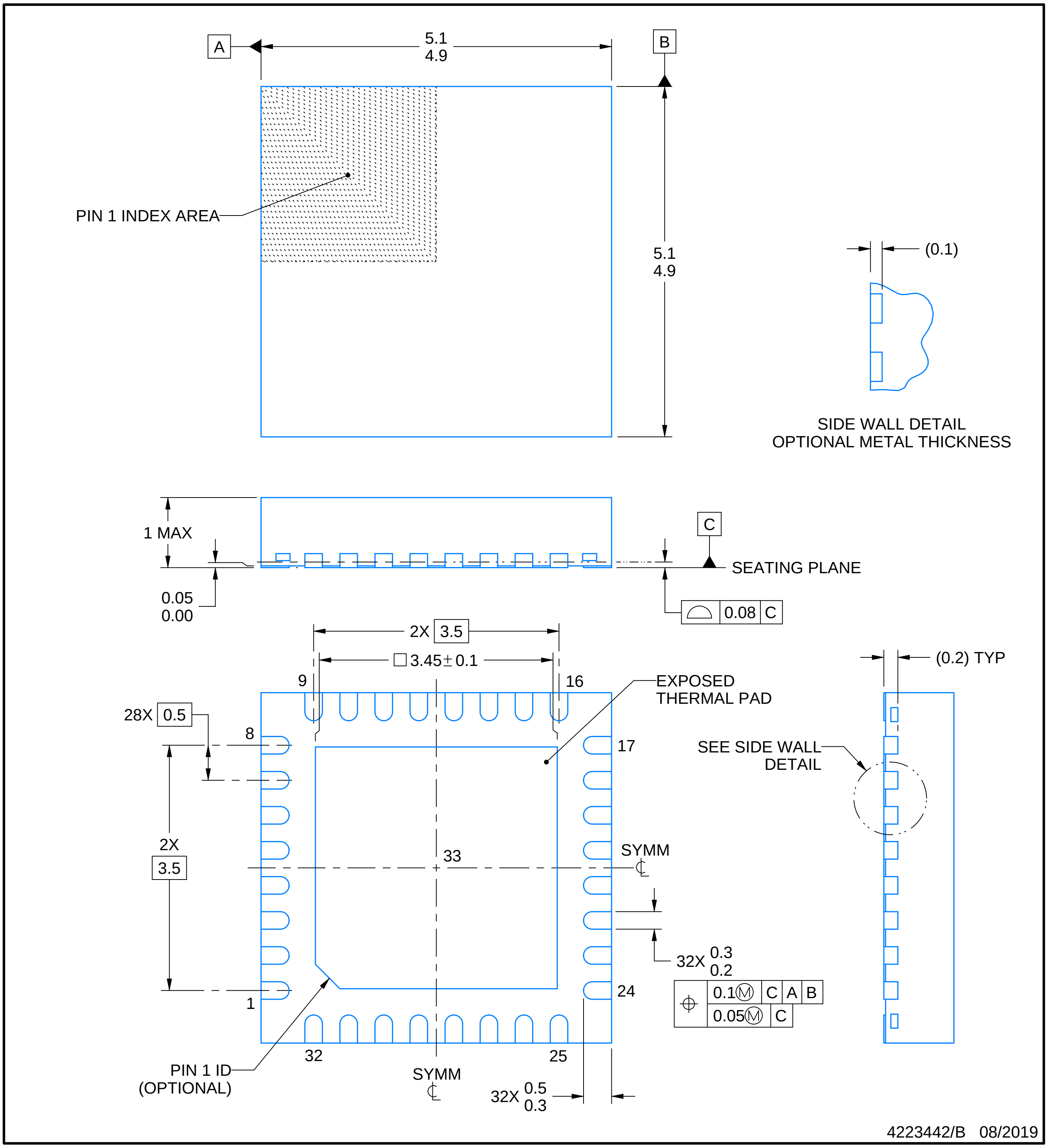
5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



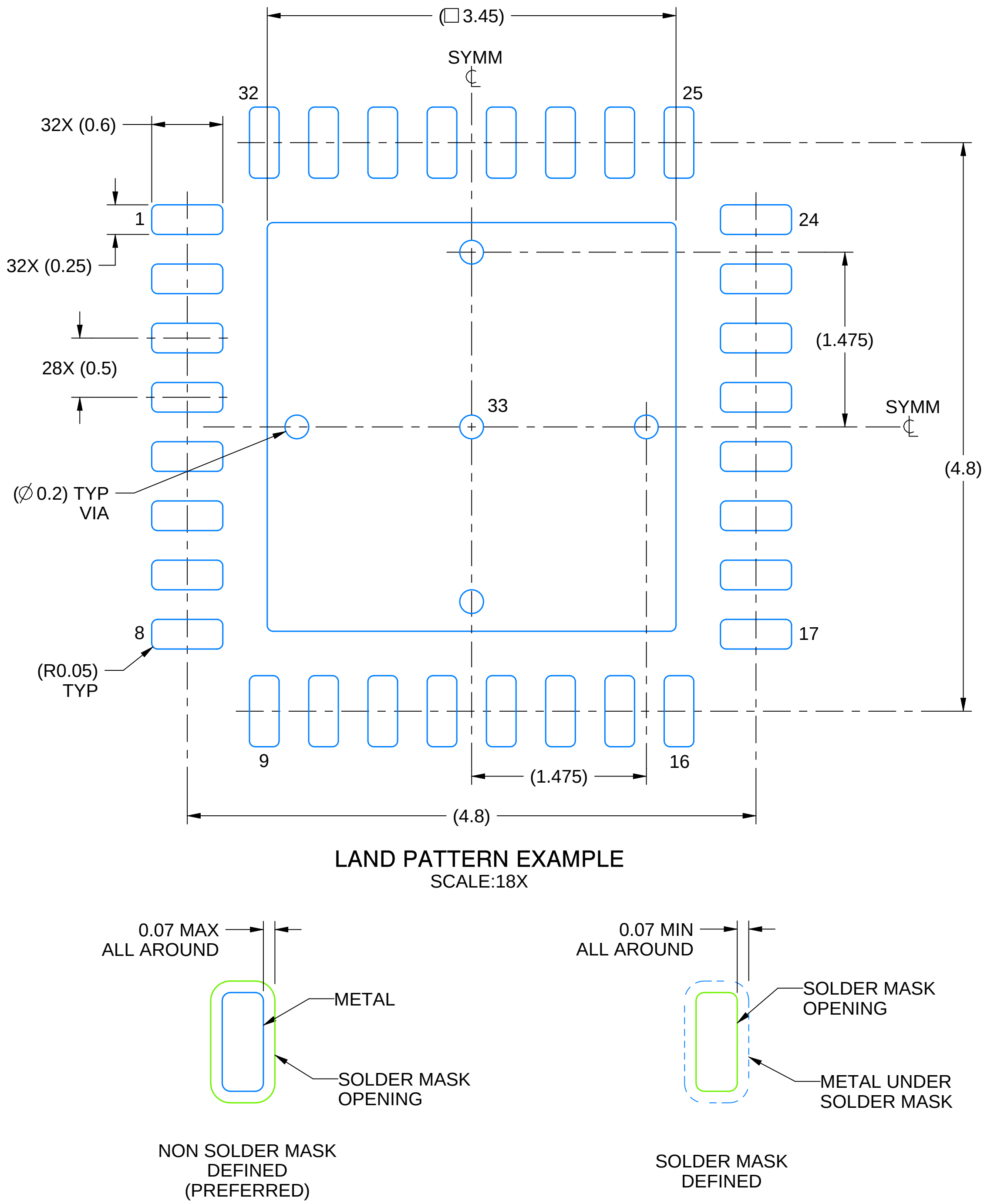
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224745/A



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X

NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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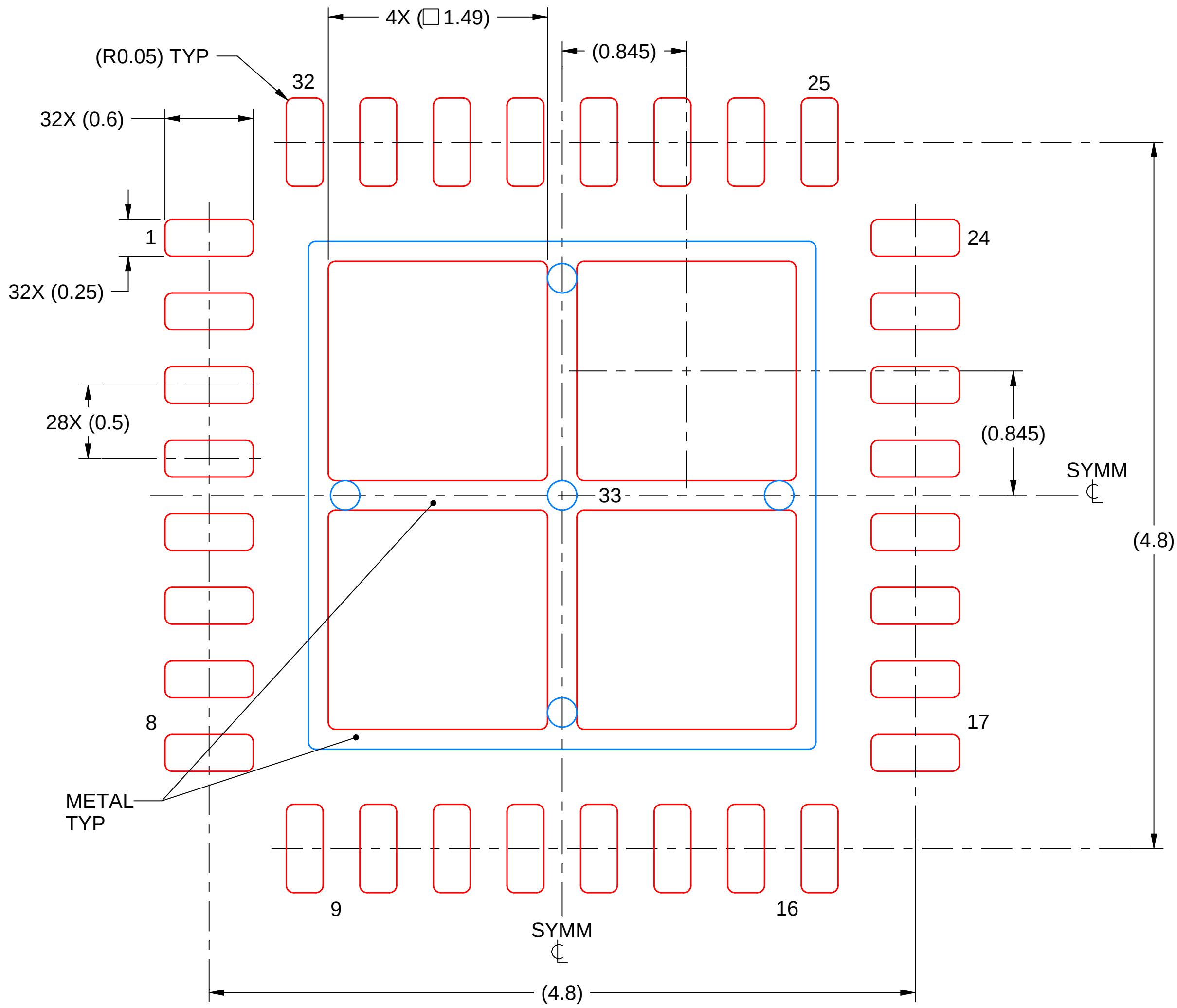
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.