

# BQ79881-Q1 UIR Sensor with Pack-Level EIS and Voltage, Current and Insulation Resistance Monitoring in EV/BMS HV Automotive Applications

#### 1 Features

- Two fast pack voltage measurements
  - Dedicated single-ended measurements; ASIL-D
  - HV Measurement Accuracy <0.4%; 0.3-5v single ended</li>
  - OuS VI sync within BQ79881; fast 5uS typical VI Sync with cell measurements
- · Accurate Single-Ended Measurements
  - Up to 18 single ended ADC inputs; ASIL-D
  - HV Measurement Accuracy <0.4%; 0-5V single ended</li>
  - Usable as ratiometric temperature sense inputs
  - Configurable 1.8V/2.5V/3.3V reference for HV measurements
- Four Current Sense ADCs
  - Measure up to two separate currents; ASIL-D
  - Input range = +/-275mV differential, +/-750mV common mode; ASIL-D
  - 0.1% accuracy. 10mA (50u Rshunt)
- Over Current Comparators
  - Dedicated fast overcurrent digital comparator per CS ADC; ASIL-D
  - Response: 100uS to 1mS. Accuracy: 1%
  - Thresholds: 0mV to +/-300mV.
  - OC response on GPIO pins.
  - Majority voting option
- · Upgraded Daisy Chain Interface
  - 2x parallel SPI ports to MCU to support split chain with single bridge device
  - 2-wire isolated interface, SPI to MCU
  - 2Mbps single chain/ring, 4Mbps split chain for up to 4x speed improvement
  - Closed Loop BCI: 200mA; Open Loop BCI: 300mA
  - Isolation: Transformer or capacitor-only
  - FDTI Time: <100ms for 800V packs or 250 cells</li>
  - Support for ring architecture
  - Reverse wakeup available without ring architecture
- Smart EIS Engine
  - Integrated Electrochemical Impedance Spectroscopy measurement engine
  - Impedance Accuracy: 1% with 1A excitation,
     >200uΩ impedance
  - Excitation frequency: 0.01Hz 3.5kHz
  - < 5us I/V synchronization from device to device</li>

- Support for global excitation
- Other
  - 12V switch drive pins to drive NMOSFET or Opto-MOS switches
  - Package: 48-pin QFN, 0.5mm pitch
  - Meets AEC-Q100 and ISO26262 ASIL-D Functional Safety
- Power Consumption

Active mode: < 100mW</li>Sleep mode: < 0.5mW</li>

Deep sleep mode: < 0.05mW</li>

#### 2 Applications

- Battery Management System (BMS) in hybrid and electric powertrain systems
- Energy storage battery packs with Battery Management Systems

#### 3 Description

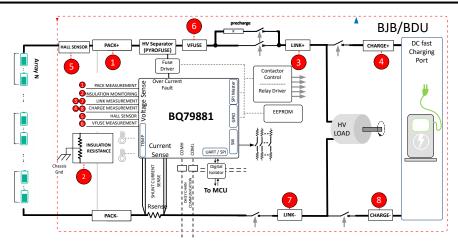
The device can be used to measure divided down high voltage nodes in a battery system. It can measure voltages across Fuses and Contactors, and it can check isolation voltages in battery junction box (BJB) systems. The device has four integrated current sense paths supporting low side shunt resistors. Coulomb counting is available for accurate SOC calculation. There are 18 GPIOs/auxiliary inputs that can be used for HV measurements, thermistor measurements and driving relays. There are 4 SW outputs that can be used to drive MOSFET switches in the measurement path. The device can function as a SPI and I2C HUB and interface with up to 8 separate SPI devices/groups. Over current protection response can be achieved autonomously using OC Pins for fast reaction in dangerous over current events. The isolated bi-directional daisy chain ports support both capacitor and transformer based isolation. The device can also communicate with MCU over SPI.

#### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
BQ79881-Q1	HTQFP (48-pin)	7mm × 7mm

 For all available packages, see the orderable addendum at the end of the data sheet.





**Simplified System Diagram** 



#### 4 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

#### 4.1 Device Support

#### 4.1.1 Third-Party Products Disclaimer

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#### 4.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 4.3 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### 4.4 Trademarks

TI E2E<sup>™</sup> is a trademark of Texas Instruments.

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#### 4.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 4.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

#### 5 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



#### 5.1 Package Option Addendum

**Packaging Information** 

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>		MSL Peak Temp <sup>(3)</sup>	Op Temp (°C)	Device Marking <sup>(4) (5)</sup>
PBQ79881QPH PQ1	ADVANCED RELEASE	HTQFP	PHP	48	250	RoHS & Green	NiPdAu	MSL-3-260C-16 8 HR	-40 to 125C	PBQ79881A1

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PRE\_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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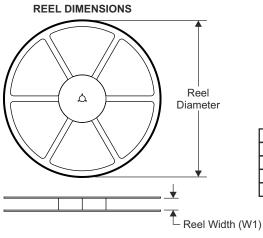
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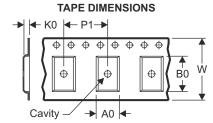
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Product Folder Links: BQ79881-Q1



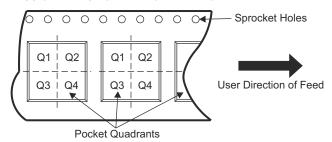
#### 5.2 Tape and Reel Information





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

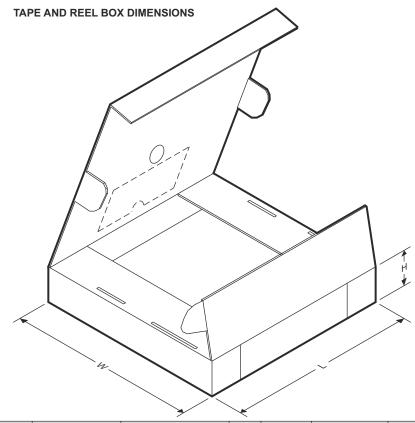
#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant	
PBQ79881QPHPQ1	HTQFP	PHP	48	250	330.0	16.4	9.3	9.3	2.2	12.0	16.0	Q2	

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PBQ79881QPHPQ1	HTQFP	PHP	64	1000	367.0	367.0	55.0



#### 5.3 Mechanical Data

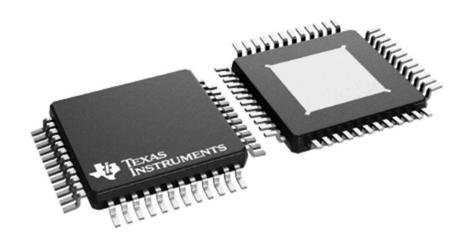
# **PHP 48**

TQFP - 1.2 mm max height

7 x 7, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



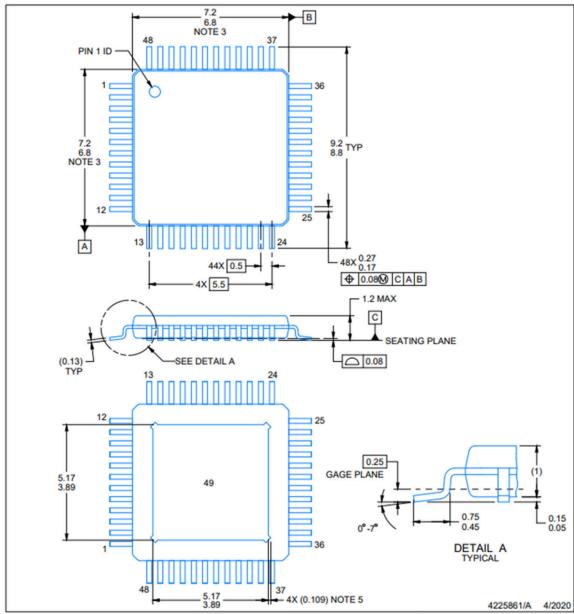


#### **PACKAGE OUTLINE**

### **PHP0048G**

# PowerPAD™ HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



#### NOTES:

PowerPAD is a trademark of Texas Instruments

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
- per ASME Y14.5M.

  2. This drawing is subject to change without notice.
- This drawing is subject to draingle without notice.
   This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
   Reference JEDEC registration MS-026.
   Feature may not be present.

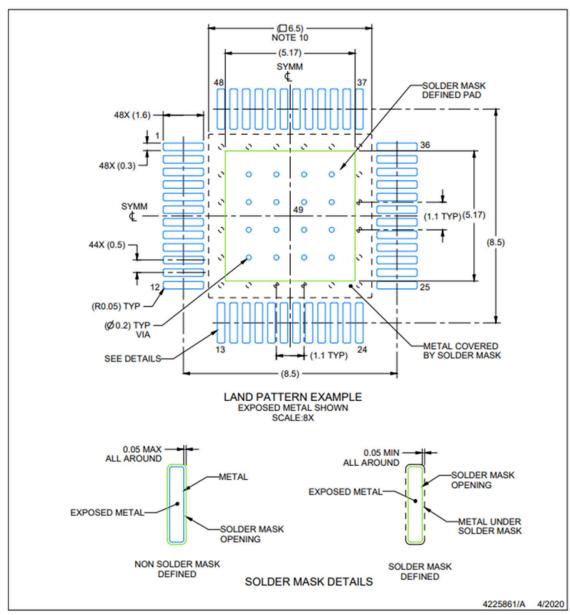


#### **EXAMPLE BOARD LAYOUT**

#### **PHP0048G**

# PowerPAD™ HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



#### NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
- 9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
- 10. Size of metal pad may vary due to creepage requirement.

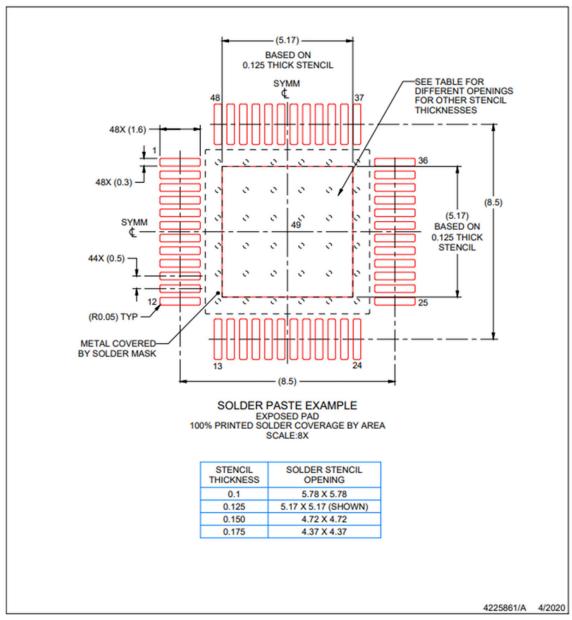


#### **EXAMPLE STENCIL DESIGN**

# **PHP0048G**

# PowerPAD™ HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



NOTES: (continued)

- Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 12. Board assembly site may have different recommendations for stencil design.

www.ti.com 16-Oct-2025

#### PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
PBQ79881QPHPQ1	Active	Preproduction	HTQFP (PHP)   48	160   JEDEC TRAY (10+1)	-	Call TI	Call TI	-	

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

7 x 7, 0.5 mm pitch

QUAD FLATPACK

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