BQ79826Z-Q1 Automotive 26S/24S Battery Monitor with Smart EIS Engine

1 Features

- 26 Channels
  - 26S – 0 to 5.5V range for cell, -2V to 2V range for busbar
  - 143V Abs Max Rating, 9V minimum
  - Busbar support on every channel, except first channel.
  - Stackable up to 128 devices
- Voltage Accuracy
  - <1.7 mV accuracy, -40 to 125C, Cell: 0V to 5.5V
  - Dedicated ADC per channel. Synchronized redundant measurement.
- Passive Cell Balancing with integrated FETs up to 300mA odd/even balancing with programmable PWM control
- Smart EIS Engine
  - Integrated Electrochemical Impedance Spectroscopy measurement engine
  - Impedance Accuracy: 1% (with 1A excitation and 200uΩ impedance)
  - Measurement frequency: 0.01Hz to 3.5kHz
  - < 5us I/V synchronization from device to device
  - Support for global and local excitation
- Sensor & GPIOs
  - 20 GPIO: Temp Sensor (NTC/PTC), voltage measurement, Interrupt
  - SPI / I^2C Interface
  - Temperature Threshold (Active / Sleep)
  - Pressure Threshold / Peak Detector (Active / Sleep)
  - On-chip memory for one-time custom programming
- Diagnostics & Protection
  - Monitoring
    - Low Power Monitoring Mode (<20uA power consumption)
    - Cell Over-voltage, Under-voltage (OVUV)
    - Cell Over-temperature, Under-temperature (OTUT)
    - 2x die temperature monitors
    - Supply (BAT)
    - Open Wire Detection
  - Reverse Wake Up based on selectable faults
  - Redundancy Paths
    - Cell Voltage
    - GPIO/NTC Voltage
    - Limp Home Mode
  - Diagnostics
    - Automatic diagnostics during cell balancing in active mode
  - Functional Safety Compliant
    - Developed under ISO26262
    - System and hardware capability up to ASIL-D
- Upgraded Daisy Chain Interface
  - 2Mbps bus speed, Up to 4Mbps with dual SPI
  - <+/-5us device to device synchronization
  - Closed Loop BCI: 200mA, Open Loop BCI: 300mA
  - Isolation: Transformer or capacitor-only
  - FDTI Time: <100ms for 800V packs or 250 cells
  - Support for stack, ring, multidrop, and split-ring
  - Device-to-device automatic communications balancing
- Power
  - Integrated DC-DC Converter
  - Shutdown: <10uA
  - Sleep Mode with monitoring: As low as 20uA
  - Active Mode: <5mA
- Package
  - 100-pin QFP, 4mm pitch
  - PowerPad on bottom

2 Applications

- EV - Electric Vehicles
- ESS - Energy Storage Systems

3 Description

The BQ79826Z-Q1 is a new high-cell count 26S stackable battery monitor that includes integrated electrochemical impedance spectroscopy (EIS) engine. The EIS engine provides a new way to detect impedance changes in the cell that allows for monitoring of aging, temperature, SoC, thermal runaway and many other cell parameters. In addition, the device incorporates an intelligent sensor controller to enable easier and more reliable sensor measurements.

Package Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
BQ79826Z-Q1	HTQFP (100)	12mm x 12mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

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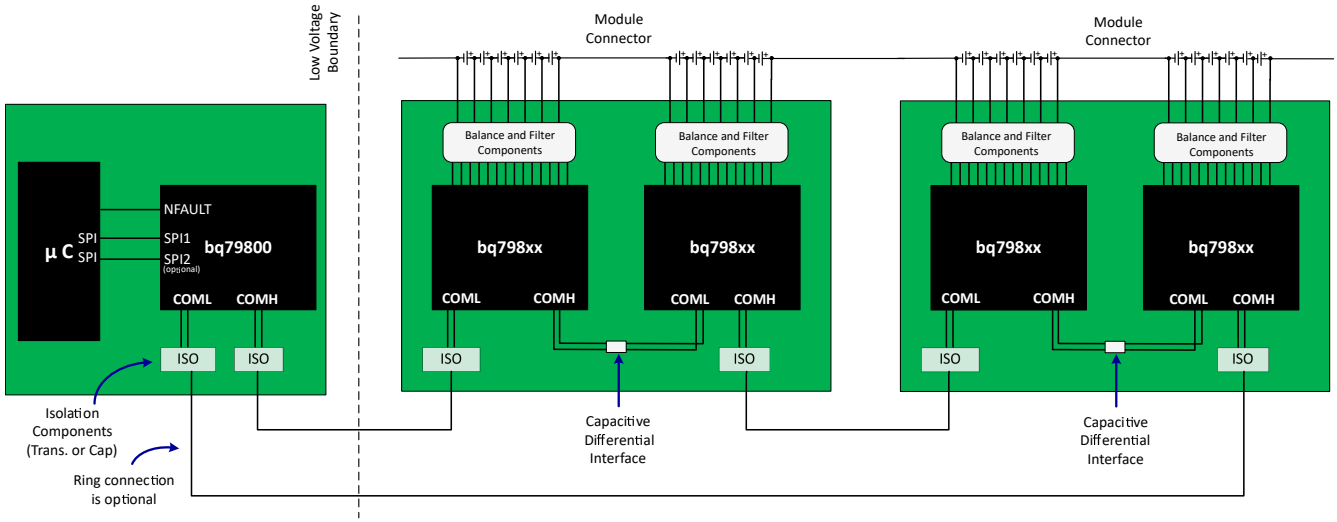

Battery Management System

ADVANCE INFORMATION

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4 Pin Configuration and Functions

See the GPIO Configuration Table for the full GPIO functions list and behavior. Most GPIO functions are listed in the pin-outs, but some functions that move or interact with other pins are not fully described in Section 4.

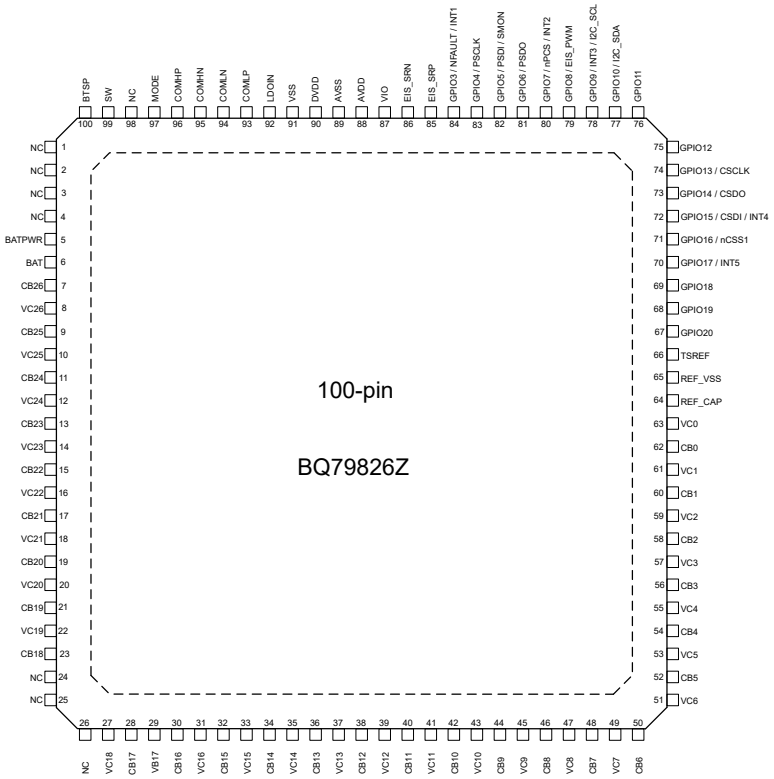

Figure 4-1. BQ79826Z Pin Configuration

Table 4-1. Pin Functions

Pin Name		Type	Description
BQ79826Z	No		
NC	1	NC	Do not connect. Not internally connected to the die.
NC	2	NC	Do not connect. Not internally connected to the die.
NC	3	NC	Do not connect. Not internally connected to the die.
NC	4	NC	Do not connect. Not internally connected to the die.
BATPWR	5	P	Power supply input to the DC-DC converter. Connect to BAT.
BAT	6	P	Power supply input and top of module measurement input. Connect to the top cell of the battery module. Bypass a capacitor to VSS.
CBxx	Odd Pins 7-23	I	Cell balance connection. Require differential RC filter, which the filter resistor also set the internal balance current.
VCxx	Even Pins 8-22	I	Cell voltage sense input. Connect to the positive terminal of cell below. Requires differential RC filter.
NC	24	NC	Do not connect. Not internally connected to the die.
NC	25	NC	Do not connect. Not internally connected to the die.
NC	26	NC	Do not connect. Not internally connected to the die.
CBxx	Odd Pins 27-63	I	Cell balance connection. Require differential RC filter, which the filter resistor also set the internal balance current.

Table 4-1. Pin Functions (continued)

Pin Name		Type	Description
BQ79826Z	No		
VCxx	Even Pins 28-62	I	Cell voltage sense input. Connect to the positive terminal of cell below. Requires differential RC filter.
REF_CAP	64	R	1st ADC reference output pin, bypass with a capacitor to REF_VSS.
REF_VSS	65	GND	Ground connection for the precision reference REF_CAP and TSREF. Connect to VSS, please refer layout guidance for layout.
TSREF	66	R	2nd ADC reference output pin, also provides bias voltage for thermistor. Bypass TSREF with a capacitor to REF_VSS.
GPIO20	67	I/O	GPIOx can be used as general-purpose input/output like digital I/O, analog input, etc.
GPIO19	68	I/O	
GPIO18	69	I/O	
GPIO17 / INT5	70	I/O	
GPIO16 / nCSS1	71	I/O	Selectable as SPI controller (hub) interface to peripheral devices or GPIO.
GPIO15 / CSDI / INT4	72	I/O	
GPIO14 / CSDO	73	I/O	
GPIO13 / CSCLK	74	I/O	
GPIO12	75	I/O	GPIOx can be used as general-purpose input/output like digital I/O, analog input, etc.
GPIO11	76	I/O	
GPIO10 / I2C_SDA	77	I/O	Selectable as I2C controller (hub) or GPIO.
GPIO9 / INT3 / I2C_SCL	78	I/O	
GPIO8 / EIS_PWM	79	I/O	GPIOx can be used as general-purpose input/output like digital I/O, analog input, etc. Electrochemical impedance spectroscopy PWM output.
GPIO7 / nPCS / INT2	80	I/O	Selectable as SPI device control or GPIO.
GPIO6 / PSDO	81	I/O	
GPIO5 / PSDI / SMON	82	I/O	
GPIO4 / PSCLK	83	I/O	
GPIO3 / NFAULT / INT1	84	I/O	Selectable as NFAULT interrupt pin or GPIO
EIS_SRP	85	I/O	GPIOx can be used as general-purpose input/output like digital I/O, analog input, etc. Electrochemical impedance spectroscopy differential current sense input.
EIS_SRN	86	I/O	
VIO	87	P	Input supply voltage for GPIOs. Connect direclty to AVDD or an external IO supply.
AVDD	88	P	Regulated output. AVDD supplies the internal analog circuits as well as up to xxmA of external Load. Bypass AVDD with a capacitor to AVSS
AVSS	89	GND	Analog reference ground.
DVDD	90	R	Digitial supply. Connect cap from DVDD_CAP to DVSS.
VSS	91	GND	Digital ground. Bonded to pad.
LDOIN	92	I/O	Regulated supply input. Connect to the output of the DC-DC buck converter. Bypass LDOIN to VSS with a capacitor.
COMLP	93	I/O	AC coupled bi-directional I/O pin for daisy chain (VIF) communication. Do not apply external DC voltage to this pin. Connect to COMHN/P of adjacent device through proper isolation. Leave disconnected if not used.
COMLN	94	I/O	
COMHN	95	I/O	
COMHP	96	I/O	
MODE	97	I/O	Connect resistor to ground. Configures the settings for AVDD status during SHUTDOWN and DEEPSLEEP and device multidrop or non-multidrop.
NC	98	NC	Do not connect. Not internally connected to the die.

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Table 4-1. Pin Functions (continued)

Pin Name		Type	Description
BQ79826Z	No		
SW	99	P	DC-DC switch node. Connect to inductor.
BTSP	100	P	Buck converter bootstrap. Connect bootstrap capacitor from BTSP to SW.

P = Power, GND = Device ground, R = reference, I = Cell or BB Input, I/O = Input/Output, NC = No connect

Mode Pin Configuration

The MODE pin must be configured with a resistor to ground (R_{MODE}). The resistor is chosen based on the operating mode and the devices communication type as either as non-multidrop or multidrop device.

Table 4-2. MODE Pin Configuration

R_{MODE} Value	AVDD Mode in SHUTDOWN and DEEP SLEEP	Multidrop
R_{MODE} < 413kΩ or Open	ON	No
132kΩ < R_{MODE} < 168kΩ	ON	Yes
49kΩ < R_{MODE} < 63kΩ	OFF	Yes
R_{MODE} < 21kΩ	OFF	No

ADVANCE INFORMATION

5 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

5.1 Documentation Support

5.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

5.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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5.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

6.1 Package Option Addendum

Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
PBQ79826ZQPZSQ1	PRE_PROD	HTQFP	PZS	100	1000	Call TI	Call TI	Call TI	-40 to 125C	PBQ79826ZQ

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

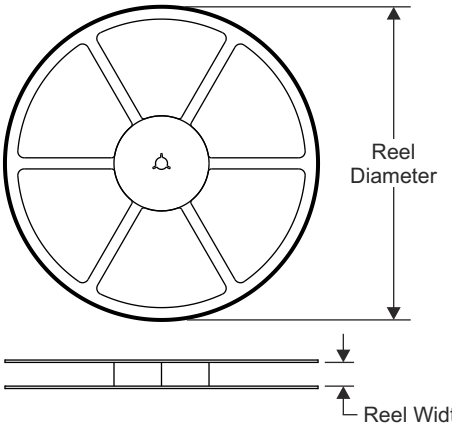
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

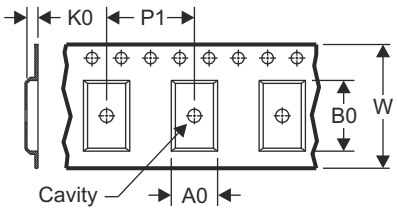
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

6.2 Tape and Reel Information

REEL DIMENSIONS

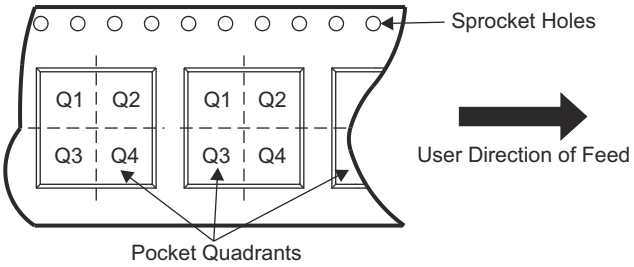


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PBQ79826ZQPZSQ1	HTQFP	PZS	100	2000	330	16.4	15	15	2	20	24	2

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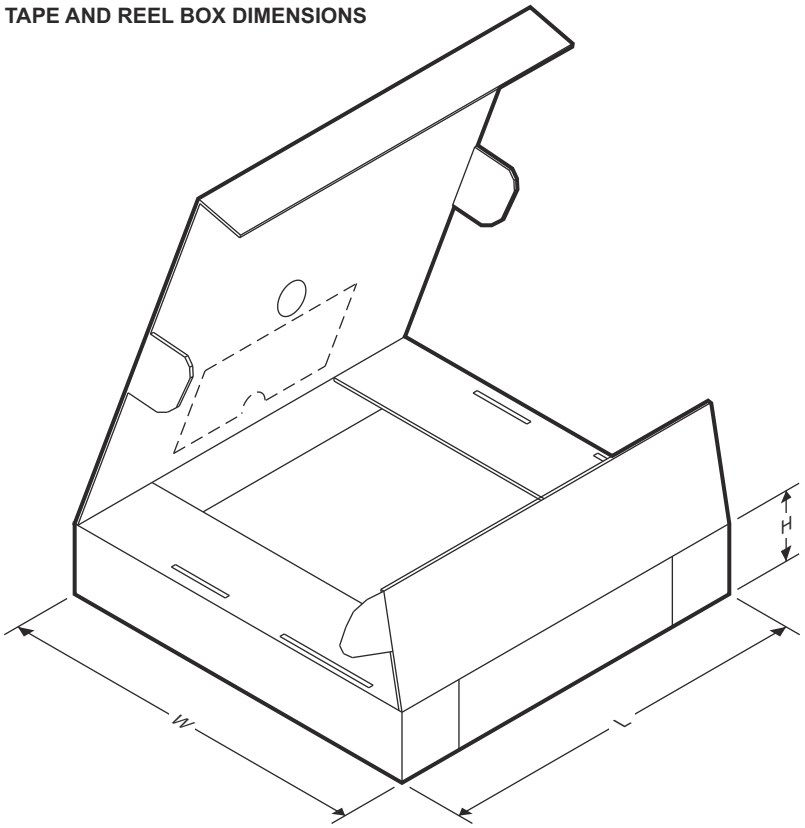
TAPE AND REEL BOX DIMENSIONS



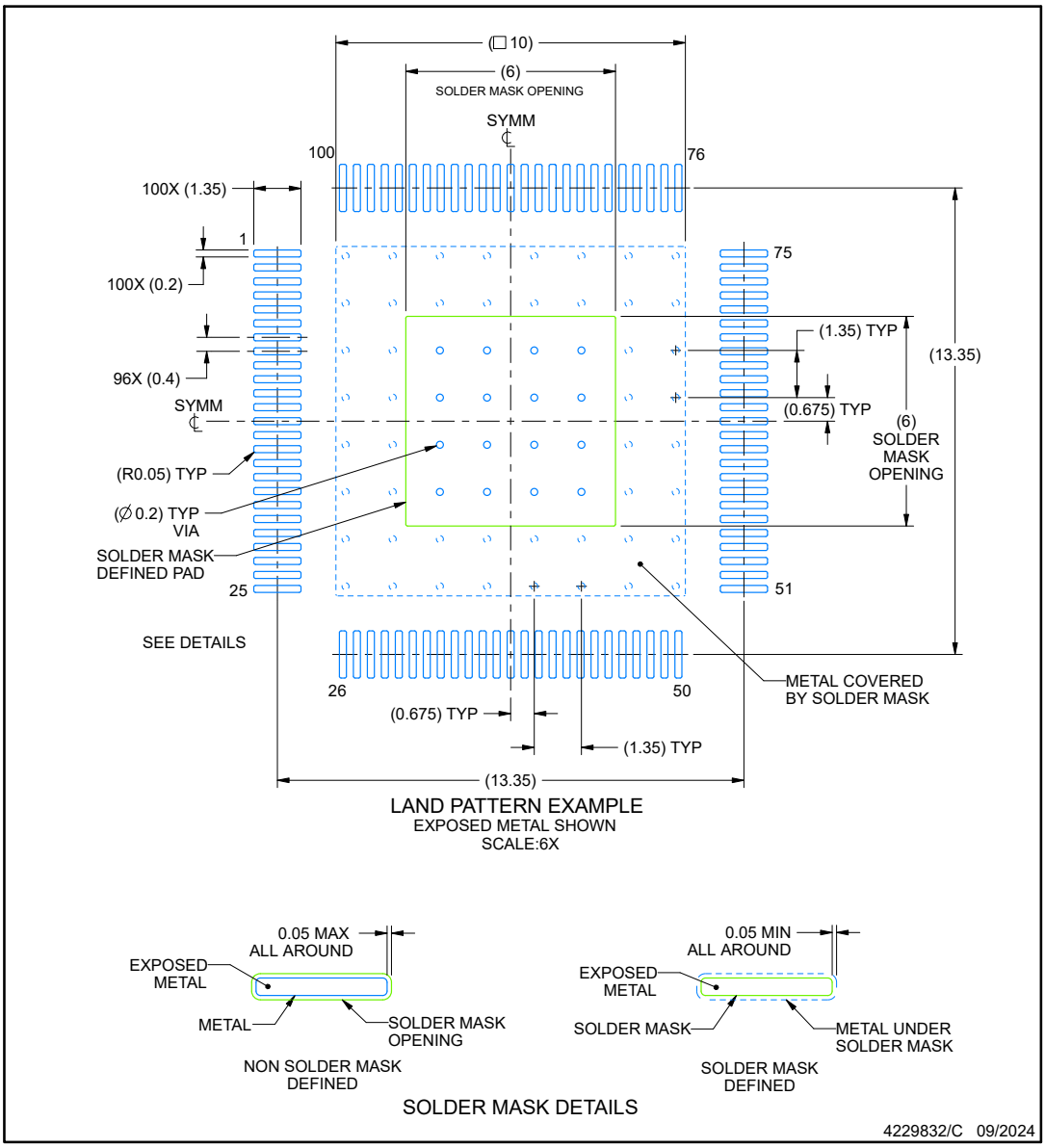
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PBQ79826ZQPZSQ1	HTQFP	PZS	100	2000	360	350	45

6.3 Mechanical Data

EXAMPLE BOARD LAYOUT

PZS0100A — **PowerPAD ™ HTQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



NOTES: (continued)

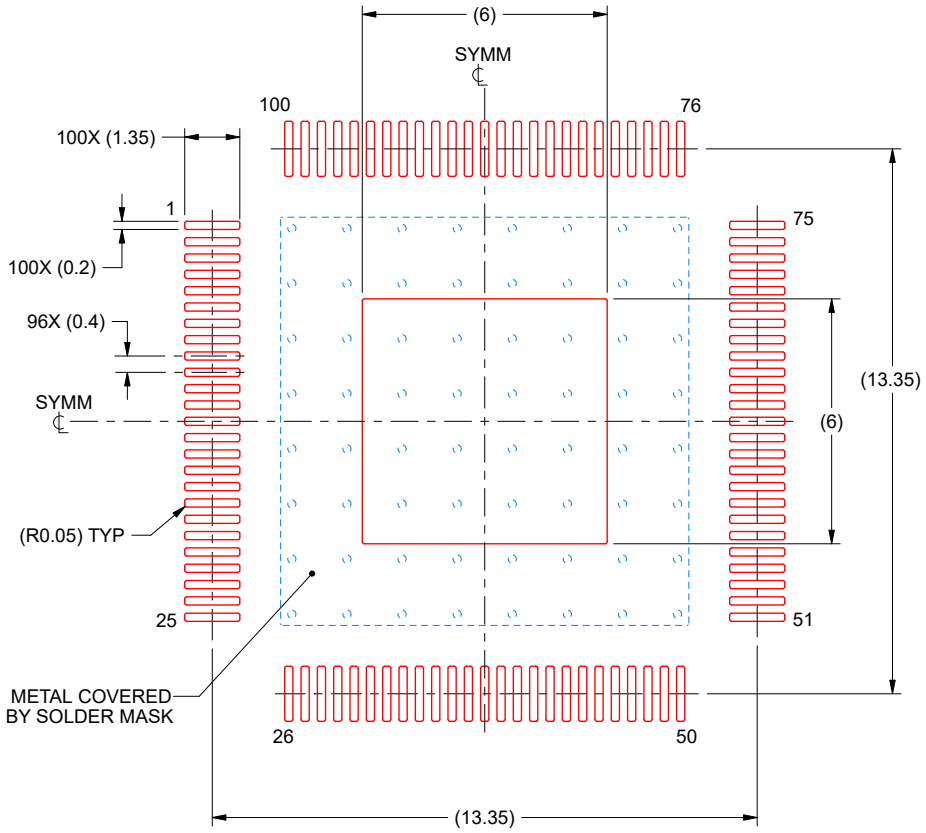
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

PZS0100A — **PowerPAD ™ HTQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE

EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	6.71 X 6.71
0.125	6.00 X 6.00 (SHOWN)
0.15	5.48 X 5.48
0.175	5.07 X 5.07

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PBQ79826ZQPZSQ1	Active	Preproduction	HTQFP (PZS) | 100	160 | JEDEC TRAY (5+1)	-	Call TI	Call TI	-	

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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