bq2920x Voltage Protection with Automatic Cell Balance for 2-Series Cell Li-Ion Batteries

1 Features

- 2-Series Cell Secondary Protection
- Automatic Cell Imbalance Correction with External Enable Control
  - ±30-mV Enable, 0-mV Disable Thresholds Typical
- External Capacitor-Controlled Delay Timer
- External Resistor-Controlled Cell Balance Current
- Low Power Consumption I_{CC} < 3 µA Typical (V_{CELL}(ALL) < $V_{PROTECT}$)
- Internal Cell Balancing Handles Current up to 15 mA
- External Cell Balancing Mode Supported
- High-Accuracy Overvoltage Protection:
  - ±25 mV with T_A = 0°C to 60°C
- Fixed Overvoltage Protection Thresholds: 4.30 V, 4.35 V
- Small 8L DRB Package

2 Applications

- 2nd Level Protection in Li-Ion Battery Packs
  - Netbook Computers
  - Power Tools
  - Portable Equipment and Instrumentation
  - Battery Backup Systems

3 Description

The bq2920x device is a secondary overvoltage protection IC for 2-series cell lithium-ion battery packs that incorporates a high-accuracy precision overvoltage detection circuit and automatic cell imbalance correction.

The voltage of each cell in a 2-series cell battery pack is compared to a factory programmed internal reference voltage. If either cell reaches an overvoltage condition, the OUT pin changes from low to high state.

The bq2920x can perform automatic voltage-based cell imbalance correction. Balancing can start when the cell voltages are different by nominally 30 mV or more and stops when the difference is nominally 0 mV. Cell balancing is enabled and disabled by the CB_EN pin.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq29200	VSON (8)	3.00 mm × 3.00 mm
bq29209		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic

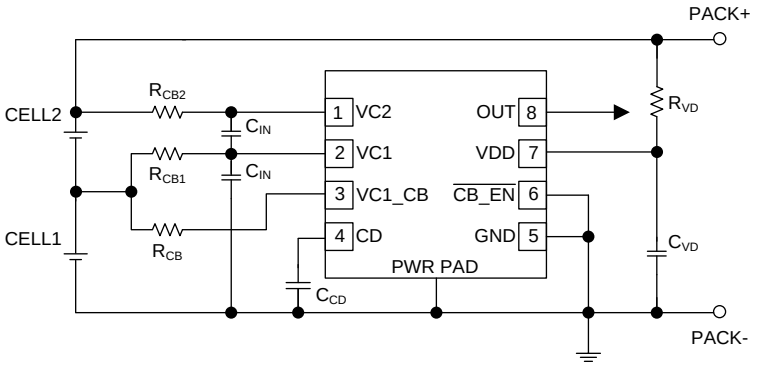


Table of Contents

4 Revision History

Changes from Revision B (December 2014) to Revision C **Page**

- Changed *Typical Application* title to *Simplified Schematic* ... 1
- Changed resistor R_{VD} location, added PACK+ and PACK- in the *Simplified Schematic* image ... 1
- Deleted the Lead Temperature (soldering) from the *Absolute Maximum Ratings* table ... 4
- Deleted table notes 2 through 7 from the *Thermal Information* ... 5
- Changed resistor R_{VD} location in Figure 9 ... 13
- Added title to Table 1 ... 13
- Changed resistor R_{VD} location, added PACK+ and PACK- in Figure 11 ... 14

Changes from Revision A (September 2010) to Revision B **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

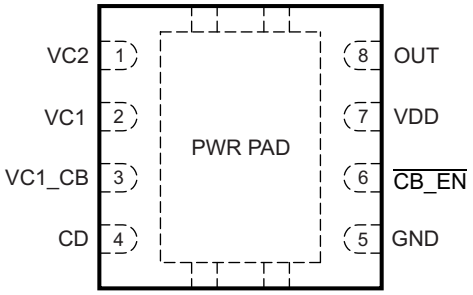
Changes from Original (June 2010) to Revision A **Page**

5 Device Options

T_A	PART NUMBER	OVP
–40°C to +110°C	BQ29200	4.35 V
	BQ29209	4.30 V

6 Pin Configuration and Functions

DRB Package
8-Pin VSON
Top View



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
$\overline{\text{CB\_EN}}$	6	Cell balance enable
CD	4	Connection to external capacitor for programmable delay time
GND	5	Ground pin
OUT	8	Output
Thermal Pad	PWR PAD	GND pin to be connected to the PWRPAD on the printed circuit board for proper operation
VC1	2	Sense voltage input for bottom cell
VC1_CB	3	Cell balance input for bottom cell
VC2	1	Sense voltage input for top cell
VDD	7	Power supply

7 Specifications

7.1 Absolute Maximum Ratings

Over-operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range, V_{MAX}	VDD–GND	–0.3	16	V
Input voltage range, V_{IN}	VC2–GND, VC1–GND	–0.3	16	V
	VC2–VC1, CD–GND	–0.3	8	V
	$\overline{\text{CB\_EN}}$–GND	–0.3	16	V
Output voltage range, V_{OUT}	OUT–GND	–0.3	16	V
Continuous total power dissipation, P_{TOT}		See *Thermal Information.*		
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, VDD		4		10	V
Input voltage range	VC2–VC1, VC1–GND	0		5	V
Delay time capacitance, $t_{d(CD)}$	C_{CD} (See Figure 9.)		0.1		µF
Voltage monitor filter resistance	R_{IN} (See Figure 9.)	100	1K		Ω
Voltage monitor filter capacitance	C_{IN} (See Figure 9.)	0.01	0.1		µF
Supply voltage filter resistance	R_{VD} (See Figure 9.)		100	1K	Ω
Supply voltage filter capacitance	C_{VD} (See Figure 9.)		0.1		µF
Cell balance resistance	R_{CB} (See Figure 9 and *Protection (OUT) Timing*.)	100		4.7K	Ω
Operating ambient temperature range, T_A		–40		110	°C

7.4 Thermal Information

THERMAL METRIC (1)		bq2920x DRB 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	25.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	18.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	5.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Typical values stated where T_A = 25°C and VDD = 7.2 V. Minimum and maximum values stated where T_A = –40°C to 110°C and VDD = 4 V to 10 V (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{PROTECT}$	Overvoltage detection voltage	bq29209			4.3		V
		bq29200			4.35		
V_{HYS}	Overvoltage detection hysteresis			200	300	400	mV
V_{OA}	Overvoltage detection accuracy		T_A = 25°C	–10		10	mV
V_{OA_DRIFT}	Overvoltage threshold temperature drift		T_A = 0°C to 60°C	–0.4		0.4	mV°/C
			T_A = –40°C to 110°C	–0.6		0.6	
X_{DELAY}	Overvoltage delay time scale factor		T_A = 0°C to 60°C Note: Does not include external capacitor variation.	6	9	12	s/µF
			T_A = –40°C to 110°C Note: Does not include external capacitor variation.	5.5	9	13.5	

Electrical Characteristics (continued)

Typical values stated where T_A = 25°C and VDD = 7.2 V. Minimum and maximum values stated where T_A = –40°C to 110°C and VDD = 4 V to 10 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
X_{DELAY_CTM} (1)	Overvoltage delay time scale factor in Customer Test Mode			0.08		s/µF
$I_{CD(CHG)}$	Overvoltage detection charging current			150		nA
$I_{CD(DSG)}$	Overvoltage detection discharging current			60		µA
V_{CD}	Overvoltage detection external capacitor comparator threshold			1.2		V
I_{CC}	Supply current	(VC2–VC1) = (VC1–GND) = 3.5 V (See Figure 7.)		3	6	µA
V_{OUT}	OUT pin drive voltage	(VC2–VC1) or (VC1–GND) > $V_{PROTECT}$, VDD = 10 V, I_{OH} = 0	6	8.25	9.5	V
		(VC2–VC1) or (VC1–GND) = $V_{PROTECT}$, VDD = $V_{PROTECT}$, I_{OH} = –100 µA, T_A = 0°C to 60°C	1.75	2.5		V
		(VC2–VC1) and (VC1–GND) < $V_{PROTECT}$, I_{OL} = 100 µA, T_A = 25°C			200	mV
		(VC2–VC1) and (VC1–GND) < $V_{PROTECT}$, I_{OL} = 0 µA, T_A = 25°C		0	10	mV
		VC2 = VC1 = VDD = 4 V, I_{OL} = 100 µA			200	mV
I_{OH}	High-level output current	OUT = 1.75 V, (VC2–VC1) or (VC1–GND) = $V_{PROTECT}$, VDD = $V_{PROTECT}$ to 10 V, T_A = 0°C to 60°C	–100			µA
I_{OL}	Low-level output current	OUT = 0.05 V, (VC2–VC1) or (VC1–GND) < $V_{PROTECT}$, VDD = $V_{PROTECT}$ to 10 V, T_A = 0°C to 60°C	30		85	µA
I_{OH_ZV}	High-level short-circuit output current	OUT = 0 V, (VC2–VC1) = (VC1–GND) = $V_{PROTECT}$ VDD = 4 to 10 V			–8	mA
I_{IN}	Input current at VCx pins	Measured at VC1, (VC2–VC1) = (VC1–GND) = 3.5 V, T_A = 0°C to 60°C (See Figure 7.)	–0.2		0.2	µA
		Measured at VC2, (VC2–VC1) = (VC1–GND) = 3.5 V, T_A = 0°C to 60°C (See Figure 7.)			2.5	µA
$V_{MM\_DET\_ON}$	Cell mismatch detection threshold for turning ON	(VC2–VC1) versus (VC1–GND) and vice-versa when cell balancing is enabled. VC2 = VDD = 7.6 V	17	30	45	mV
$V_{MM\_DET\_OFF}$	Cell mismatch detection threshold for turning OFF	Delta between (VC2–VC1) and (VC1–GND) when cell balancing is disabled. VC2 = VDD = 7.6 V	–9	0	9	mV
$V_{CB\_EN\_ON}$	Cell balance enable ON threshold	Active LOW pin at $\overline{CB\_EN}$			1	V
$V_{CB\_EN\_OFF}$	Cell balance enable OFF threshold	Active HIGH at $\overline{CB\_EN}$	2.2			V
I_{CB_EN}	Cell balance enable ON input current	$\overline{CB\_EN}$ = GND (See Figure 8.)			0.2	µA
R_{CB1}	Internal cell balance switch resistance	$\overline{CB\_EN}$ = GND				Ω
R_{CB2}	Internal cell balance switch resistance	$\overline{CB\_EN}$ = GND				Ω

(1) Specified by design. Not 100% tested in production.

7.6 Recommended Cell Balancing Configurations

Typical values stated where T_A = 25°C and (VC2–VC1), (VC1–GND) = 3.8 V. Minimum and maximum values stated where T_A = –40°C to 110°C, VDD = 4 V to 10 V, and (VC2–VC1), (VC1–GND) = 3 V to 4.2 V. All values assume recommended supply voltage filter resistance R_{VD} of 100 Ω and 5% accurate or better cell balance resistor R_{CB}.

			MIN	NOM	MAX	UNIT
I_{CB}	Cell balance input current	R_{CB} = 4700 Ω	0.5	0.75	1	mA
		R_{CB} = 2200 Ω	1	1.5	2	
		R_{CB} = 910 Ω	2	3	4	
		R_{CB} = 560 Ω	3	4.5	6	
		R_{CB} = 360 Ω	3.5	6	8.5	
		R_{CB} = 240 Ω	4	7.5	11	
		R_{CB} = 120 Ω	5	10	15	

7.7 Typical Characteristics

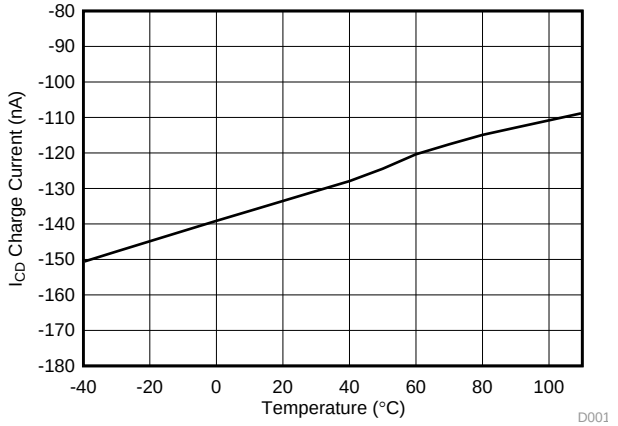


Figure 1. I_{CD} Charge Current

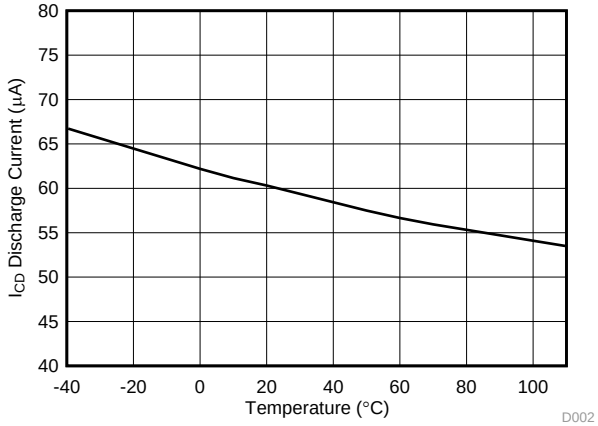


Figure 2. I_{CD} Discharge Current

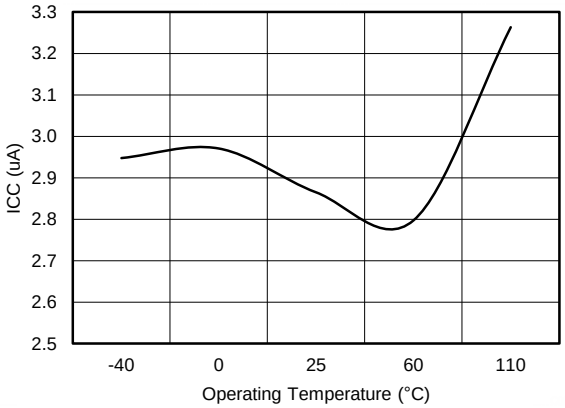


Figure 3. Average ICC During Normal Operation Across Operational Temperature

8 Detailed Description

8.1 Overview

The bq2920x provides overvoltage protection and cell balancing for 2-series cell lithium-ion battery packs.

8.1.1 Voltage Protection

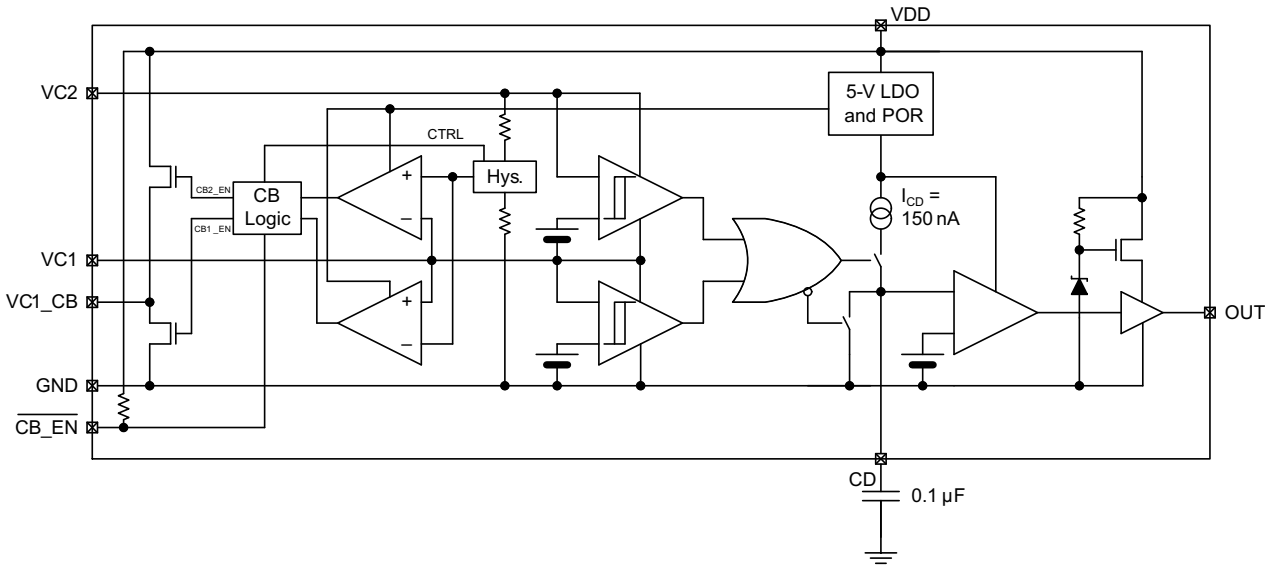
Each cell voltage is continuously compared to a factory configured internal reference threshold. If either cell reaches an overvoltage condition, the bq2920x device starts a timer that provides a delay proportional to the capacitance on the CD pin. Upon expiration of the internal timer, the OUT pin changes from a low to high state.

8.1.2 Cell Balancing

If enabled, the bq2920x performs automatic cell-balance correction where the two cells are automatically corrected for voltage imbalance by loading the cell with the higher voltage with a small balancing current. When the cells are measured to be equal within nominally 0 mV, the load current is removed. It will be re-applied if the imbalance exceeds nominally 30 mV. The cell mismatch correction circuitry is enabled by pulling the $\overline{\text{CB\_EN}}$ pin low, and disabled when $\overline{\text{CB\_EN}}$ is pulled to greater than 2.2 V, for example, VDD.

If the internal cell balancing current of up to 15 mA is insufficient, the bq2920x may be configured via external circuitry to support much higher external cell balancing current.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Protection (OUT) Timing

Sizing the external capacitor is based on the desired delay time as follows:

$$C_{CD} = \frac{t_d}{X_{DELAY}}$$

Where t_d is the desired delay time and X_{DELAY} is the overvoltage delay time scale factor, expressed in seconds per microFarad. X_{DELAY} is nominally 9 s/µF. For example, if a nominal delay of 3 seconds is desired, use a C_{CD} capacitor that is 3 s / 9 s/µF = 0.33 µF.

The delay time is calculated as follows:

$$t_d = C_{CD} \times X_{DELAY}$$

Feature Description (continued)

If the cell overvoltage condition is removed before the external capacitor reaches the reference voltage, the internal current source is disabled and an internal discharge block is employed to discharge the external capacitor down to 0 V. In this instance, the OUT pin remains in a low state.

8.3.2 Cell Voltage > $V_{PROTECT}$

When one or both of the cell voltages rises above $V_{PROTECT}$, the internal comparator is tripped, and the delay begins to count to t_d. If the input remains above $V_{PROTECT}$ for the duration of t_d, the bq2920x output changes from a low to a high state, by means of an internal pull-up network, to a regulated voltage of no more than 9.5 V when I_{OH} = 0 mA.

The external delay capacitor should charge up to no more than the internal LDO voltage (approximately 5 V typically), and will fully discharge in approximately under 100 ms when the overvoltage condition is removed.

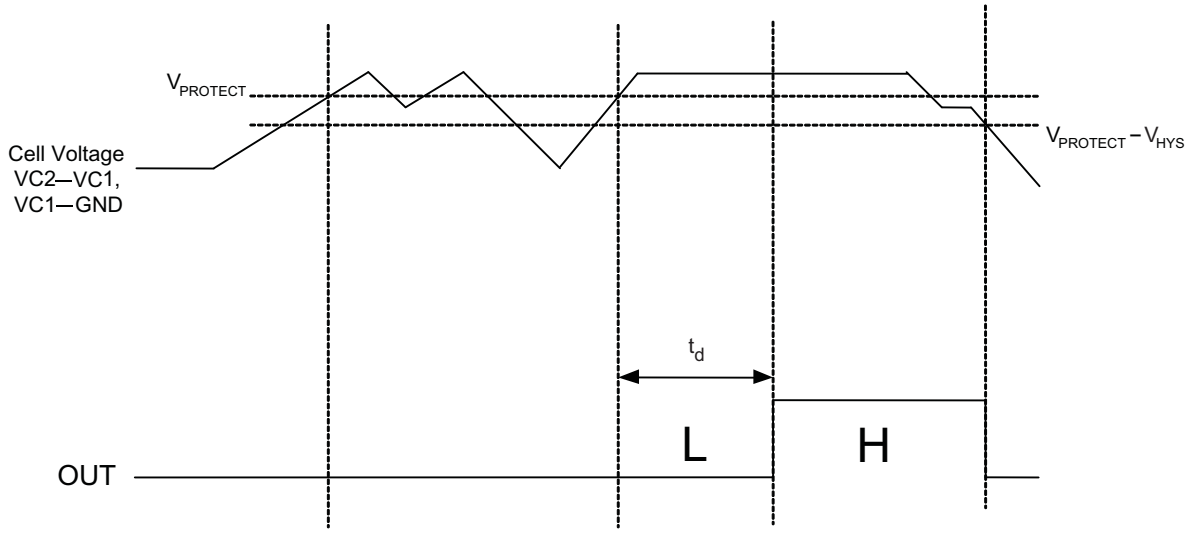


Figure 4. Timing for Overvoltage Sensing

8.3.3 Cell Connection Sequence

NOTE

Before connecting the cells, populate the overvoltage delay timing capacitor, C_{CD}.

The recommended cell connection sequence begins from the bottom of the stack, as follows:

1. GND
2. VC1
3. VC2

While not advised, connecting the cells in a sequence other than that described above does not result in errant activity on the OUT pin. For example:

1. GND
2. VC2 or VC1
3. Remaining VCx pin

8.3.4 Cell Balance Enable Control

To avoid prematurely discharging the cells, it is recommended to turn off (pull high) the active-low Cell Balance Enable Control pin at lower State of Charge (SOC) levels.

Feature Description (continued)

8.3.5 Cell Balance Configuration

The cell balancing current may be calculated as follows:

For Cell 1 (VC1–GND) balancing current, I_{CB1}:

$$I_{CB1} = \frac{VC1}{R_{CB} + R_{CB1}} \quad (1)$$

For Cell 2 (VC2–VC1) balancing current, I_{CB2}:

$$I_{CB2} = \frac{(VC2 - VC1)}{(R_{CB} + R_{VD}) + R_{CB2}} \quad (2)$$

Where:

RCB = resistor connected between the top of Cell 1 and the VC1_CB

RCB1 = resistor connected between the top of Cell 1 and the VC1

RCB2 = resistor connected between the top of Cell 2 and the VC2

RVD = resistor connected between the top of Cell 2 and the VDD

8.3.6 Cell Imbalance Auto-Detection (Via Cell Voltage)

The $V_{MM\_DET\_ON}$ and $V_{MM\_DET\_OFF}$ specifications are calibrated where VDD = VC2 = 7.6 V and VC1 = 3.8 V. The recommended range of cell balancing is VC2 and VDD between 6.0 V and 8.4 V, and VC1 between 3 V and 4.2 V. Below VDD = 6 V, it is recommended to pull $\overline{CB\_EN}$ high to disable the cell balancing function.

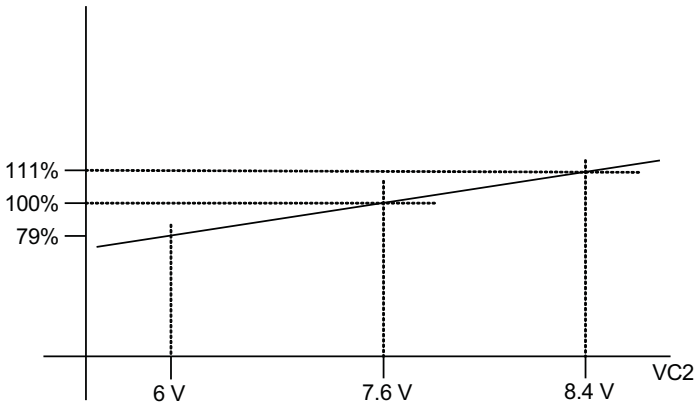


Figure 5. $V_{MM\_DET\_ON}$ and $V_{MM\_DET\_OFF}$ Threshold

8.3.7 Customer Test Mode

Customer Test Mode (CTM) helps to greatly reduce the overvoltage detection delay time and enable quicker customer production testing. This mode is intended for quick-pass board-level verification tests, and, as such, individual cell overvoltage levels may deviate slightly from the specifications ($V_{PROTECT}$, V_{OA}). If accurate overvoltage thresholds are to be tested, use the standard delay settings that are intended for normal use.

To enter CTM, VDD should be set to approximately 9.5 V higher than VC2. When CTM is entered, the device switches from the normal overvoltage delay time scale factor, X_{DELAY}, to a significantly reduced factor of approximately 0.08, thereby reducing the delay time during an overvoltage condition.

Feature Description (continued)

CAUTION

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the part into CTM. Also, avoid exceeding absolute maximum voltages for the individual cell voltages (VC1–GND) and (VC2–VC1). Stressing the pins beyond the rated limits may cause permanent damage to the device.

To exit CTM, power off the device and then power it back on.

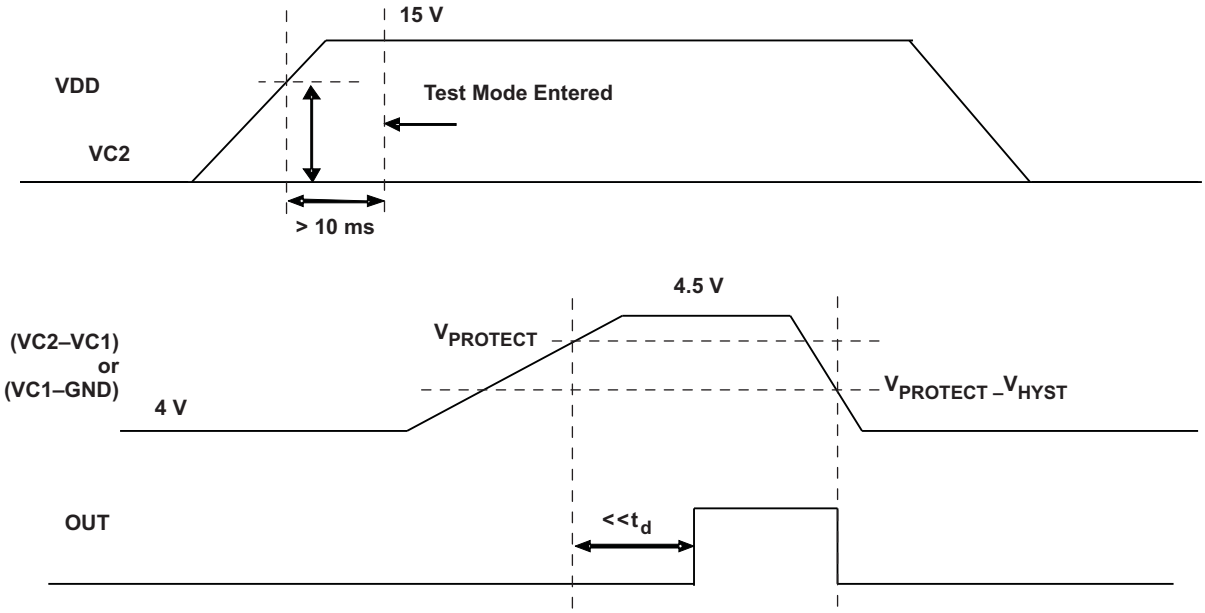


Figure 6. Voltage Test Limits

8.3.8 Test Conditions

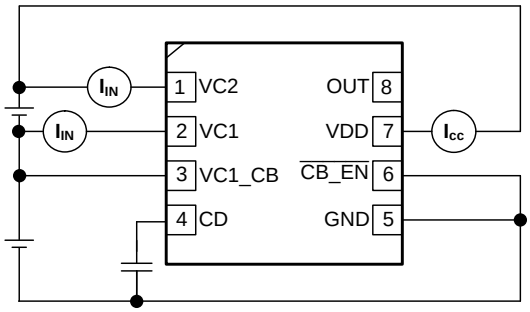


Figure 7. I_{CC}, I_{IN} Measurement

Feature Description (continued)

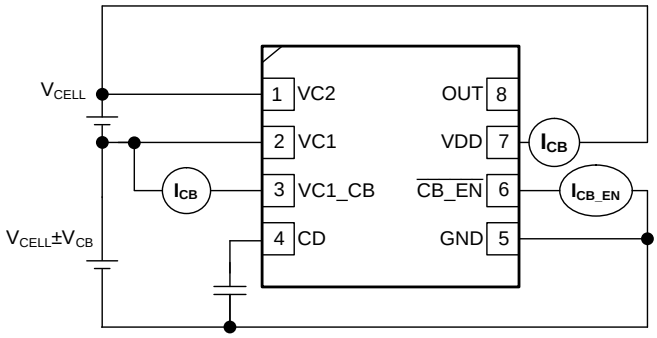


Figure 8. I_{CB} Measurement

8.4 Device Functional Modes

This device monitors the voltage of the cells connected to the VCx pins and depending on these voltages and the overall battery voltage at VDD the device enters different operating modes.

8.4.1 NORMAL Mode

The device is operating in NORMAL mode when the cell voltage range is between the over-charge detection threshold ($V_{PROTECT}$) and the minimum supply voltage.

If this condition is satisfied, the device turns OFF the OUT pin.

8.4.2 PROTECTION Mode

The device is operating in PROTECTION mode when the cell over voltage protection feature has been triggered. See *Cell Voltage > $V_{PROTECT}$* for more details on this feature.

If this condition is satisfied, the device turns ON the OUT pin.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The bq2920x is designed to be used in 2-series Li-Ion battery packs and with the option to include voltage-based cell balancing. The number of parallel cells or the overall capacity of the battery only affects the cell balancing circuit due to the level of potential imbalance that needs to be corrected.

9.2 Typical Applications

9.2.1 Battery Connection

Figure 9 shows the configuration for the 2-series cell battery connection with cell balancing enabled.

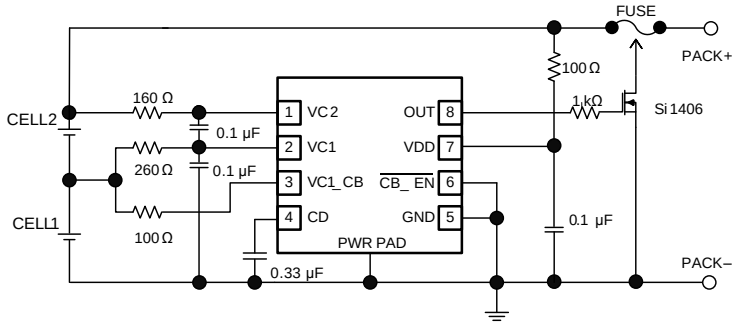


Figure 9. 2-Series Cell Configuration

9.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE at T_A = 25°C
Input voltage range	4 V to 10 V
Overvoltage Protection (OVT)	4.35 V
Overvoltage detection delay time	3 s
Overvoltage detection delay timer capacitor	0.33 µF
Cell Balancing Enabled	Yes
Cell Balancing Current, ICB1 and ICB2	10 mA
Cell Balancing Resistors, RCB, RCB1, RCB2 and RVD	RCB = 100 Ω, RCB1 = 260 Ω, RCB2 = 160 Ω, RVD = 100 Ω

9.2.1.2 Detailed Design Procedure

The bq2920x has limited features but there are some key calculations to be made when selecting external component values.

- Calculate the required CCD capacitor value for the voltage protection delay time. Care should be taken to evaluate the tolerances of the capacitor and the bq2920x to ensure system specifications are met.
- Calculate the cell balancing resistor values to provide a suitable level of balancing current that will, at a minimum, counter act an increase in imbalance during normal operation of the battery. Care should be taken to ensure any connectivity resistance is also considered as this will also reduce the balancing current level.

9.2.1.3 Application Curve

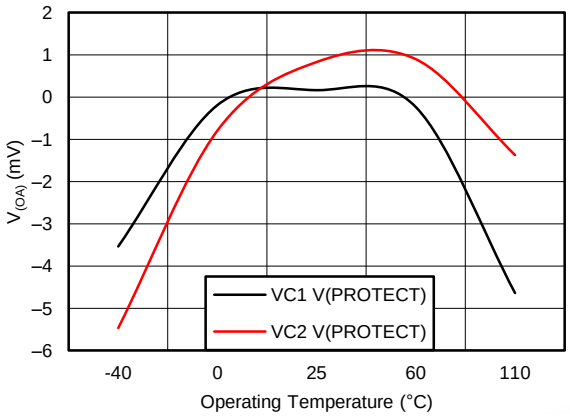


Figure 10. Average $V_{PROTECT}$ Accuracy (V_{OA}) Across Operation Temperature

9.3 System Example

9.3.1 External Cell Balancing

Higher cell balancing currents can be supported by means of a simple external network, as shown in Figure 11.

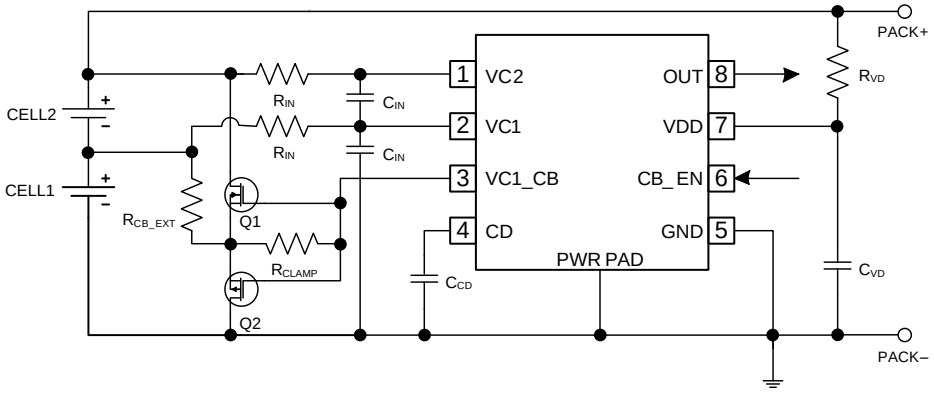


Figure 11. External Cell Balancing Configuration

R_{CLAMP} ensures that both Q1 and Q2 remain off when balancing is disabled, and should be sized above 2 kΩ to prevent excessive internal device current when the balancing network is activated. R_{CB_EXT} determines the value of the balancing current, and is dependent on the voltage of the balanced cell, as follows:

$$I_{bal} = \frac{V_{CELL}}{R_{CB\_EXT}}$$

10 Power Supply Recommendations

The recommended power supply for this device is a maximum 10-V operation on the VDD input pin.

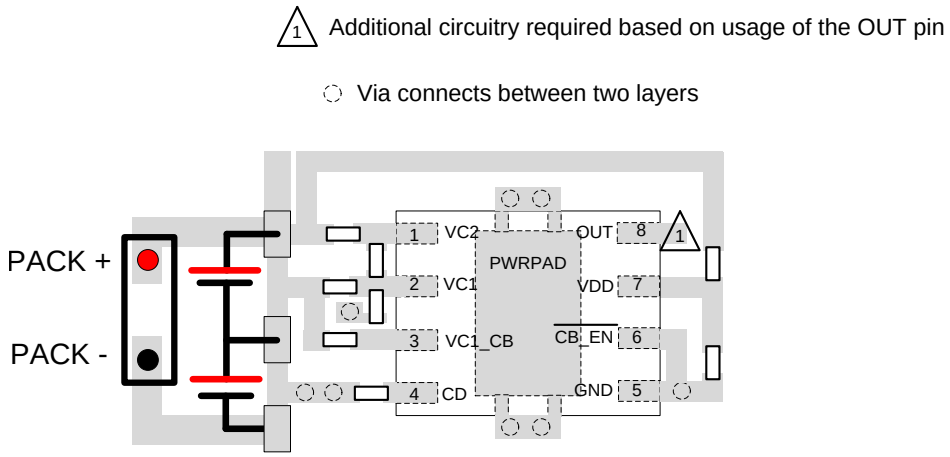
11 Layout

11.1 Layout Guidelines

The following are the recommended layout guidelines:

1. Ensure the input filters to the VC1 and VC2 pins are as close to the IC as possible to improve noise immunity.
2. If the OUT pin is used to control a high current path, for example: to blow a chemical fuse, then care should be taken to ensure the high current path creates minimal interference of the bq2920x voltage sense inputs.
3. The input RC filter on the VDD pin should be close to the terminal of the IC.

11.2 Layout Example



12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
bq29200	Click here	Click here	Click here	Click here	Click here
bq29209	Click here	Click here	Click here	Click here	Click here

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ29200DRBR	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	200
BQ29200DRBR.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	200
BQ29200DRBR.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	200
BQ29200DRBT	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	Call TI | Nipdau	Level-2-260C-1 YEAR	-40 to 85	200
BQ29200DRBT.A	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	200
BQ29200DRBT.B	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	200
BQ29209DRBR	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	209
BQ29209DRBR.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	209
BQ29209DRBT	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	209
BQ29209DRBT.A	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	209
BQ29209DRBT.B	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	209
BQ29209DRBTG4	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	209
BQ29209DRBTG4.A	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	209
BQ29209DRBTG4.B	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	209

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF BQ29209 :

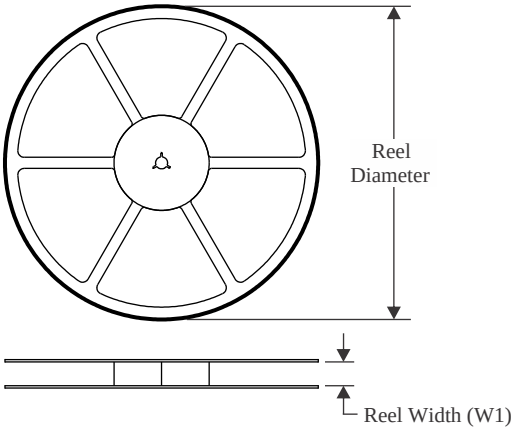
- Automotive : BQ29209-Q1

NOTE: Qualified Version Definitions:

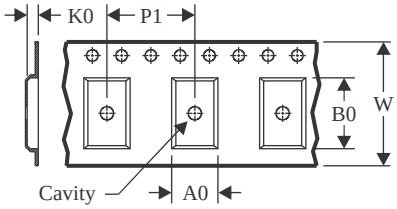
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

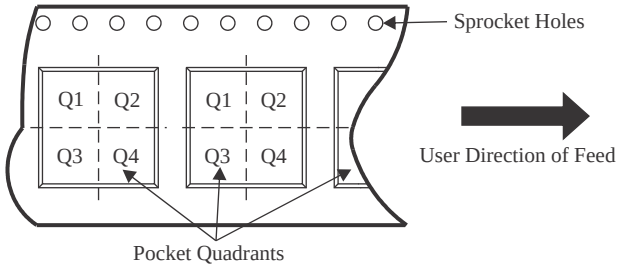


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

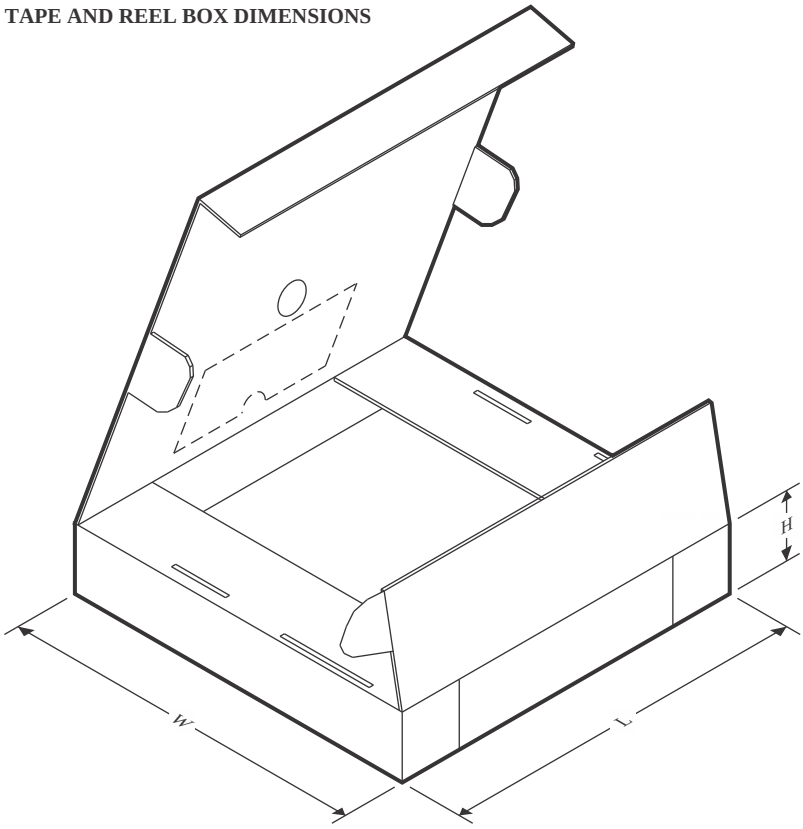
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ29200DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ29200DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ29209DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ29209DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ29209DRBTG4	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ29200DRBR	SON	DRB	8	3000	346.0	346.0	33.0
BQ29200DRBT	SON	DRB	8	250	210.0	185.0	35.0
BQ29209DRBR	SON	DRB	8	3000	346.0	346.0	33.0
BQ29209DRBT	SON	DRB	8	250	210.0	185.0	35.0
BQ29209DRBTG4	SON	DRB	8	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DRB 8

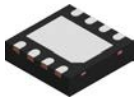
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

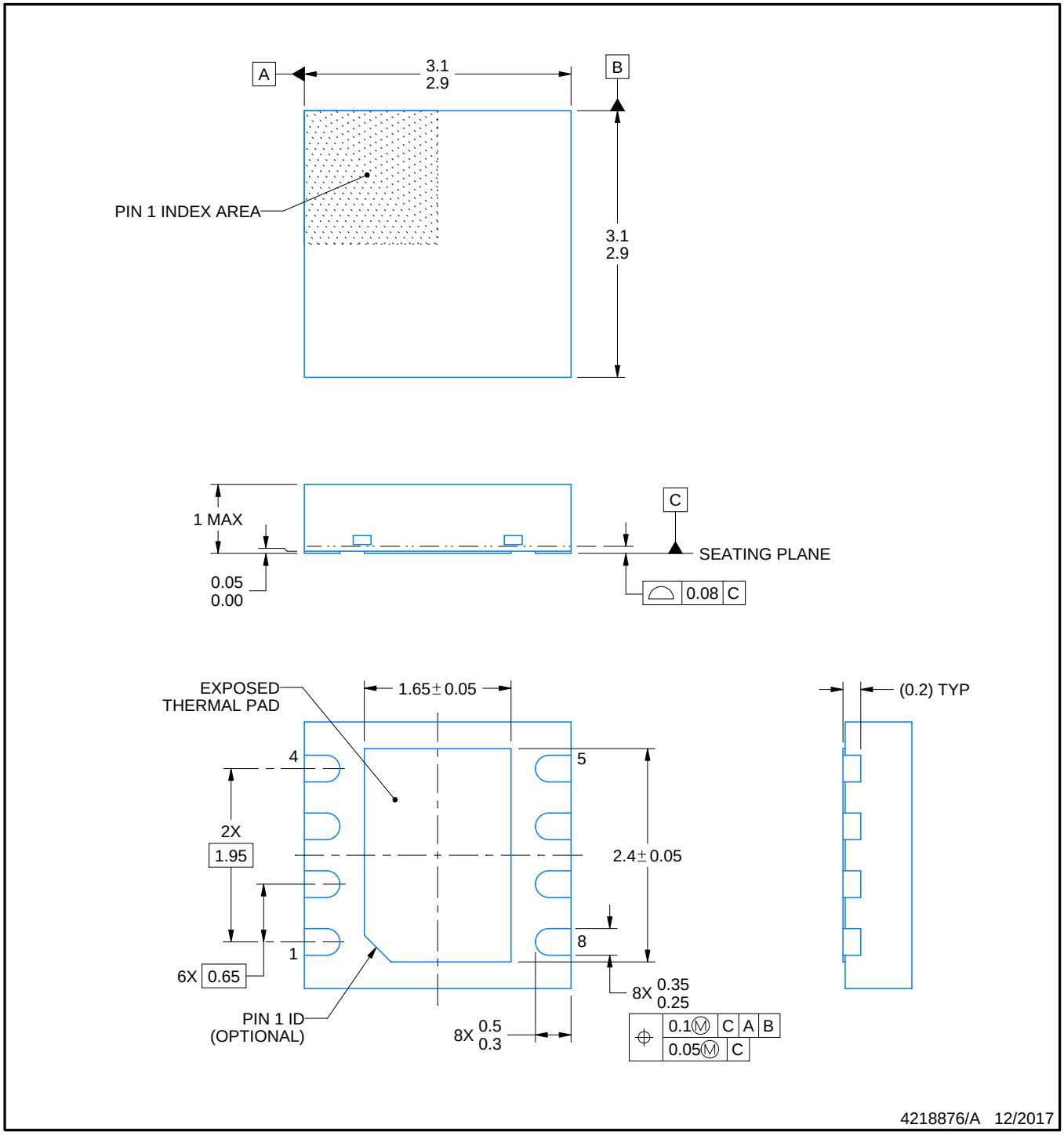
DRB0008B



PACKAGE OUTLINE

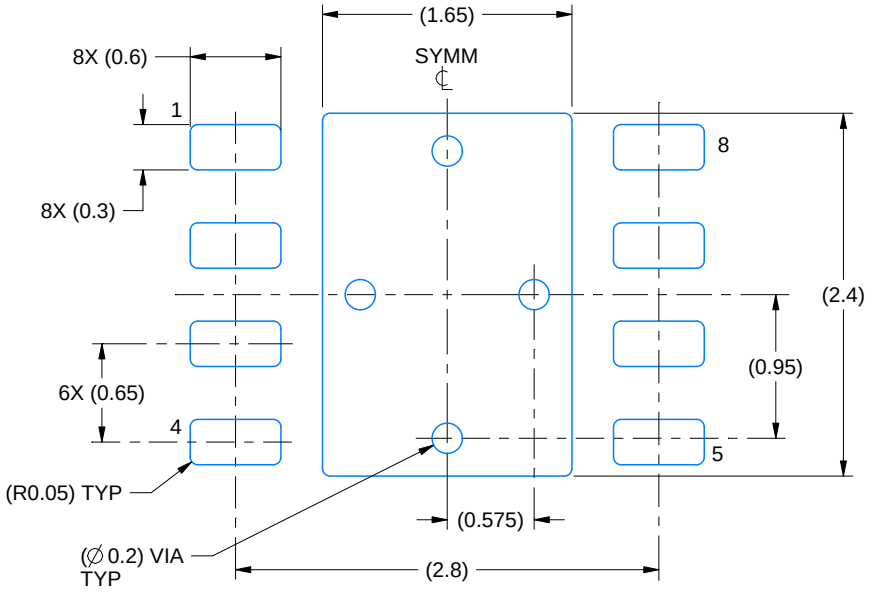
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

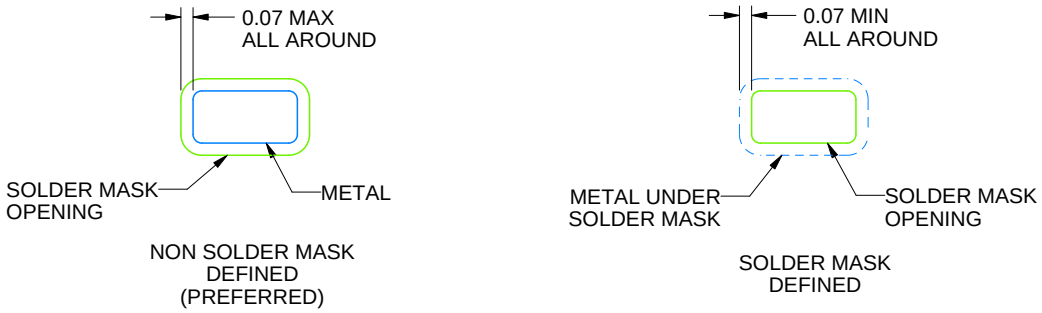


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

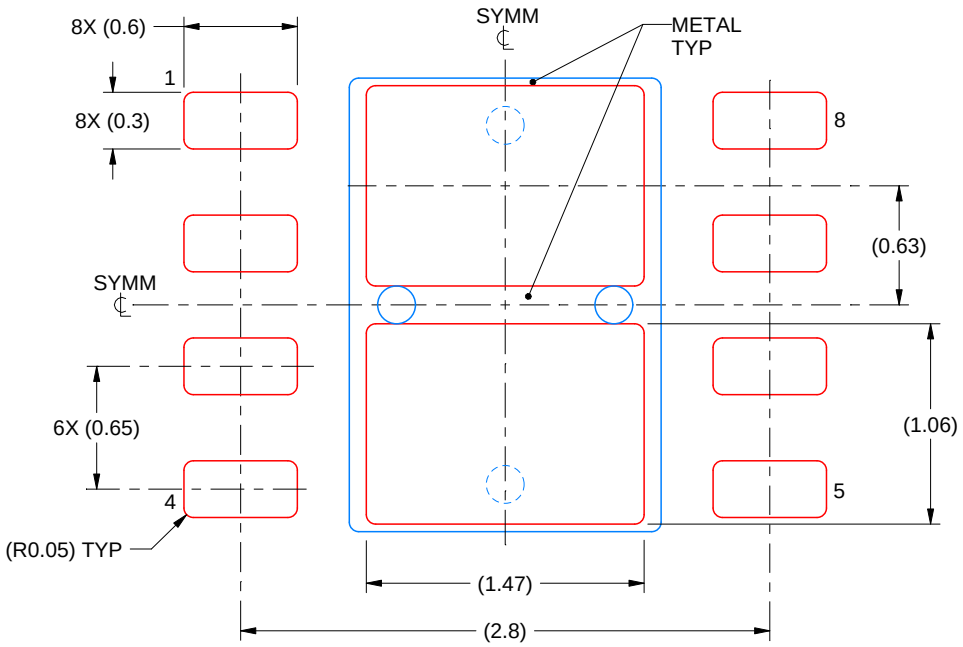


SOLDER MASK DETAILS

4218876/A 12/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218876/A 12/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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