

www.ti.com SLUSA66 –JULY 2011

1A, Single-Input, Single-Cell LiFePO₄ Linear Battery Charger with 50mA LDO

Check for Samples: bq25070

FEATURES

- Single Cell LiFePO₄ Charging Algorithm
- 30V Input Rating, With 10.5V Over-Voltage Protection (OVP)
- 50mA Integrated Low Dropout Linear Regulator (LDO)
- Programmable Charge Current Through Single Input Interface (CTRL)
- 7% Charge Current Regulation Accuracy
- · Thermal Regulation and Protection
- Soft-Start Feature to Reduce Inrush Current

- Battery NTC Monitoring
- · Charging Status Indication
- Available in Small 2mm × 3mm 10 Pin SON Package

APPLICATIONS

- Smart Phones
- Mobile Phones
- Portable Media Players
- Low Power Handheld Devices

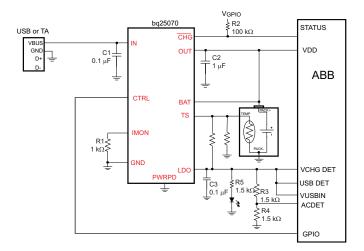
DESCRIPTION

The bq25070 is a highly integrated LiFePO₄ linear battery charger targeted at space-limited portable applications. It operates from either a USB port or AC Adapter and charges a single-cell LiFePO₄ battery with up to 1A of charge current. The 30V input voltage range with input over-voltage protections supports low-cost unregulated adapters.

The bq25070 has a single power output that charges the battery and powers the system. The charge current is programmable up to 1A using the CTRL input. Additionally, a 4.9V ±10% 50mA LDO is integrated into the IC for supplying low power external circuitry.

The LiFePO₄ charging algorithm removes the constant voltage mode control usually present in Li-Ion battery charge cycles. Instead, the battery is fastcharged to the overcharge voltage and then allowed to relax to a lower float charge voltage threshold. The removal of the constant voltage control reduces charge time significantly. During the charge cycle, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded. The charger power stage and charge current sense functions are fully integrated. The charger function has high accuracy current and voltage regulation loops, and charge status display.

APPLICATION SCHEMATIC





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

PART NUMBER	I _{LIM(DEF)}	V _{BAT(OVCH)}	V _{BAT(FLOAT)}	V _{OVP}	V_{LDO}	MARKING
bq25070DQCR	300 mA	3.7 V	3.5 V	10.5 V	4.9 V	QUS
bq25070DQCT	300 mA	3.7 V	3.5 V	10.5 V	4.9 V	QUS

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on ti.com (www.ti.com),

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Innut Valtage	IN (with respect to GND)	-0.3 to 30	V
Input Voltage	CTRL, TS (with respect to GND)	-0.3 to 7	V
Output Voltage	BAT, OUT, LDO, CHG, IMON (with respect to GND)	-0.3 to 7	V
Input Current (Continuous)	IN	1.2	Α
Output Current (Continuous)	BAT	1.2	Α
Output Current (Continuous)	LDO	100	mA
Output Sink Current	CHG	5	mA
Junction temperature, T _J		-40 to 150	°C
Storage temperature, T _{STG}		-65 to 150	°C

⁽¹⁾ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

THERMAL INFORMATION

		bq25070	
	THERMAL METRIC ⁽¹⁾	SON	UNITS
		10 PINS	
θ _{JA} Junction-to-ambie	ent thermal resistance ⁽²⁾	58.7	°C/W
θ _{JCtop} Junction-to-case	(top) thermal resistance (3)	3.9	C/VV

- (1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNITS
\/	IN voltage range	3.75 ⁽¹⁾	28	V
V_{IN}	IN operating voltage range	3.75 ⁽¹⁾	10.2	V
I _{IN}	Input current, IN		1	Α
I _{OUT}	Output Current in charge mode, OUT		1	Α
T_{J}	Junction Temperature	0	125	°C

(1) Charge current may be limited at low input voltages due to the dropout of the device.

www.ti.com SLUSA66 -JULY 2011

ELECTRICAL CHARACTERISTICS

Over junction temperature range $0^{\circ}C \le T_{J} \le 125^{\circ}C$ and recommended supply voltage (unless otherwise noted)

· ·	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT			•		l	
V _{UVLO}	Under-voltage lock-out	V_{IN} : 0 V \rightarrow 4 V	3.15	3.30	3.55	V
V _{HYS-UVLO}	Hysteresis on UVLO	V_{IN} : 4 V \rightarrow 0 V		250		mV
V _{BATUVLO}	Battery UVLO	V _{BAT} rising	1.95	2.05	2.15	V
V _{HYS-BUVLO}	Hysteresis on BAT UVLO	V _{BAT} falling		125		mV
V _{IN-SLP}	Valid input source threshold V _{IN-SLP} above VBAT	Input power good if $V_{IN} > V_{BAT} + V_{IN-SLP}$ $V_{BAT} = 3.6 \text{ V}, V_{IN}: 3.5 \text{ V} \rightarrow 4 \text{ V}$	30	75	150	mV
V _{HYS-INSLP}	Hysteresis on V _{IN-SLP}	V_{BAT} = 3.6 V, V_{IN} : 4 V \rightarrow 3.5 V	18	32	54	mV
t _{DGL(NO-IN)}	Delay time, input power loss to charger turn-off	Time measured from V _{IN} : 5 V \rightarrow 2.5 V 1 μ s fall-time		32		ms
V _{OVP}	Input over-voltage protection threshold	V _{IN} : 5 V → 11 V	10.2	10.5	10.8	V
V _{HYS-OVP}	Hysteresis on OVP	V _{IN} : 11 V → 5 V		100		mV
t _{BLK(OVP)}	Input over-voltage blanking time			100		μs
t _{REC(OVP)}	Input over-voltage recovery time	Time measured from V _{IN} : 11 V \rightarrow 5 V 1 μ s fall-time to LDO = HI, V _{BAT} = 3.5 V		100		μs
QUIESCENT	CURRENT					
		$V_{IN} = 0 \text{ V}, V_{\overline{CHG}} = \text{High, TS Enabled}$		120	150	μA
I _{BAT(PDWN)}	Battery current into BAT, No input connected	$V_{IN} = 0 \text{ V}, V_{\overline{CHG}} = \text{Low, TS Disabled,}$ $T_J = 85^{\circ}\text{C}$			6	μΑ
		$CTRL = HI, V_{IN} = 5.5V$			0.25	
I _{IN(STDBY)}	Standby current into IN pin	$CTRL = HI, V_{IN} \le V_{OVP}$			0.5	mA
		CTRL = HI, V _{IN} > V _{OVP}			2	
ICC	Active supply current, IN pin	V _{IN} = 6 V, No load on OUT pin, V _{BAT} > V _{BAT(REG)} , IC enabled			3	mA
BATTERY C	HARGER FAST-CHARGE					
V	Pottory float charge valtage	$T_A = 0$ °C to 125°C	3.465	3.5	3.535	V
$V_{BAT(REG)}$	Battery float charge voltage	$T_A = 25^{\circ}C$	3.465	3.5	3.529	V
V _{BAT(OVCH)}	Battery overcharge voltage threshold		3.62	3.7	3.78	V
		4 pulses on CTRL	87	93	100	
		5 pulses on CTRL	174	187	200	
		6 pulses on CTRL	261	280	300	
ı	Input Current Limit (selected by CTRL	7 pulses on CTRL	348	374	400	mA
I _{IN(LIM)}	interface)	8 pulses on CTRL	435	467	500	ША
		9 pulses on CTRL				
		10 pulses on CTRL	739	794	850	
		11 pulses on CTRL	869	935	1000	
$V_{DO(IN-OUT)}$	V _{IN} – V _{OUT}	$V_{IN} = 3.5 \text{ V}, I_{OUT} = 0.75 \text{ A}$		500	1400	mV
K _{IMON}	Input current monitor ratio	$K_{IMON} = I_{IMON} / I_{CHG}, R_{IMON} = 1k\Omega,$ Current programmed using CTRL		1		mA / A
V _{IMON(MAX)}	Maximum IMON voltage	IMON open		1.2	1.25	V
·	IMON Acquirecy	I _{IN} < 100 mA	-25%		25%	
	IMON Accuracy	I _{IN} = 100 mA to 1 A	-10%		10%	
PRE-CHARG	E AND CHARGE DONE					
V_{LOWV}	Pre-charge to fast-charge transition threshold		2.4	2.5	2.6	V
t _{DGL1(LOWV)}	Deglitch time on pre-charge to fast-charge transition			25		ms
t _{DGL2(LOWV)}	Deglitch time on fast-charge to pre-charge transition			25		ms



ELECTRICAL CHARACTERISTICS (continued)

Over junction temperature range $0^{\circ}C \le T_{J} \le 125^{\circ}C$ and recommended supply voltage (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I _{PRECHARGE}	Precharge current to BAT during precharge mode	V _{BAT} = 0 V to 0.7 V	41.5	45	48.5	mA
RECHARGE	OR REFRESH				•	
V _{RCH}	Recharge detection threshold	V _{BAT} falling	3.1	3.3	3.5	V
t _{DGL(RCH)}	Deglitch time, recharge threshold detected	V _{BAT} falling to New Charge Cycle		25		ms
LDO						
V_{LDO}	LDO Output Voltage	V _{IN} = 5 V to 10.5 V, I _{LDO} = 0 mA to 50 mA	4.7	4.9	5.1	V
I _{LDO}	Maximum LDO Output Current		60			mA
V_{DO}	Dropout Voltage	V _{IN} = 4.5V, ILDO = 50mA		200	350	mV
CTRL INTER	FACE					
t _{CTRL_DGL}	CTRL Deglitch timer		5			ms
t _{CTRL_LATCH}	CTRL Latch timer		2			ms
t _{HI_MIN}	High Duration on CTRL		50		1000	μs
t _{LO_MIN}	Low Time Duration on CTRL		50		1000	μs
R _{PULLDOWN}	CTRL Pulldown Resistor			260		kΩ
LOGIC LEVE	LS ON CTRL					
V _{IL}	Logic LOW input voltage				0.4	V
V_{IH}	Logic HIGH input voltage		1.4			V
BATTERY-PA	ACK NTC MONITOR (TS)					
V _{COLD}	TS Cold Threshold	V _{TS} Rising	24.5	25	25.5	%V _{LDO}
V _{CUTOFF}	TS Cold Cutoff Threshold	V _{TS} Falling		1		%V _{LDO}
V _{HOT}	TS Hot Threshold	V _{TS} Falling	12	12.5	13	$%V_{LDO}$
V _{HOT_HYS}	TS Hot Cutoff Threshold	V _{TS} Rising		1		%V _{LDO}
t _{dgl(TS)}	Deglitch for TS Fault	Fault detected on TS to stop charge		25		ms
CHG OUTPU	т					
V _{OL}	Output LOW voltage	I _{SINK} = 1 mA			0.45	V
I _{IH}	Leakage current	CHG = 5 V			1	μΑ
t _{FLSH(TS)}	TS fault flash period	50% Duty Cycle, TS out of valid range		100		ms
THERMAL R	EGULATION					
$T_{J(REG)}$	Temperature Regulation Limit	T _J rising		125		С
T _{J(OFF)}	Thermal shutdown temperature	T _J rising		155		С
T _{J(OFF-HYS)}	Thermal shutdown hysteresis	T _J falling		20		С



www.ti.com SLUSA66 -JULY 2011

TYPICAL CHARACTERISTICS

 $V_{IN} = 5 \text{ V}, V_{BAT} = 3.2 \text{ V}, I_{\overline{CHG}} = 280 \text{ mA}, Typical Application Circuit}$

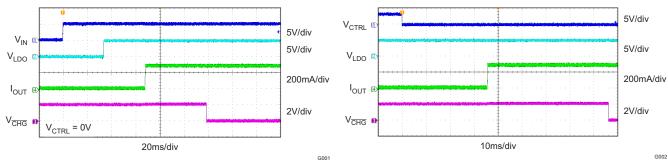


Figure 1. Adapter Plug-In With Battery Connected

Figure 2. Charger Enable Using CTRL

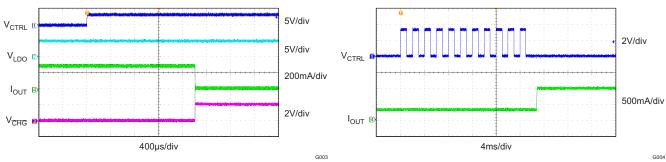


Figure 3. Charger Disable Using CTRL

Figure 4. Default to 1A Transition Using CTRL

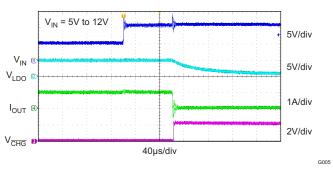


Figure 5. OVP Fault

TYPICAL CHARACTERISTICS (continued)

 $V_{IN} = 5 \text{ V}$, $V_{BAT} = 3.2 \text{ V}$, $I_{\overline{CHG}} = 280 \text{ mA}$, Typical Application Circuit

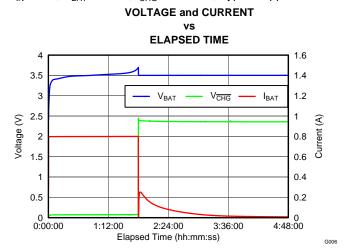
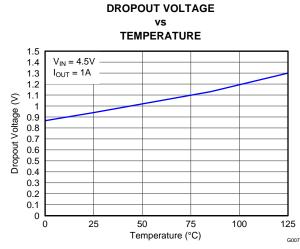
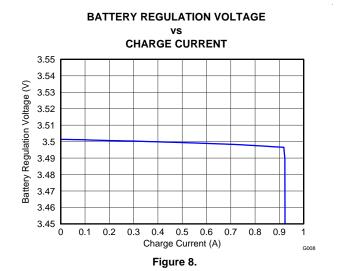


Figure 6. Complete Charge Cycle

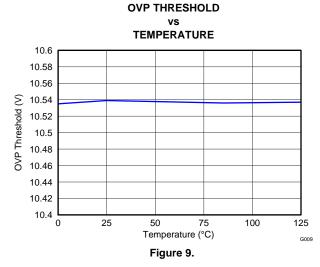


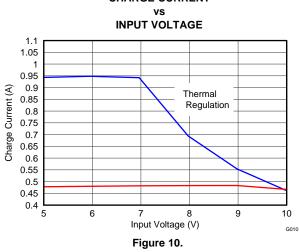
NSTRUMENTS

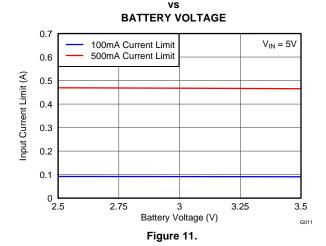
Figure 7.



CHARGE CURRENT





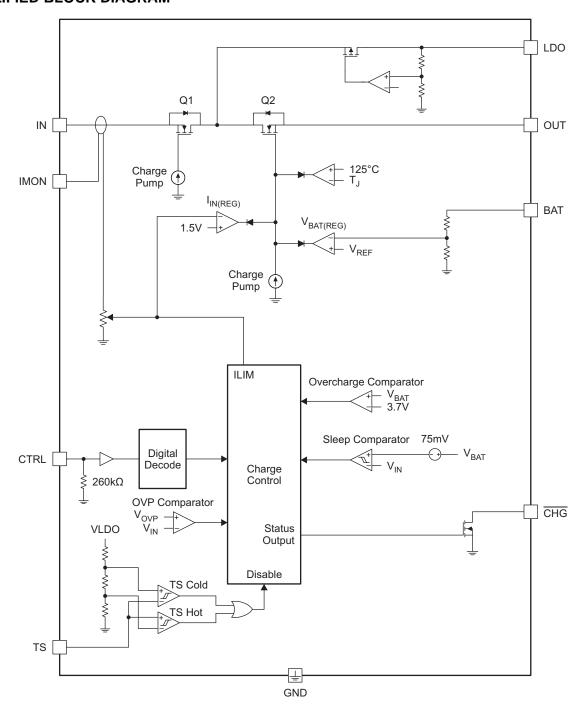


INPUT CURRENT LIMIT

SLUSA66 -JULY 2011

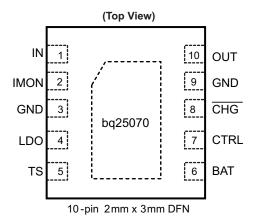


SIMPLIFIED BLOCK DIAGRAM





PIN CONFIGURATION



PIN FUNCTIONS

PIN		1/0						
NAME	NO.		DESCRIPTION					
IN	1	I	Input power supply. IN is connected to the external DC supply (AC adapter or USB port). Bypass IN to GND with at least a 0.1µF ceramic capacitor.					
IMON	2	0	Current monitoring output. Connect a $1k\Omega$ resistor from IMON to GND to monitor the input current. The voltage at IMON ranges from 0V to 1V which corresponds to an input current from 0A to 1A.					
GND	3, 9	_	Ground terminal. Connect to the thermal pad and the ground plane of the circuit.					
LDO	4	0	LDO output. LDO is regulated to 4.9V and drives up to 50mA. Bypass LDO to GND with a $0.1\mu F$ ceramic capacitor. LDO is enabled when $V_{UVLO} < V_{IN} < V_{OVP}$.					
TS	5	I	Battery pack NTC monitoring input. Connect a resistor divider from LDO to GND with TS connected to the center tap to set the charge temperature window. The battery pack NTC is connected in parallel with the bottom resistor of the divider. See the Applications Design section for details on the selecting the proper component values.					
BAT	6	0	Battery connection output. BAT is the sense input for the battery. Connect BAT and OUT to the battery and bypass to GND with a 1µF ceramic capacitor.					
CTRL	7	I	Single-input interface Input. Drive CTRL with pulses to enable/disable the device, enable/disable V _{IN} -DPM, and select current limits. See the interface section for details on using the CTRL interface.					
CHG	8	0	Charge status indicator open-drain output. $\overline{\text{CHG}}$ is pulled low while the device is charging the battery. $\overline{\text{CHG}}$ goes high impedance when the battery is fully charged.					
OUT	10	0	System output connection. Connect OUT and BAT together. Bypass the OUT and BAT connection to GND with a 1µF ceramic capacitor.					
Thermal PAD	Pad	-	There is an internal electrical connection between the exposed thermal pad and the GND pin of the device. The thermal pad must be connected to the same potential as the GND pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. GND pin must be connected to ground at all times.					

www.ti.com SLUSA66 -JULY 2011

APPLICATIONS CIRCUITS

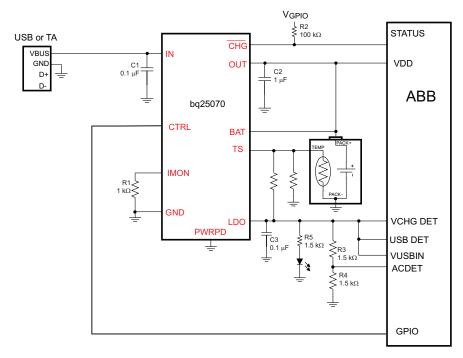


Figure 12. bq25070 Typical Application Circuit



DETAILED FUNCTIONAL DESCRIPTION

The bq25070 is a highly integrated LiFePO₄ linear battery charger targeted at space-limited portable applications. It operates from either a USB port or AC Adapter and charges a single-cell LiFePO₄ battery with up to 1A of charge current. The 30V input voltage range with input over-voltage protections supports low-cost unregulated adapters.

The LiFePO₄ charging algorithm removes the constant voltage mode control usually present in Li-Ion battery charge cycles. Instead, the battery is charged with the fastcharge current to the overcharge voltage and then allowed to relax to a lower float charge voltage threshold. The removal of the constant voltage control reduces charge time significantly. During the charge cycle, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded. The charger power stage and charge current sense functions are fully integrated. The charger function has high accuracy voltage and current regulation loops, and charge status display.

CHARGING OPERATION

The bq25070 uses a charge algorithm that is unique to LiFePO₄ chemistry cells. The constant voltage mode control usually present in Li-Ion battery charge cycles is eliminated. This dramatically decreases the charge time. When the bq25070 is enabled by CTRL, the battery voltage is monitored to verify which stage of charging must be used. When $V_{BAT} < V_{LOWV}$, the bq25070 charges in precharge mode; when $V_{BAT} > V_{LOWV}$, the normal charge cycle is used.

Charger Operation with Minimum System Voltage Mode Enabled

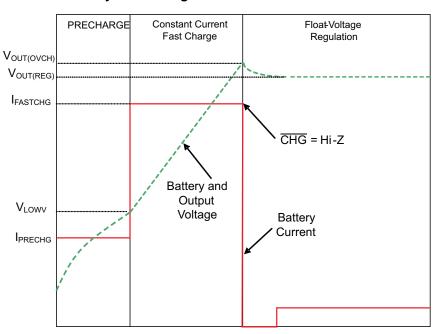


Figure 13. Typical Charging Cycle with Minimum System Voltage Enabled

Precharge Mode (V_{BAT} ≤ V_{LOWV})

The bq25070 enters precharge mode when $V_{BAT} \le V_{LOWV}$. Upon entering precharge mode, the battery is charged with a 47.5mA current and CHG goes low.

www.ti.com SLUSA66 - JULY 2011

Fast Charge Mode

Once $V_{BAT} > V_{LOWV}$, the bq25070 enters constant current (CC) mode where charge current is regulated using the internal MOSFETs between IN and OUT. The total current is shared between the output load and the battery. Once the battery voltage charges up to $V_{BAT(OVCH)}$, the \overline{CHG} output goes high indicating the charge cycle is complete and the bq25070 switches the battery regulation voltage to $V_{BAT(REG)}$. The battery voltage is allowed to relax down to $V_{BAT(REG)}$. The charger remains enabled and regulates the output to $V_{BAT(REG)}$. If at any time the battery falls below V_{REC} , the charge cycle restarts.

CHARGE CURRENT TRANSLATOR (IMON)

When the charger is enabled, internal circuits generate a current proportional to the charge current at the IMON input. The current out of IMON is 1/1000 ($\pm 10\%$) of the charge current. This current, when applied to the external charge current programming resistor, R1 (Figure 12), generates an analog voltage that can be monitored by an external host to calculate the current sourced from BAT. Connect a $1k\Omega$ resistor from IMON to GND. The voltage at IMON is calculated as:

$$V_{\rm IMON} = I_{\rm IN} \times 1 \, V_{\rm A} \tag{1}$$

INPUT OVER VOLTAGE PROTECTION

The bq25070 contains an input over voltage protection circuit that disables the LDO output and charging when the input voltage rises above V_{OVP} . This prevents damage from faulty adapters. The OVP circuitry contains an 115µs deglitch that prevents ringing on the input from line transients from tripping the OVP circuitry falsely. If an adapter with an output greater than V_{OVP} is plugged in, the IC completes soft-start power up and then shuts down if the voltage remains above V_{OVP} after 115µs. The LDO remains off and charging remains disabled until the input voltage falls below V_{OVP} .

UNDER-VOLTAGE LOCKOUT (UVLO)

The bq25070 remains in power down mode when the input voltage is below the under-voltage lockout threshold (V_{UVLO}) . During this mode, the control input (CTRL) is ignored. The LDO, the charge FET connected between IN and OUT are off and the status output (CHG) is high impedance. Once the input voltage rises above V_{UVLO} , the internal circuitry is turned on and the normal operating procedures are followed.

EXTERNAL NTC MONITORING (TS)

The bq25070 features a flexible, voltage based external battery pack temperature monitoring input. The TS input connects to the NTC thermistor in the battery pack to monitor battery temperature and prevent dangerous over-temperature conditions. During charging, the voltage at TS is continuously monitored. If, at any time, the voltage at TS is outside of the operating range (V_{COLD} to V_{HOT}), charging is suspended. When the voltage measured at TS returns to within the operation window, charging is resumed. When charging is suspended due to a battery pack temperature fault, the CHG output remains low and continues to indicate charging.

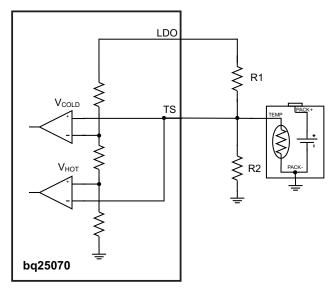
The temperature thresholds are programmed using a resistor divider from LDO to GND with the NTC thermistor connected to the center tap from TS to GND. See Figure 14 for the circuit example. The value of R1 and R2 are calculated using the following equations:

$$R1 = \frac{-R2 \times RHOT \times (0.125 - 1)}{0.125 \times (R2 + RHOT)}$$
(2)

$$R2 = \frac{-RHOT \times RCOLD \times (0.125 - 0.250)}{RHOT \times 0.250 \times (0.125 - 1) + RCOLD \times 0.125 \times (1 - 0.250)}$$
(3)

RHOT is the expected thermistor resistance at the programmed hot threshold; RCOLD is the expected thermistor resistance at the programmed cold threshold.





For applications that do not require the TS monitoring function, set R1 = $490k\Omega$ and R2 = $100k\Omega$ to set the TS voltage at a valid level and maintain charging.

Figure 14. NTC Monitoring Function

50 mA LDO (LDO)

The LDO output of the bq25070 is a low dropout linear regulator (LDO) that supplies up to 50mA while regulating to V_{LDO} . The LDO is active whenever the input voltage is above V_{UVLO} and below V_{OVP} . It is not affected by the CTRL input. The LDO output is used to power and protect circuitry such as USB transceivers from transients on the input supply.

CHARGE STATUS INDICATOR (CHG)

The bq25070 contains an open drain $\overline{\text{CHG}}$ out<u>put that indicates when charge cycles and faults. When charging a battery in precharge or fastcharge mode, the CHG output is pulled to GND. Once the BAT output reaches the overcharge voltage threshold, $\overline{\text{CHG}}$ goes high impedance to signal the battery is fully charged. The $\overline{\text{CHG}}$ output goes low during battery recharge cycles to signal the host.</u>

Additionally, \overline{CHG} notifies the host if a NTC temperature fault has occurred. \overline{CHG} pulses with a period of 100ms and a 50% duty cycle if a TS faults occurs. Connect \overline{CHG} to the required logic level voltage through a $1k\Omega$ to $100k\Omega$ resistor to use the signal with a microprocessor. $I_{\overline{CHG}}$ must be below 5mA.

The IC monitors the CHG pin when no input is connected to verify if the system circuitry is active. If the voltage at CHG is logic being drive low when no input is connected, the TS circuit is turned off for a low quiescent current state. Once the voltage at CHG increases above logic high, the TS circuit is turned on.

SINGLE INPUT INTERFACE (CTRL)

CTRL is used to enable/disable the device as well as select the input current limit, enable/disable charge, extend the TS operation range and disable V_{IN} -DPM mode. CTRL is pulled low to enable the device. After the 50µs deglitch expires, the IC enters the 32ms WAIT state. CTRL may be used to program the bq25070 during this time. Once t_{WAIT} expires, the IC starts up. If no command is sent to CTRL during t_{WAIT} , the IC starts up with a default 285mA current limit.

Programming the different modes is done by pulsing the CTRL input. See Table 1 for a map of the different modes. The width of the CTRL pulses is unimportant as long as they are between 50µs and 1000µs long. The time between pulses must be between 50µs and 1000µs to be properly read. Once CTRL is held low for 2ms, the number of pulses is passed to the control logic and decoded and then the mode changes. To ensure proper operation, do not send more than 16 pulses in one programming cycle.



www.ti.com SLUSA66 -JULY 2011

# of Pulses	Current Limit					
1	No Change					
2	No Change					
3	No Change					
4	93 mA					
5	187 mA					
6	280 mA					
7	374 mA					
8	467 mA					
9	654 mA					
10	794 mA					
11	935 mA					
>11	No Change					

Table 1. Pulse Counting Map for CTRL Interface

If, at any time, the CTRL input is held high for more than 2ms, the IC is disabled. When disabled, charging is suspended and the bq25070 input quiescent current is reduced.

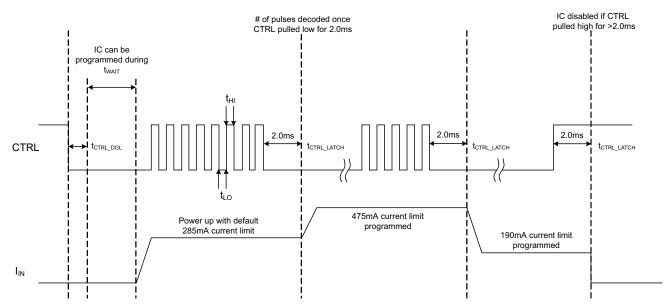


Figure 15. CTRL Timing Diagram

THERMAL REGULATION AND THERMAL SHUTDOWN

The bq25070 contains a thermal regulation loop that monitors the die temperature continuously. If the temperature exceeds $T_{J(REG)}$, the device automatically reduces the charging current to prevent the die temperature from increasing further. In some cases, the die temperature continues to rise despite the operation of the thermal loop, particularly under high V_{IN} conditions. If the die temperature increases to $T_{J(OFF)}$, the IC is turned off. Once the device die temperature cools by $T_{J(OFF-HYS)}$, the device turns on and returns to thermal regulation. Continuous over-temperature conditions result in the pulsing of the load current. If the junction temperature of the device exceeds $T_{J(OFF)}$, the charge FET is turned off. The FET is turned back on when the junction temperature falls below $T_{J(OFF)} - T_{J(OFF-HYS)}$.

Note that these features monitor the die temperature of the bq25070. This is not synonymous with ambient temperature. Self heating exists due to the power dissipated in the IC because of the linear nature of the battery charging algorithm.



APPLICATION INFORMATION

SELECTION OF INPUT/OUTPUT CAPACITORS

In most applications, all that is needed is a high-frequency decoupling capacitor on the input power pin. For normal charging applications, a 0.1µF ceramic capacitor, placed in close proximity to the IN pin and GND pad works best. In some applications, depending on the power supply characteristics and cable length, it may be necessary to increase the input filter capacitor to avoid exceeding the OVP voltage threshold during adapter hot plug events where the ringing exceeds the deglitch time.

The charger in the bq25070 requires a capacitor from OUT to GND for loop stability. Connect a 1µF ceramic capacitor from BAT to GND close to the pins for best results. More output capacitance may be required to minimize the output droop during large load transients.

The LDO also requires an output capacitor for loop stability. Connect a 0.1µF ceramic capacitor from LDO to GND close to the pins. For improved transient response, this capacitor may be increased.

THERMAL CONSIDERATIONS

The bq25070 is packaged in a thermally enhanced QFN package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB). Full PCB design guidelines for this package are provided in the application note entitled: QFN/SON PCB Attachment Application Note (SLUA271).

The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

Where:

$$\theta_{JA} = \frac{T_J - T_A}{P_D} \tag{4}$$

 T_J = chip junction temperature

 T_A = ambient temperature

P_D = device power dissipation

Factors that can greatly influence the measurement and calculation of θ_{JA} include:

- Whether or not the device is board mounted
- Trace size, composition, thickness, and geometry
- Orientation of the device (horizontal or vertical)
- Volume of the ambient air surrounding the device under test and airflow
- Whether other surfaces are in close proximity to the device being tested

The device power dissipation, P_D , is a function of the charge rate and the voltage drop across the internal PowerFET. It can be calculated from the following equation when a battery pack is being charged:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Due to the charge profile of LiFePO₄ batteries the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. See the charging profile, Figure 13. If the board thermal design is not adequate the programmed fast charge rate current may not be achieved under maximum input voltage and minimum battery voltage, as the thermal loop can be active, effectively reducing the charge current to avoid excessive IC junction temperature.

PCB LAYOUT CONSIDERATIONS

It is important to pay special attention to the PCB layout. The following provides some guidelines:

• To obtain optimal performance, the decoupling capacitor from IN to GND (thermal pad) and the output filter capacitors from OUT to GND (thermal pad) should be placed as close as possible to the bq25070, with short trace runs to both IN, OUT and GND (thermal pad).



www.ti.com SLUSA66 –JULY 2011

All low-current GND connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.

- The high current charge paths into IN pin and from the OUT pin must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces.
- The bq25070 is packaged in a thermally enhanced SON package. The package includes a thermal pad to
 provide an effective thermal contact between the IC and the printed circuit board (PCB); this thermal pad is
 also the main ground connection for the device. Connect the thermal pad to the PCB ground connection. Full
 PCB design guidelines for this package are provided in the application note entitled: QFN/SON PCB
 Attachment Application Note (SLUA271).

www.ti.com 11-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
BQ25070DQCR	Active	Production	WSON (DQC) 10	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QUS
BQ25070DQCR.A	Active	Production	WSON (DQC) 10	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QUS
BQ25070DQCR.B	Active	Production	WSON (DQC) 10	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QUS
BQ25070DQCT	Active	Production	WSON (DQC) 10	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QUS
BQ25070DQCT.A	Active	Production	WSON (DQC) 10	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QUS
BQ25070DQCT.B	Active	Production	WSON (DQC) 10	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QUS

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

www.ti.com 11-Nov-2025

PACKAGE MATERIALS INFORMATION

www.ti.com 30-Apr-2018

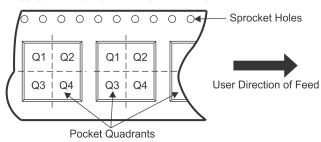
TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

7 til dillionolollo aro nominar												
Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25070DQCR	WSON	DQC	10	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
BQ25070DQCT	WSON	DQC	10	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com 30-Apr-2018



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25070DQCR	WSON	DQC	10	3000	210.0	185.0	35.0
BQ25070DQCT	WSON	DQC	10	250	210.0	185.0	35.0

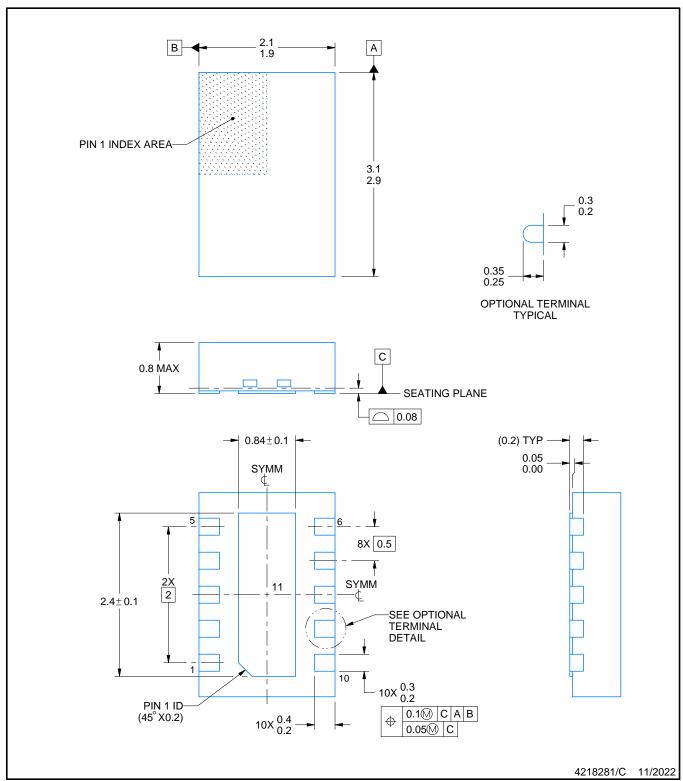


Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4209674/B







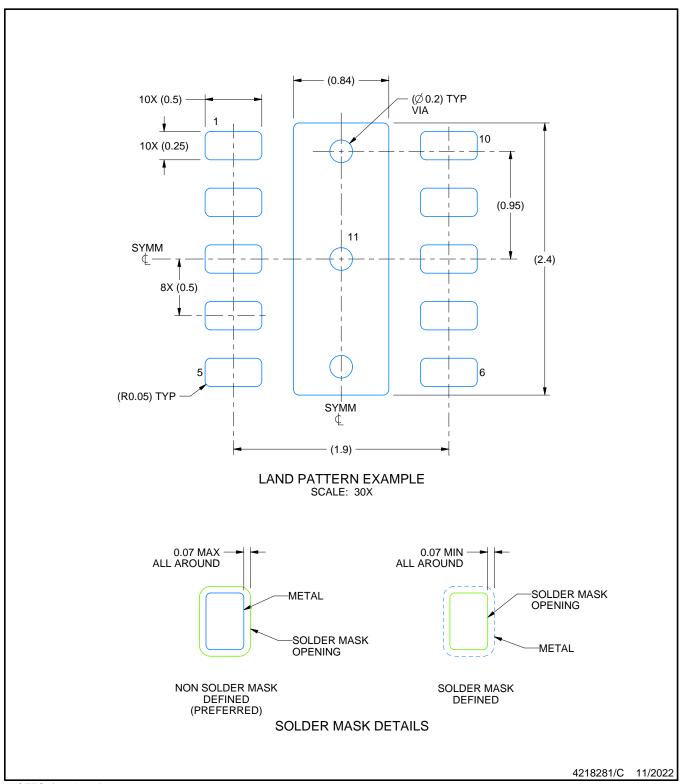
NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

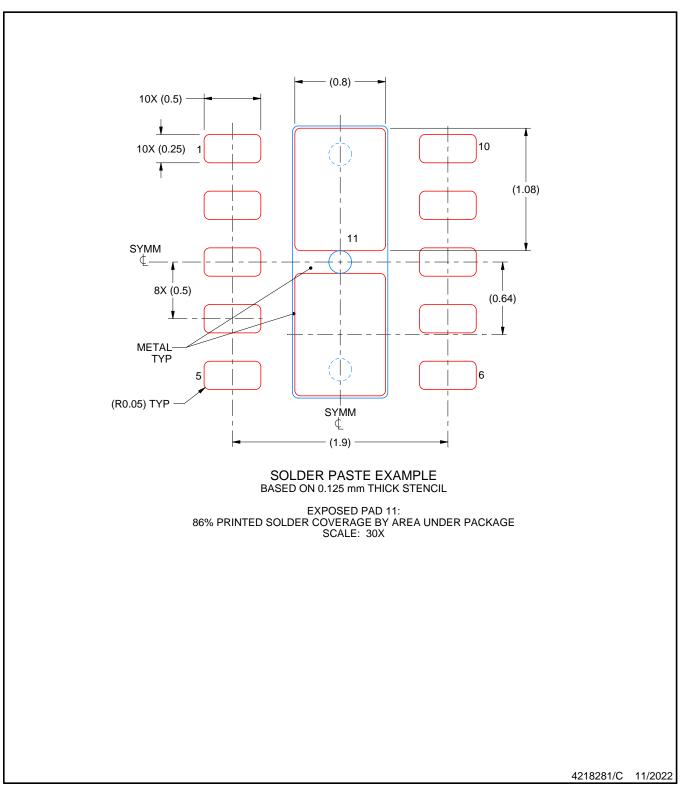




NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.





NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025