









**AMC3330** SBASA34B - JUNE 2020 - REVISED AUGUST 2024

# AMC3330 Precision, ±1V Input, Reinforced Isolated Amplifier With Integrated DC/DC Converter

#### 1 Features

- 3.3V or 5V single supply operation with integrated DC/DC converter
- ±1V input voltage range optimized for voltage measurements with high input impedance
- Fixed gain: 2.0 Low DC errors:
  - Gain error: ±0.2% (max) Gain drift: ±45ppm/°C (max) Offset error: ±0.3mV (max)
  - Offset drift: ±4µV/°C (max) Nonlinearity: ±0.02% (max)
- High CMTI: 85kV/µs (min)
- System-level diagnostic features
- Safety-related certifications:
  - 6000V<sub>PK</sub> reinforced isolation per DIN EN IEC 60747-17 (VDE 0884-17)
  - 4250V<sub>RMS</sub> isolation for 1 minute per UL1577
- Meets CISPR-11 and CISPR-25 EMI standards

## 2 Applications

- Isolated voltage sensing in:
  - Motor drives
  - Photovoltaic inverters
  - Power delivery systems
  - EV charging infrastructure
  - Battery energy storage systems

## 3 Description

The AMC3330 is a precision, isolated amplifier with a fully integrated, isolated DC/DC converter that allows single-supply operation from the low-side of the device. The reinforced capacitive isolation barrier is certified according to DIN EN IEC 60747-17 (VDE 0884-17) and UL1577 and separates sections of the system that operate on different common-mode voltage levels and protects low-voltage domains from damage.

The input of the AMC3330 is optimized for direct connection to high-impedance, voltage-signal sources such as a resistor-divider network to sense high-voltage signals. The integrated isolated DC/DC converter allows measurement of non-groundreferenced signals and makes the device a unique solution for noisy, space-constrained applications.

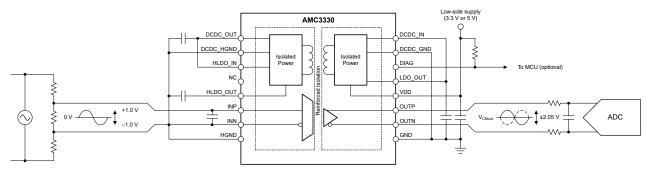
The excellent performance of the device supports accurate voltage monitoring and control. integrated DC/DC converter fault-detection diagnostic output pin of the AMC3330 simplify system-level design and diagnostics.

The AMC3330 is specified over the temperature range of -40°C to +125°C.

**Package Information** 

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>		
AMC3330	DWE (SOIC, 16)	10.3mm × 10.3mm		

- For more information, see the Mechanical, Packaging, and Orderable Information .
- The package size (length × width) is a nominal value and includes pins, where applicable.



**Application Example** 



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# **4 Pin Configuration and Functions**

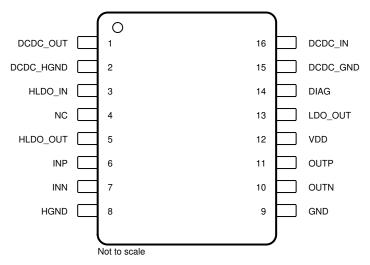


Figure 4-1. DWE Package, 16-Pin SOIC (Top View)

**Table 4-1. Pin Functions** 

	PIN	TYPE	DESCRIPTION
NO.	NAME	IIPE	DESCRIPTION
1	DCDC_OUT	Power	High-side output of the isolated DC/DC converter; connect this pin to the HLDO_IN pin.(1)
2	DCDC_HGND	Power Ground	High-side ground reference for the isolated DC/DC converter; connect this pin to the HGND pin.
3	HLDO_IN	Power	Input of the high-side low-dropout (LDO) regulator; connect this pin to the DCDC_OUT pin. <sup>(1)</sup>
4	NC	_	No internal connection. Connect this pin to the high-side ground or leave this pin unconnected (floating).
5	HLDO_OUT	Power	Output of the high-side LDO. <sup>(1)</sup>
6	INP	Analog Input	Noninverting analog input.
7	INN	Analog Input	Inverting analog input. Connect this pin to HGND.
8	HGND	Signal Ground	High-side analog ground; connect this pin to the DCDC_HGND pin.
9	GND	Signal Ground	Low-side analog ground; connect this pin to the DCDC_GND pin.
10	OUTN	Analog Output	Inverting analog output.
11	OUTP	Analog Output	Noninverting analog output.
12	VDD	Power	Low-side power supply. <sup>(1)</sup>
13	LDO_OUT	Power	Output of the low-side LDO; connect this pin to the DCDC_IN pin. <sup>(1)</sup>
14	DIAG	Digital Output	Active-low, open-drain status indicator output; connect this pin to the pullup supply (for example, VDD) using a resistor or leave this pin floating if not used.
15	DCDC_GND	Power Ground	Low-side ground reference for the isolated DC/DC converter; connect this pin to the GND pin.
16	DCDC_IN	Power	Low-side input of the isolated DC/DC converter; connect this pin to the LDO_OUT pin. <sup>(1)</sup>

<sup>(1)</sup> See the *Power Supply Recommendations* section for power-supply decouplng recommendations.



## **5 Specifications**

## 5.1 Absolute Maximum Ratings

see (1)

		MIN	MAX	UNIT
Power-supply voltage	VDD to GND	-0.3	6.5	V
Analog input voltage	INP, INN	HGND – 6	V <sub>HLDOout</sub> + 0.5	V
Analog output voltage	OUTP, OUTN	GND – 0.5	VDD + 0.5	V
Digital output voltage	DIAG	GND – 0.5	6.5	V
Input current	Continuous, any pin except power-supply pins	-10	10	mA
Temperature	Junction, T <sub>J</sub>		150	°C
remperature	Storage, T <sub>stg</sub>	-65	150	

Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

## 5.2 ESD Ratings

			VALUE	UNIT
V	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
V <sub>(ESD)</sub>	Liectiostatic discillarge	Charged-device model (CDM), per per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±1000	V

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER S	SUPPLY					
VDD	Low-side supply voltage	VDD to GND	3.0	3.3	5.5	V
ANALOG	INPUT					
V <sub>Clipping</sub>	Differential input voltage before clipping output	$V_{IN} = V_{INP} - V_{INN}$		±1.25		V
V <sub>FSR</sub>	Specified linear differential full-scale voltage	$V_{IN} = V_{INP} - V_{INN}$	-1		1	V
	Absolute common-mode input voltage <sup>(1)</sup>	(V <sub>INP</sub> + V <sub>INN</sub> ) / 2 to HGND	-2		3	V
		(V <sub>INP</sub> + V <sub>INN</sub> ) / 2 to HGND, V <sub>INP</sub> = V <sub>INN</sub>	-1.4		1.6	
V <sub>CM</sub>	Operating common-mode input voltage	(V <sub>INP</sub> + V <sub>INN</sub> ) / 2 to HGND,  V <sub>INP</sub> - V <sub>INN</sub>   = 1.0 V <sup>(2)</sup>	-0.925		0.725	V
		(V <sub>INP</sub> + V <sub>INN</sub> ) / 2 to HGND,  V <sub>INP</sub> - V <sub>INN</sub>   = 1.25 V	-0.8		0.6	
ANALOG	ОИТРИТ					
C <sub>LOAD</sub>	Capacitive load	On OUTP or OUTN to GND2, Without any series resistance			500	pF
C <sub>LOAD</sub>	Capacitive load	OUTP to OUTN, Without any series resistance			250	pF
R <sub>LOAD</sub>	Resistive load	On OUTP or OUTN to GND2		10	1	kΩ
DIGITAL (	DUTPUT					
	Pull-up supply-voltage for DIAG pin		0		VDD	V
TEMPERA	ATURE RANGE					
T <sub>A</sub>	Operating ambient temperature		-40	25	125	°C

Steady-state voltage supported by the device in case of a system failure. See specified common-mode input voltage V<sub>CM</sub> for normal operation. Observe analog input voltage range as specified in the Absolute Maximum Ratings table.

Linear response.



## **5.4 Thermal Information**

		AMC3330	
	nction-to-case (top) thermal resistance nction-to-board thermal resistance	DWE (SOIC)	UNIT
		16 PINS	
R <sub>0JA</sub>	Junction-to-ambient thermal resistance	73.5	°C/W
R <sub>0JC(top)</sub>	Junction-to-case (top) thermal resistance	31	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	44	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	16.7	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	42.8	°C/W
R <sub>0JC(bot)</sub>	Junction-to-case (bottom) thermal resistance	n/a	°C/W

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 5.5 Power Ratings

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pn	Maximum power dissipation	VDD = 5.5 V			236.5	mW
FD	Maximum power dissipation	VDD = 3.6 V			155	11100



### **5.6 Insulation Specifications**

over operating ambient temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	VALUE	UNIT
GENER	AL			
CLR	External clearance <sup>(1)</sup>	Shortest pin-to-pin distance through air	≥ 8	mm
CPG	External creepage <sup>(1)</sup>	Shortest pin-to-pin distance across the package surface	≥ 8	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance - capacitive signal isolation)	≥ 21	μm
DTI	Distance through insulation	Minimum internal gap (internal clearance - transformer power isolation)	≥ 120	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	1	
	Overvoltage category	Rated mains voltage ≤ 600V <sub>RMS</sub>	1-111	
	per IEC 60664-1	Rated mains voltage ≤ 1000V <sub>RMS</sub>	1-11	
DIN EN	IEC 60747-17 (VDE 0884-17)			
V <sub>IORM</sub>	Maximum repetitive peak isolation voltage	At AC voltage	1700	V <sub>PK</sub>
V <sub>IOTM</sub>	Maximum-rated isolation	At AC voltage (sine wave)	1200	V <sub>RMS</sub>
VIOWM	working voltage	At DC voltage	1700	$V_{DC}$
$V_{IOTM}$	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$ , t = 60s (qualification test), $V_{TEST} = 1.2 \times V_{IOTM}$ , t = 1s (100% production test)	6000	V <sub>PK</sub>
V <sub>IMP</sub>	Maximum impulse voltage(2)	Tested in air, 1.2/50µs waveform per IEC 62368-1	7700	V <sub>PK</sub>
V <sub>IOSM</sub>	Maximum surge isolation voltage <sup>(3)</sup>	Tested in oil (qualification test), 1.2/50µs waveform per IEC 62368-1	10000	V <sub>PK</sub>
		Method a, after input/output safety test subgroups 2 and 3, $V_{pd(ini)} = V_{IOTM}$ , $t_{ini} = 60$ s, $V_{pd(m)} = 1.2 \times V_{IORM}$ , $t_m = 10$ s	≤ 5	
~	Apparent shares (4)	Method a, after environmental tests subgroup 1, $V_{pd(ini)} = V_{IOTM}$ , $t_{ini} = 60s$ , $V_{pd(m)} = 1.6 \times V_{IORM}$ , $t_m = 10 s$	≤ 5	
q <sub>pd</sub>	Apparent charge <sup>(4)</sup>	Method b1, at preconditioning (type test) and routine test, $V_{pd(ini)} = 1.2 \times V_{IOTM}$ , $t_{ini} = 1$ s, $V_{pd(m)} = 1.875 \times V_{IORM}$ , $t_m = 1$ s	≤ 5	— pC
		Method b2, at routine test (100% production) <sup>(6)</sup> , $V_{pd(ini)} = V_{pd(m)} = 1.2 \times V_{IOTM}$ , $t_{ini} = t_m = 1s$	≤ 5	
C <sub>IO</sub>	Barrier capacitance, input to output <sup>(5)</sup>	V <sub>IO</sub> = 0.5 V <sub>PP</sub> at 1MHz	~4.5	pF
		V <sub>IO</sub> = 500 V at T <sub>A</sub> = 25°C	> 10 <sup>12</sup>	
$R_{IO}$	Insulation resistance, input to output <sup>(5)</sup>	V <sub>IO</sub> = 500 V at 100°C ≤ T <sub>A</sub> ≤ 125°C	> 10 <sup>11</sup>	Ω
	har to earle at	V <sub>IO</sub> = 500 V at T <sub>S</sub> = 150°C	> 10 <sup>9</sup>	
	Pollution degree		2	
	Climatic category		40/125/21	
UL1577	•			
V <sub>ISO</sub>	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ , t = 60s (qualification test), $V_{TEST} = 1.2 \times V_{ISO}$ , t = 1s (100% production test)	4250	V <sub>RMS</sub>

<sup>(1)</sup> Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Maintain the creepage and clearance distance of a board design to make sure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.

- (2) Testing is carried out in air to determine the surge immunity of the package.
- (3) Testing is carried in oil to determine the intrinsic surge immunity of the isolation barrier.
- (4) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (5) All pins on each side of the barrier are tied together, creating a two-pin device.
- 6) Either method b1 or b2 is used in production.



#### 5.7 Safety-Related Certifications

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN IEC 62368-1 (VDE 0868-1), EN IEC 62368-1, IEC 62368-1 Clause: 5.4.3; 5.4.4.4; 5.4.9	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
Certificate number: 40040142	File number: E181974

## 5.8 Safety Limiting Values

Safety limiting (1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Safety input, output, or supply current	R <sub>θJA</sub> = 73.5°C/W, VDD = 5.5 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			309	mA
I <sub>S</sub>		R <sub>θJA</sub> = 73.5°C/W, VDD = 3.6 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			472	IIIA
Ps	Safety input, output, or total power	R <sub>θJA</sub> = 73.5°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			1700	mW
T <sub>S</sub>	Maximum safety temperature				150	°C

The maximum safety temperature, T<sub>S</sub>, has the same value as the maximum junction temperature, T<sub>J</sub>, specified for the device. The I<sub>S</sub> and P<sub>S</sub> parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I<sub>S</sub> and P<sub>S</sub>. These limits vary with the ambient temperature,  $T_A$ . The junction-to-air thermal resistance,  $R_{\theta JA}$ , in the *Thermal Information* table is that of a device installed on a high-K test board for

leaded surface-mount packages. Use these equations to calculate the value for each parameter:

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 $T_J = T_A + R_{\theta JA} \times P$ , where P is the power dissipated in the device.

 $T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$ , where  $T_{J(max)}$  is the maximum junction temperature.

 $P_S = I_S \times VDD_{max}$ , where  $VDD_{max}$  is the maximum low-side voltage.



## **5.9 Electrical Characteristics**

minimum and maximum specifications apply from  $T_A = -40^{\circ}\text{C}$  to +125°C, VDD = 3.0 V to 5.5 V, INP = -1 V to +1 V, and INN = HGND = 0 V; typical specifications are at  $T_A = 25^{\circ}\text{C}$ , and VDD = 3.3 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG	INPUT					
R <sub>IN</sub>	Single-ended input resistance	INN = HGND	0.1	0.8		
R <sub>IND</sub>	Differential input resistance		0.1	1.2		GΩ
I <sub>IB</sub>	Input bias current	INP = INN = HGND, I <sub>IB</sub> = (I <sub>IBP</sub> + I <sub>IBN</sub> ) / 2	-10	2.5	10	nA
TCI <sub>IB</sub>	Input bias current drift			-14		pA/°C
I <sub>IO</sub>	Input offset current	$I_{IO} = I_{INP} - I_{INN}$ ; INP = INN = HGND	-10	-0.8	10	nA
C <sub>IN</sub>	Single-ended input capacitance	INN = HGND, f <sub>IN</sub> = 310 kHz		2		
C <sub>IND</sub>	Differential input capacitance	f <sub>IN</sub> = 310 kHz		2		pF
ANALOG		TIN STOTALE				
ANALOG	Nominal gain			2		V/V
V	Common-mode output voltage		1.39	1.44	1.49	V
V <sub>CMout</sub>	Clipping differential output voltage	$V_{OUT} = (V_{OUTP} - V_{OUTN});$	1.39	±2.49	1.49	V
V <sub>Failsafe</sub>	Failsafe differential output voltage	$ V_{IN}  =  V_{INP} - V_{INN}  > V_{Clipping}$ $V+ = (V_{OUTP} - V_{OUTN}); V_{DCDCout} \le V_{DCDCUV}$ or $V_{HLDOout} \le V_{HLDOUV}$		-2.57	-2.5	V
BW <sub>OUT</sub>	Output bandwidth		300	375		kHz
R <sub>OUT</sub>	Output resistance	On OUTP or OUTN		0.2		Ω
	Output short-circuit current	On OUTP or OUTN, sourcing or sinking, INP = INN = HGND, outputs shorted to either GND or VDD		14		mA
CMTI	Common-mode transient immunity	HGND – GND  = 2 kV	85	135		kV/µs
ACCURAC	CY					
V <sub>OS</sub>	Input offset voltage <sup>(1) (2)</sup>	T <sub>A</sub> = 25°C, INP = INN = HGND	-0.3	±0.05	0.3	mV
TCV <sub>OS</sub>	Input offset drift <sup>(1)</sup> (2) (4)		-4	±1	4	μV/°C
E <sub>G</sub>	Gain error	T <sub>A</sub> = 25°C	-0.2%	-0.08%	0.2%	•
TCE <sub>G</sub>	Gain error drift <sup>(1)</sup> (5)		<b>–45</b>	±7	45	ppm/°C
. u_g	Nonlinearity		-0.02%	0.01%	0.02%	PP, 0
	Nonlinearity drift		0.0270	0.4	0.0270	ppm/°C
	,	V <sub>IN</sub> = 2 V <sub>PP</sub> , f <sub>IN</sub> = 1 kHz, BW = 10 kHz, 10 kHz filter	81	85		
SNR	Signal-to-noise ratio	V <sub>IN</sub> = 2 V <sub>PP</sub> , f <sub>IN</sub> = 10 kHz, BW = 100 kHz, 1 MHz filter		72		dB
THD	Total harmonic distortion <sup>(3)</sup>	V <sub>IN</sub> = 2 Vpp, f <sub>IN</sub> = 10 kHz, BW = 100 kHz		-84		dB
	Output noise	INP = INN = HGND, f <sub>IN</sub> = 0 Hz, BW = 100 kHz		250		$\mu V_{RMS}$
		f <sub>IN</sub> = 0 Hz, V <sub>CM min</sub> ≤ V <sub>CM</sub> ≤ V <sub>CM max</sub>		-100		
CMRR	Common-mode rejection ratio	$f_{IN} = 10 \text{ kHz}, V_{CM \text{ min}} \le V_{CM} \le V_{CM}$ max		-86		dB
		VDD from 3.0 V to 5.5 V, at dc, input referred		-98		
PSRR	Power-supply rejection ratio	INP = INN = HGND, VDD from 3.0 V to 5.5 V, 10 kHz / 100 mV ripple, input referred		-86		dB
DIGITAL C	DUTPUT ( DIAG)				'	
V <sub>OL</sub>	Low-level output voltage	I <sub>SINK</sub> = 4 mA		80	250	mV

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## 5.9 Electrical Characteristics (continued)

minimum and maximum specifications apply from  $T_A = -40^{\circ}\text{C}$  to +125°C, VDD = 3.0 V to 5.5 V, INP = -1 V to +1 V, and INN = HGND = 0 V; typical specifications are at  $T_A = 25^{\circ}\text{C}$ , and VDD = 3.3 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>LKG</sub>	Open-drain output leakage current	VDD = 5V		5	100	nA
POWER SU	IPPLY				'	
IDD	Low-side supply current	No external load on HLDO		28.5	41	mA
טטו	Low-side supply current	1 mA external load on HLDO		30.5	43	mA
VDD	VDD analog undervoltage detection	VDD rising			2.9	V
VDD <sub>UV</sub>	threshold	VDD falling			2.8	V
VDD	VDD digital reset threshold	VDD rising			2.5	V
VDD <sub>POR</sub>	digital reset tilleshold	VDD falling			2.4	V
V <sub>DCDC_OUT</sub>	DC/DC output voltage	DCDC_OUT to HGND	3.1	3.5	4.65	V
V <sub>DCDCUV</sub>	DC/DC output undervoltage detection threshold voltage	DCDC output falling	2.1	2.25		V
V <sub>HLDO_OUT</sub>	High-side LDO output voltage	HLDO to HGND, up to 1 mA external load	3	3.2	3.4	V
V <sub>HLDOUV</sub>	High-side LDO output undervoltage detection threshold voltage	HLDO output falling	2.4	2.6		V
1	High-side supply current for auxiliary	3 V ≤ VDD < 4.5 V, load connected from HLDO_OUT to HGND, non-switching			1	Λ
IH circuitry		4.5 V ≤ VDD ≤ 5.5 V, load connected from HLDO_OUT to HGND, non-switching			4.3	mA
t <sub>AS</sub>	Analog settling time	VDD step to 3.0 V, to OUTP and OUTN valid, 0.1% settling		0.6	1.1	ms

- (1) The typical value includes one standard deviation ("sigma") at nominal operating conditons.
- (2) This parameter is input referred.
- (3) THD is the ratio of the rms sum of the amplitues of first five higher harmonics to the amplitude of the fundamental.
- (4) Offset error temperature drift is calculated using the box method, as described by the following equation:  $TCV_{OS} = (V_{OS,MAX} V_{OS,MIN}) / TempRange$  where  $V_{OS,MAX}$  and  $V_{OS,MIN}$  refer to the maximum and minimum  $V_{OS}$  values measured within the temperature range (–40 to 125°C).
- (5) Gain error temperature drift is calculated using the box method, as described by the following equation:  $TCE_G(ppm) = ((E_{G,MAX} E_{G,MIN}) / TempRange) \times 10^4$  where  $E_{G,MAX}$  and  $E_{G,MIN}$  refer to the maximum and minimum  $E_G$  values (in %) measured within the temperature range (–40 to 125°C).

## 5.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>r</sub>	Output signal rise time			1.3		μs
t <sub>f</sub>	Output signal fall time			1.3		μs
	V <sub>INx</sub> to V <sub>OUTx</sub> signal delay (50% – 10%)	Unfiltered output		1.2	1.3	μs
	V <sub>INx</sub> to V <sub>OUTx</sub> signal delay (50% – 50%)	Unfiltered output		1.6	2.1	μs
	V <sub>INx</sub> to V <sub>OUTx</sub> signal delay (50% – 90%)	Unfiltered output		2.2	2.6	μs



# **5.11 Timing Diagram**

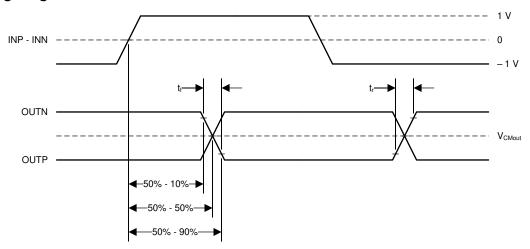
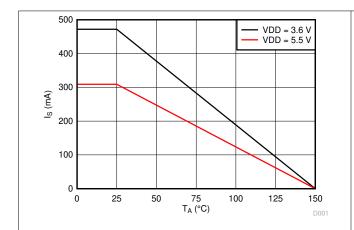


Figure 5-1. Rise, Fall, and Delay Time Waveforms



## **5.12 Insulation Characteristics Curves**



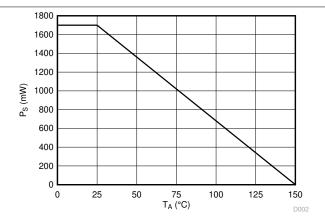


Figure 5-2. Thermal Derating Curve for Safety-Limiting Current per VDE

Figure 5-3. Thermal Derating Curve for Safety-Limiting Power per VDE

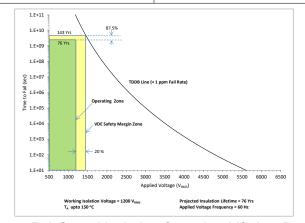
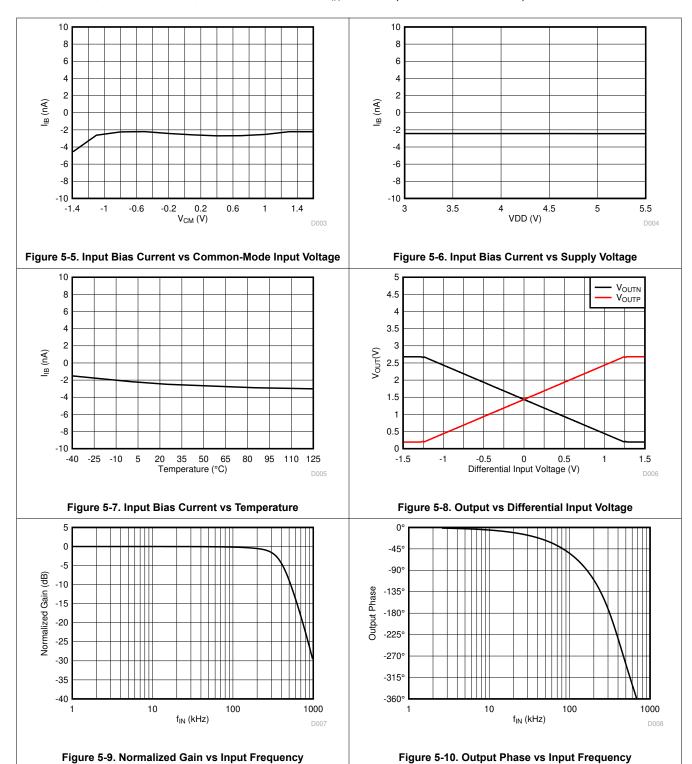


Figure 5-4. Reinforced Isolation Capacitor Lifetime Projection



## **5.13 Typical Characteristics**

at VDD = 3.3 V, INP = -1 V to 1 V, INN = HGND = 0V, and  $f_{IN}$  = 10 kHz (unless otherwise noted)

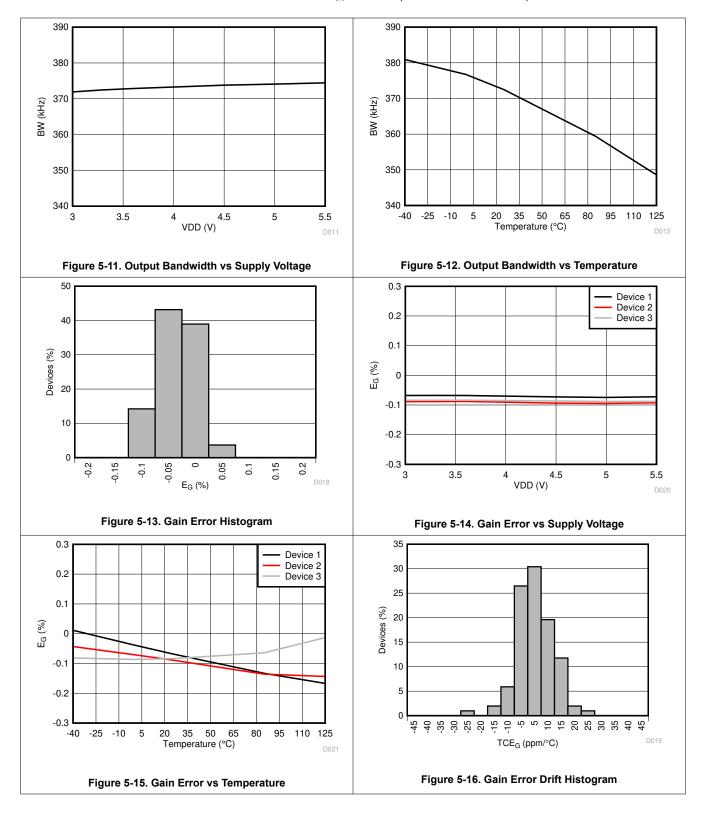


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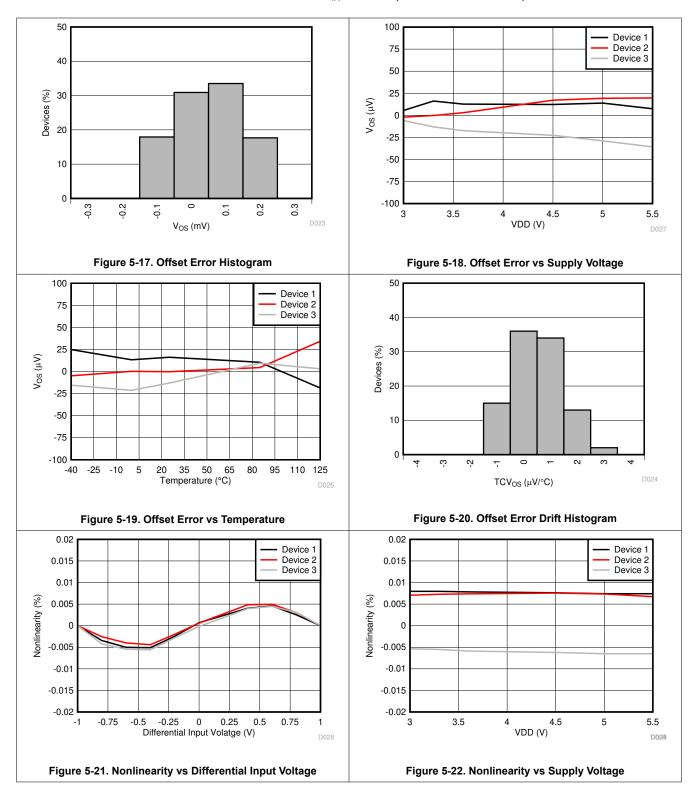


at VDD = 3.3 V, INP = -1 V to 1 V, INN = HGND = 0V, and  $f_{IN}$  = 10 kHz (unless otherwise noted)





at VDD = 3.3 V, INP = -1 V to 1 V, INN = HGND = 0V, and  $f_{IN}$  = 10 kHz (unless otherwise noted)

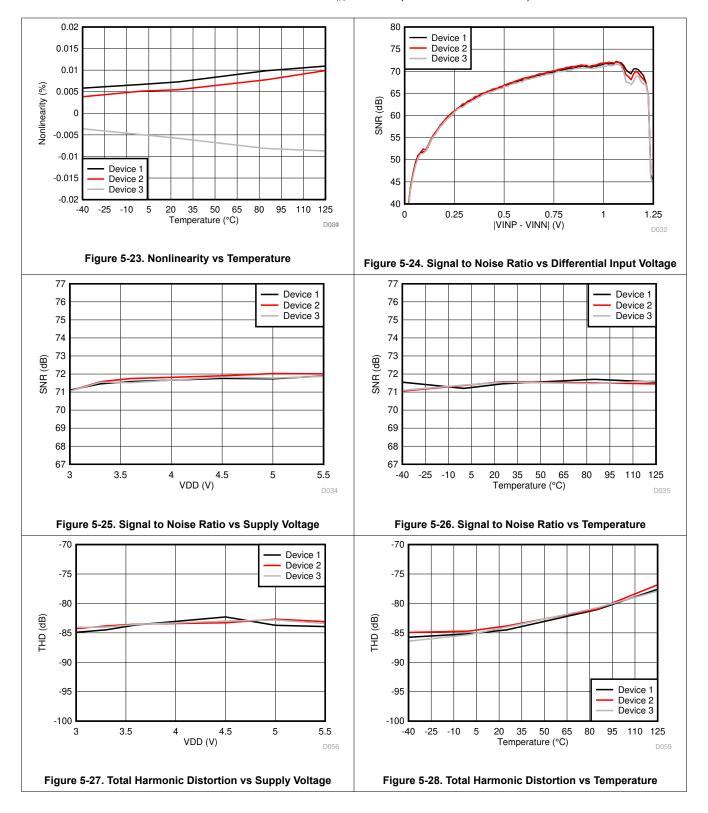


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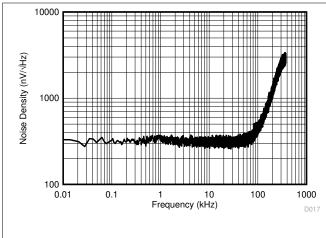


at VDD = 3.3 V, INP = -1 V to 1 V, INN = HGND = 0V, and  $f_{IN}$  = 10 kHz (unless otherwise noted)





at VDD = 3.3 V, INP = -1 V to 1 V, INN = HGND = 0V, and  $f_{IN}$  = 10 kHz (unless otherwise noted)



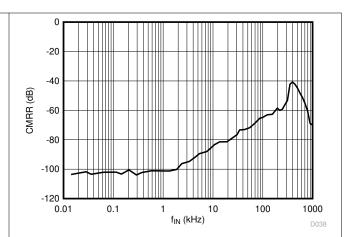
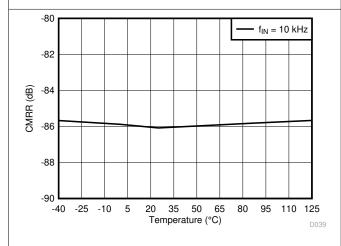


Figure 5-29. Input-Referred Noise Density vs Frequency

Figure 5-30. Common-Mode Rejection Ratio vs Input Frequency



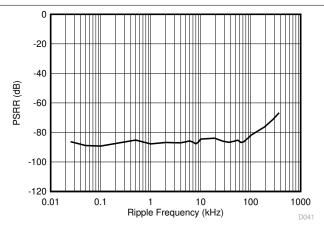
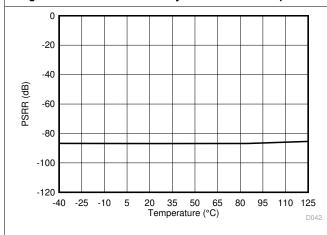


Figure 5-31. Common-Mode Rejection Ratio vs Temperature

Figure 5-32. Power-Supply Rejection Ratio vs Ripple Frequency



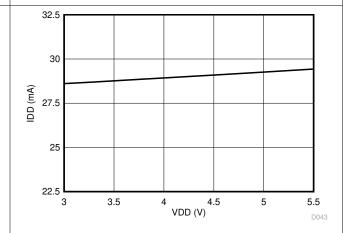


Figure 5-33. Power-Supply Rejection Ratio vs Temperature

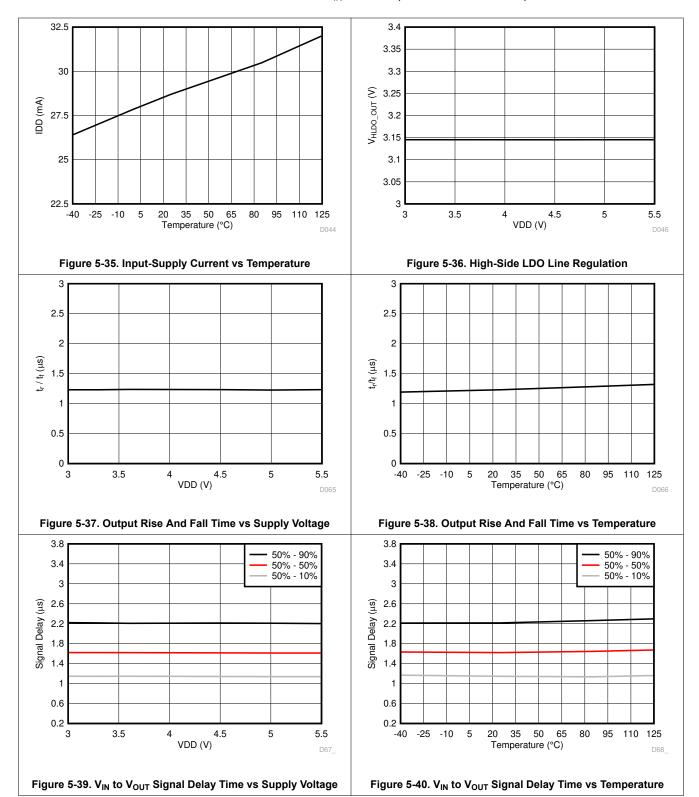
Figure 5-34. Input-Supply Current vs Supply Voltage

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at VDD = 3.3 V, INP = -1 V to 1 V, INN = HGND = 0V, and  $f_{IN}$  = 10 kHz (unless otherwise noted)





## **6 Detailed Description**

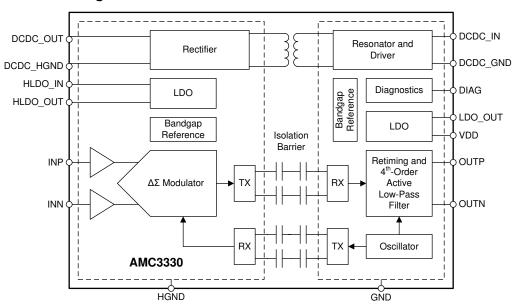
#### 6.1 Overview

The AMC3330 is a fully-differential, precision, isolated amplifier with high input impedance, and an integrated DC/DC converter that allows the device to be supplied from a single 3.3-V or 5-V voltage supply source on the low side. The input stage of the device drives a second-order, delta-sigma ( $\Delta\Sigma$ ) modulator. The modulator uses an internal voltage reference and clock generator to convert the analog input signal to a digital bitstream. The drivers (termed TX in the *Functional Block Diagram*) transfer the output of the modulator across the isolation barrier that separates the high-side and low-side voltage domains. The received bitstream and clock are synchronized and processed by a fourth-order analog filter on the low-side and presented as a differential analog output.

The *Functional Block Diagram* shows a block diagram of the AMC3330. The 1.2-G $\Omega$  differential input impedance of the analog input stage supports low gain-error signal-sensing in high-voltage applications using high-impedance resistor dividers.

The signal path is isolated by a double capacitive silicon-dioxide (SiO<sub>2</sub>) insulation barrier, whereas power isolation uses an on-chip transformer separated by a thin-film polymer as the insulating material.

## 6.2 Functional Block Diagram



#### 6.3 Feature Description

#### 6.3.1 Analog Input

The input stage of the AMC3330 feeds a second-order, switched-capacitor, feed-forward  $\Delta\Sigma$  modulator. The modulator converts the analog signal into a bitstream that is transferred over the isolation barrier, as described in the *Isolation Channel Signal Transmission* section. The high-impedance, and low bias-current input of the AMC3330 makes the device suitable for isolated, high-voltage-sensing applications that typically employ high-impedance resistor dividers.

There are two restrictions on the analog input signals (INP and INN). First, if the input voltage exceeds the input range specified in the *Absolute Maximum Ratings* table, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on. Second, the linearity and noise performance of the device are ensured only when the differential analog input voltage remains within the specified linear full-scale range V<sub>FSR</sub> and within the specified input common-mode voltage range V<sub>CM</sub> as specified in the *Recommended Operating Conditions* table.



## 6.3.2 Isolation Channel Signal Transmission

The AMC3330 uses an on-off keying (OOK) modulation scheme to transmit the modulator output-bitstream across the capacitive SiO<sub>2</sub>-based isolation barrier. Figure 6-1 shows the block diagram of an isolation channel. The transmitter modulates the bitstream at TX IN with an internally generated, 480-MHz carrier and sends a burst across the isolation barrier to represent a digital *one* and sends a *no signal* to represent the digital *zero*. The receiver demodulates the signal after advanced signal conditioning and produces the output. The symmetrical design of each isolation channel improves the common-mode transient immunity (CMTI) performance and reduces the radiated emissions caused by the high-frequency carrier.

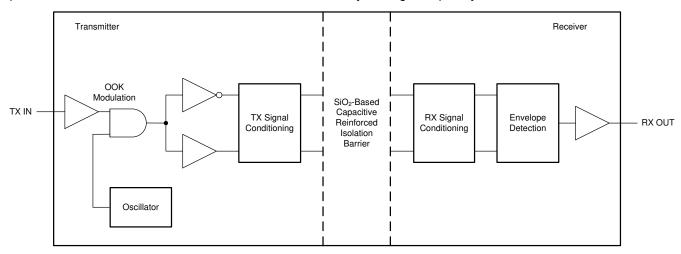


Figure 6-1. Block Diagram of an Isolation Channel

Figure 6-2 shows the concept of the on-off keying scheme.

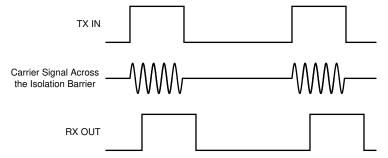


Figure 6-2. OOK-Based Modulation Scheme



#### 6.3.3 Analog Output

The AMC3330 offers a differential analog output comprised of the OUTP and OUTN pins. For differential input voltages ( $V_{\text{INP}} - V_{\text{INN}}$ ) in the range from -1 V to 1 V, the device provides a linear response with a nominal gain of 2. For example, for a differential input voltage of 1 V, the differential output voltage ( $V_{\text{OUTP}} - V_{\text{OUTN}}$ ) is 2 V. At zero input (INP shorted to INN), both pins output the same voltage,  $V_{\text{CMout}}$ , as specified in the *Electrical Characteristics* table. For absolute differential input voltages greater than 1.0 V but less than 1.25 V, the differential output voltage continues to increase in magnitude but with reduced linearity performance. The outputs saturate as shown in Figure 6-3 if the differential input voltage exceeds the  $V_{\text{Clipping}}$  value.

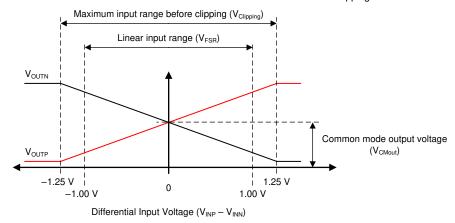


Figure 6-3. AMC3330 Output Behavior

The AMC3330 provides a fail-safe output that simplifies diagnostics on system level. The fail-safe output is active when the integrated DC/DC converter or hgh-side LDO don't deliver the required supply voltage for the high-side of the device. Figure 6-4 and Figure 6-5 illustrate the fail-safe output of the AMC3330 that is a negative differential output voltage value that does not occur under normal operating conditions. Use the maximum  $V_{\text{FAILSAFE}}$  voltage specified in the *Electrical Characteristics* table as a reference value for the fail-safe detection on system level.

Product Folder Links: AMC3330

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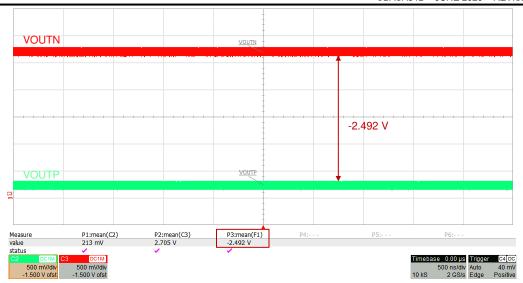


Figure 6-4. Typical Negative Clipping Output of the AMC3330

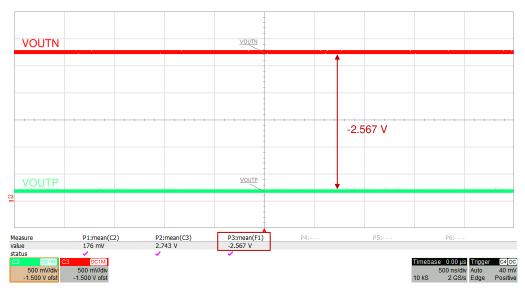


Figure 6-5. Typical Fail-Safe Output of the AMC3330



#### 6.3.4 Isolated DC/DC Converter

The AMC3330 offers a fully integrated isolated DC/DC converter that includes the following components illustrated in the *Functional Block Diagram*:

- Low-dropout regulator (LDO) on the low-side to stabilize the supply voltage VDD that drives the low-side of the DC/DC converter
- · Low-side full-bridge inverter and drivers
- · Laminate-based, air-core transformer for high immunity to magnetic fields
- High-side full-bridge rectifier
- High-side LDO to stabilize the output voltage of the DC/DC converter for high analog performance of the signal path

The DC/DC converter uses a spread-spectrum clock generation technique to reduce the spectral density of the electromagnetic radiation. The resonator frequency is synchronous to the operation of the  $\Delta\Sigma$  modulator to minimize interference with data transmission and support the high analog performance of the device.

The architecture of the DC/DC converter is optimized to drive the high-side circuitry of the AMC3330 and can source up to 1 mA of additional current ( $I_H$ ) for an optional auxiliary circuit such as an active filter, pre-amplifier, or comparator.

#### 6.3.5 Diagnostic Output and Fail-Safe Behavior

The open-drain DIAG pin can be monitored to confirm the device is operational, and the output voltage is valid. During power-up, the DIAG pin is actively held low until the high-side supply is in regulation and the device operates properly. The DIAG pin is actively pulled low if:

- The low-side does not receive data from the high-side (for example, because of a loss of power on the high-side). The amplifier outputs are driven to negative full-scale.
- The high-side DC/DC output voltage (DCDC\_OUT) or the high-side LDO output voltage (HLDO\_OUT) drop
  below their respective undervoltage detection thresholds V<sub>DCDCUV</sub> and V<sub>HLDOUV</sub> as sepecified in the *Electrical*Characteristics table. In this case, the low-side may still receive data from the high-side but the data may not
  be valid. The amplifier outputs are driven to negative full-scale.

During normal operation, the DIAG pin is in a high-impedance state. Connect the DIAG pin to a pull-up supply through a resistor or leave open if not used.

### **6.4 Device Functional Modes**

The AMC3330 is operational when the power supply VDD is applied, as specified in the *Recommended Operating Conditions* table.



## 7 Application and Implementation

#### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 7.1 Application Information

The low input bias current, AC and DC errors, and temperature drift make the AMC3330 a high-performance solution for applications where voltage measurement with high common-mode levels is required.

## 7.2 Typical Application

Isolated amplifiers are widely used for voltage measurements in high-voltage applications that must be isolated from a low-voltage domain. Typical applications are AC line voltage measurements at the input of a power factor correction (PFC) stage or the output of a solar inverter. Other applications are DC measurements at the output of a PFC stage or DC/DC converter, or phase voltage measurements in motor and servo drives. The AMC3330 integrates an isolated power supply for the high-voltage side and therefore is particularly easy to use in applications that do not have a high-side supply readily available or where a high-side supply is referenced to a different ground potential than the signal to be measured.

Figure 7-1 depicts a simplified schematic of the AMC3330 in a solar inverter where the AC phase voltage on the grid-side must be measured. At that location in the system, there is no supply readily available for powering the isolated amplifier. The integrated isolated power supply, together with its bipolar input voltage range, makes the AMC3330 ideally suited for AC line-voltage sensing. In this example, phase current is sensed by the AMC3301 across a shunt resistor on the grid-side of an LCL filter where there is also no suitable supply available for powering the isolated amplifier. The integrated power supply of the AMC3301 eliminates that problem and enables current sensing at optimal locations for the system.

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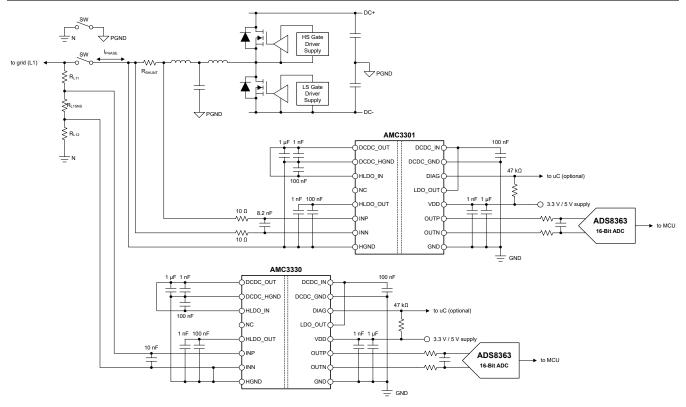


Figure 7-1. The AMC3330 in a Solar Inverter Application

#### 7.2.1 Design Requirements

Table 7-1 lists the parameters for this typical application.

Table 7-1. Design Requirements

<u></u>	•
PARAMETER	VALUE
Low-side supply voltage	3.3 V or 5 V
Voltage drop across the sensing resistor for a linear response	1 V (maximum)
Current through the resistive divider, I <sub>CROSS</sub>	100 μA (maximum)

#### 7.2.2 Detailed Design Procedure

Use Ohm's Law to calculate the minimum total resistance of the resistive divider to limit the cross current to the desired value (  $R_{TOTAL}$  =  $V_{Lx}$  /  $I_{CROSS}$  ) and the required sense resistor value to be connected to the AMC3330 input:  $R_{SNS}$  =  $V_{FSR}$  /  $I_{CROSS}$ .

Consider the following two restrictions to choose the proper value of the sense resistor R<sub>SNS</sub>:

- The voltage drop on  $R_{SNS}$  caused by the nominal voltage range of the system must not exceed the recommended input voltage range:  $V_{SNS} \le V_{FSR}$
- The voltage drop on R<sub>SNS</sub> caused by the maximum allowed system overvoltage must not exceed the input voltage that causes a clipping output: V<sub>SNS</sub> ≤ V<sub>Clipping</sub>



Table 7-2 lists examples of nominal E96-series (1% accuracy) resistor values for systems using 120-V and 230-V AC line voltages.

Table 7-2. Resistor Value Examples	<b>Table</b>	7-2.	Resistor	Value	Examples
------------------------------------	--------------	------	----------	-------	----------

PARAMETER	120-V <sub>RMS</sub> LINE VOLTAGE	230-V <sub>RMS</sub> LINE VOLTAGE
Peak voltage	170 V	325 V
Resistive divider resistors R <sub>L11</sub> , R <sub>L12</sub>	845 kΩ	1.62 ΜΩ
Sense resistor R <sub>SNS</sub>	10 kΩ	10 kΩ
Current through resistive divider I <sub>CROSS</sub>	100 μΑ	100 μΑ
Resulting voltage drop on sense resistor V <sub>SNS</sub>	1.00 V	1.00 V

#### 7.2.2.1 Input Filter Design

TI recommends placing an RC filter in front of the isolated amplifier to improve signal-to-noise performance of the signal path. Design the input filter such that:

- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency (20 MHz) of the internal ΔΣ modulator
- · The input bias current does not generate significant voltage drop across the DC impedance of the input filter
- The impedances measured from the analog inputs are equal

Most voltage sensing applications use high-impedance resistor dividers in front of the isolated amplifier to scale down the input voltage. In this case, a single capacitor as given in Figure 7-2 is sufficient to filter the input signal.

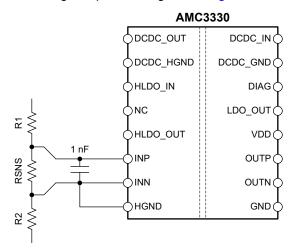


Figure 7-2. Differential Input Filter



#### 7.2.2.2 Differential to Single-Ended Output Conversion

For systems using single-ended input ADCs to convert the analog output voltage into digital, Figure 7-3 shows an example of a TLV6001 -based signal conversion and filter circuit. With R1 = R2 = R3 = R4, the output voltage equals  $(V_{OUTP} - V_{OUTN}) + V_{REF}$ . Tailor the bandwidth of this filter stage to the bandwidth requirement of the system and use NP0-type capacitors for best performance. For most applications, R1 = R2 = R3 = R4 = 10 k $\Omega$  and C1 = C2 = 1000 pF yields good performance.

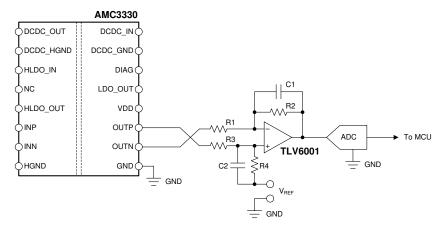


Figure 7-3. Connecting the AMC3330 Output to a Single-Ended Input ADC

For more information on the general procedure to design the filtering and driving stages of SAR ADCs, see the 18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise and 18-Bit Data Acquisition Block (DAQ) Optimized for Lowest Power reference guides, available for download at www.ti.com.

#### 7.2.3 Application Curve

Figure 7-4 shows the typical full-scale step response of the AMC3330.

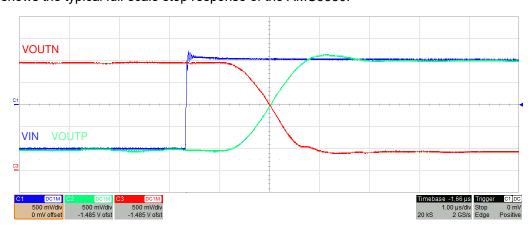


Figure 7-4. Step Respose of the AMC3330

### 7.3 Best Design Practices

Do not leave the analog inputs INP and INN of the AMC3330 unconnected (floating) when the device is powered up on the high-side. If the device input is left floating, the bias current may generate a negative input voltage that exceeds the specified input voltage range and the output of the device is invalid.

Connect the high-side ground (HGND) to INN, either directly or through a resistive path. A DC current path between INN and HGND is required to define the input common-mode voltage. Take care not to exceed the input common-mode range as specified in the *Recommended Operating Conditions* table.

The high-side LDO sources a limited amount of current (I<sub>H</sub>) to power external circuitry. Do not overload the high-side LDO.

The low-side LDO does not output a constant voltage and is not intended for powering any external circuitry. Do not connect any external load to the LDO\_OUT pin.

## 7.4 Power Supply Recommendations

The AMC3330 is powered from the low-side power supply (VDD) with a nominal value of 3.3 V (or 5 V). TI recommends a low-ESR decoupling capacitor of 1 nF (C8 in Figure 7-5) placed as close as possible to the VDD pin, followed by a 1-µF capacitor (C9) to filter this power-supply path.

The low-side of the DC/DC converter is decoupled with a low-ESR 100-nF capacitor (C4) positioned close to the device between the DCDC\_IN and DCDC\_GND pins. Use a 1-µF capacitor (C2) to decouple the high-side in addition to a low-ESR, 1-nF capacitor (C3) placed as close as possible to the device and connected to the DCDC\_OUT and DCDC\_HGND pins.

For the high-side LDO, use low-ESR capacitors of 1-nF (C6), placed as close as possible to the AMC3330, followed by a 100-nF decoupling capacitor (C5).

The ground reference for the high-side (HGND) is derived from the terminal of the sense resistor which is connected to the negative input (INN) of the device. For best DC accuracy, use a separate trace to make this connection but shorting HGND to INN directly at the device input is also acceptable. The high-side DC/DC ground terminal(DCDC HGND) is shorted to HGND directly at the device pins.

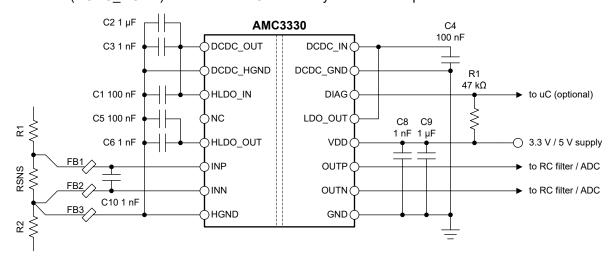


Figure 7-5. Decoupling the AMC3330

Capacitors must provide adequate *effective* capacitance under the applicable DC bias conditions they experience in the application. Multilayer ceramic capacitors (MLCC) capacitors typically exhibit only a fraction of their nominal capacitance under real-world conditions and this factor must be taken into consideration when selecting these capacitors. This problem is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

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The Best Practices to Attenuate AMC3301 Family Radiated Emissions EMI application note is available for download at www.ti.com.

Table 7-3 lists components suitable for use with the AMC3330. This list is not exhaustive. Other components may exist that are equally suitable (or better), however these listed components have been validated during the development of the AMC3330.

**Table 7-3. Recommended External Components** 

	DESCRIPTION	PART NUMBER	MANUFACTURER	SIZE (EIA, L x W)
VDD	22001111 11011			(== (== , = × · · )
C8	1 nF ± 10%, X7R, 50 V	12065C102KAT2A	AVX	1206, 3.2 mm x 1.6 mm
C9	1 μF ± 10%, X7R, 25 V	12063C105KAT2A	AVX	1206, 3.2 mm x 1.6 mm
DC/DC	CONVERTER		·	
C4	100 nF ± 10%, X7R, 50 V	C0603C104K5RACAUTO	Kemet	0603, 1.6 mm x 0.8 mm
C3	1 nF ± 10%, X7R, 50 V	C0603C102K5RACTU	Kemet	0603, 1.6 mm x 0.8 mm
C2	1 μF ± 10%, X7R, 25 V	CGA3E1X7R1E105K080AC	TDK	0603, 1.6 mm x 0.8 mm
HLDO				
C1	100 nF ± 10%, X7R, 50 V	C0603C104K5RACAUTO	Kemet	0603, 1.6 mm x 0.8 mm
C5	100 nF ± 5%, NP0, 50 V	C3216NP01H104J160AA	TDK	1206, 3.2 mm x 1.6 mm
C6	1 nF ± 10%, X7R, 50 V	12065C102KAT2A	AVX	1206, 3.2 mm x 1.6 mm
FERRIT	ΓE BEADS			
FB1,	Ferrite bead <sup>(1)</sup>	74269244182	Wurth Elektronik	0402, 1.0mm × 0.5mm
FB2,		BLM15HD182SH1	Murata	0402, 1.0mm × 0.5mm
FB3		BKH1005LM182-T	Taiyo Yuden	0402, 1.0mm × 0.5mm

<sup>(1)</sup> No ferrite beads are used for parametric validation.



## 7.5 Layout

#### 7.5.1 Layout Guidelines

Figure 7-6 shows a layout recommendation with the critical placement of the decoupling capacitors. The same component reference designators are used as in the *Power Supply Recommendations* section. Decoupling capacitors are placed as close as possible to the AMC3330 supply pins. For best performance, place the sense resistor close to the INP and INN inputs of the AMC3330 and keep the layout of both connections symmetrical.

This layout is used on the AMC3330 EVM and supports CISPR-11 compliant electromagnetic radiation levels.

#### 7.5.2 Layout Example

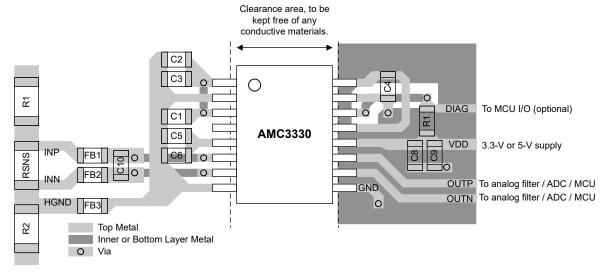


Figure 7-6. Recommended Layout of the AMC3330



## 8 Device and Documentation Support

## 8.1 Device Support

#### 8.1.1 Device Nomenclature

Texas Instruments, Isolation Glossary

#### 8.2 Documentation Support

#### 8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, ISO72x Digital Isolator Magnetic-Field Immunity application note
- Texas Instruments, AMC3301 Precision, ±250-mV Input, Reinforced Isolated Amplifier With Integrated DC/DC Converter data sheet
- Texas Instruments, TLV600x Low-Power, Rail-to-Rail In/Out, 1-MHz Operational Amplifier for Cost-Sensitive Systems data sheet
- Texas Instruments, 18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise reference guide
- Texas Instruments, 18-Bit Data Acquisition Block (DAQ) Optimized for Lowest Power reference guide

#### 8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### **8.4 Support Resources**

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the guick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### 8.5 Trademarks

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#### 8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 8.7 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.



## **9 Revision History**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (Octob	per 2020) to Revision B (August 2024)	Page
	fety-related certification from VDE V 0884-11 to DIN EN IEC 607	
	V charging infrastructure and Protection relays to Battery energy	
Systems in last two Applications	s bullets igure	
	atings: changed max for DIAG pin from 5.5 V to 6.5 V	
	and resistive drive capability specification	
	ecification from 3.5 pF to 4.5 pF	
	n DIN VDE V 0884-11 (VDE V 0884-11) to DIN EN IEC 60747-17	
0884-17) and updated the Insul	ation Specifications and Safety-Related Certifications tables acco	ordingly7
THD footnote added		8
	G) electrical specifications	
	ecifications	
	≤ VDD ≤ 5.5 V	
	sistor Value Examples table	
•	r figure	
,	DO external load discussion to Best Design Practices section	
	mendations section: Changed Decoupling the AMC3330 figure, a	
	1 Family Radiated Emissions EMI reference and added ferrite be	
	onents table	
	DD routing in Recommended Layout of the AMC3330 figure	
	Touting in Recommended Layout of the Alvicssso lighte	
Changes from Revision * (June 2	2020) to Revision A (October 2020)	Page
· Changed document status from	advance information to production data	1

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
AMC3330DWE	Active	Production	SOIC (DWE)   16	40   TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC3330
AMC3330DWE.A	Active	Production	SOIC (DWE)   16	40   TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC3330
AMC3330DWE.B	Active	Production	SOIC (DWE)   16	40   TUBE	-	Call TI	Call TI	-40 to 125	
AMC3330DWER	Active	Production	SOIC (DWE)   16	2000   LARGE T&R	Yes	Call TI   Nipdau	Level-3-260C-168 HR	-40 to 125	AMC3330
AMC3330DWER.A	Active	Production	SOIC (DWE)   16	2000   LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 125	AMC3330
AMC3330DWER.B	Active	Production	SOIC (DWE)   16	2000   LARGE T&R	-	Call TI	Call TI	-40 to 125	
AMC3330DWERG4	Active	Production	SOIC (DWE)   16	2000   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC3330
AMC3330DWERG4.A	Active	Production	SOIC (DWE)   16	2000   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC3330
AMC3330DWERG4.B	Active	Production	SOIC (DWE)   16	2000   LARGE T&R	-	Call TI	Call TI	-40 to 125	

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

## PACKAGE OPTION ADDENDUM

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and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF AMC3330:

Automotive : AMC3330-Q1

NOTE: Qualified Version Definitions:

• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

# **PACKAGE MATERIALS INFORMATION**

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## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Devic			Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC3330E	WER SO	IC	DWE	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
AMC3330DV	VERG4 SO	IC	DWE	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

**PACKAGE MATERIALS INFORMATION** 

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### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC3330DWER	SOIC	DWE	16	2000	350.0	350.0	43.0
AMC3330DWERG4	SOIC	DWE	16	2000	350.0	350.0	43.0

# **PACKAGE MATERIALS INFORMATION**

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## **TUBE**

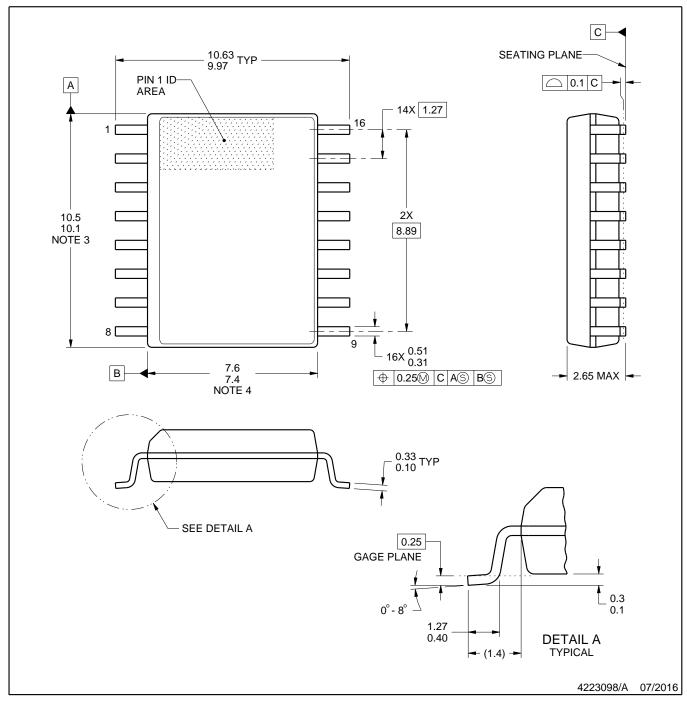


#### \*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
AMC3330DWE	DWE	SO-MOD	16	40	506.98	12.7	4826	6.6
AMC3330DWE.A	DWE	SO-MOD	16	40	506.98	12.7	4826	6.6



SOIC



#### NOTES:

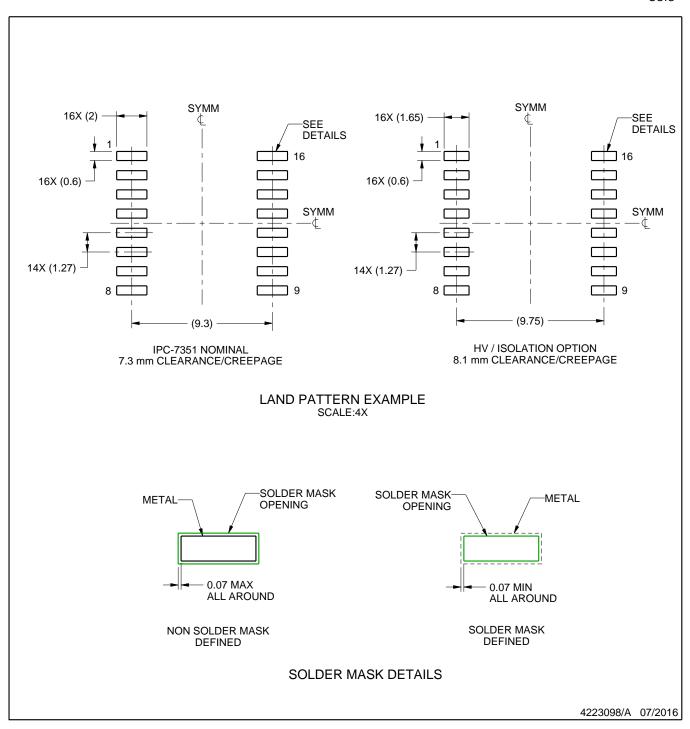
- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
- per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
- 5. Reference JEDEC registration MS-013.



SOIC



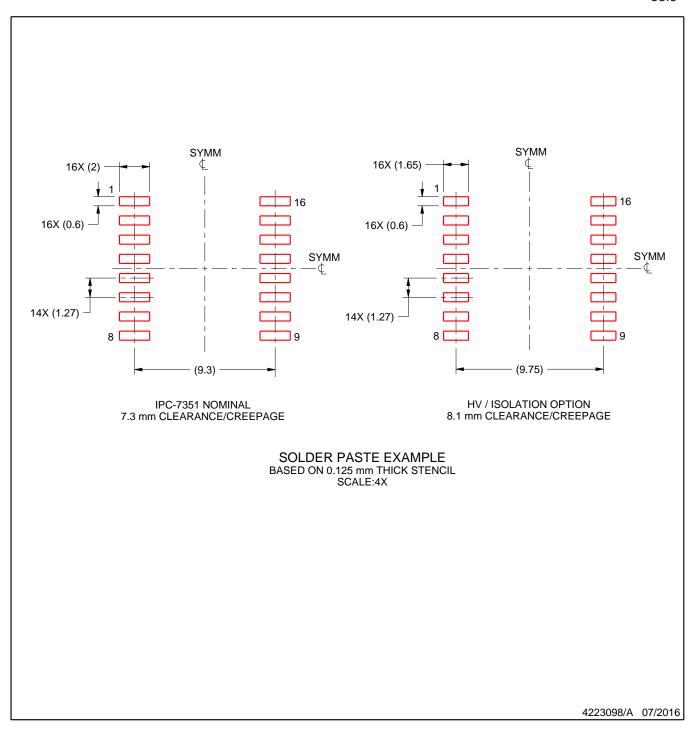
#### NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



#### NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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