AMC1200C Precision, ±250mV Input, Basic Isolated Amplifier With Differential Output

1 Features

- Linear input voltage range: ±250mV
- Supply voltage range:
  - High-side (VDD1): 3.0V to 5.5V
  - Low-side (VDD2): 3.0V to 5.5V
- Fixed gain: 8.0V/V
- Differential analog output
- Low DC errors:
  - Offset error: ±0.2mV (maximum)
  - Offset drift: ±2µV/°C (maximum)
  - Gain error: ±0.25% (maximum)
  - Gain drift: ±35ppm/°C (maximum)
  - Nonlinearity: 0.04% (maximum)
- High CMTI: 150V/ns (minimum)
- Low EMI: Meets CISPR-11 and CISPR-25 standards
- Isolation ratings: Basic isolation
- Safety-related certifications:
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577
- Fully specified over the extended industrial temperature range: –40°C to +125°C

2 Applications

- Industrial motor drives
- Frequency inverters
- Server power-supply units (PSU)
- Power factor correction (PFC)

3 Description

The AMC1200C is a precision, galvanically isolated amplifier with a ±250mV, differential input and differential output. The input is optimized for direct connection to a shunt resistor or other low-impedance signal source.

The isolation barrier separates parts of the system that operate on different common-mode voltage levels. The isolation barrier is highly resistant to magnetic interference. This barrier is certified to provide basic isolation up to 5kV$_{RMS}$ (60s).

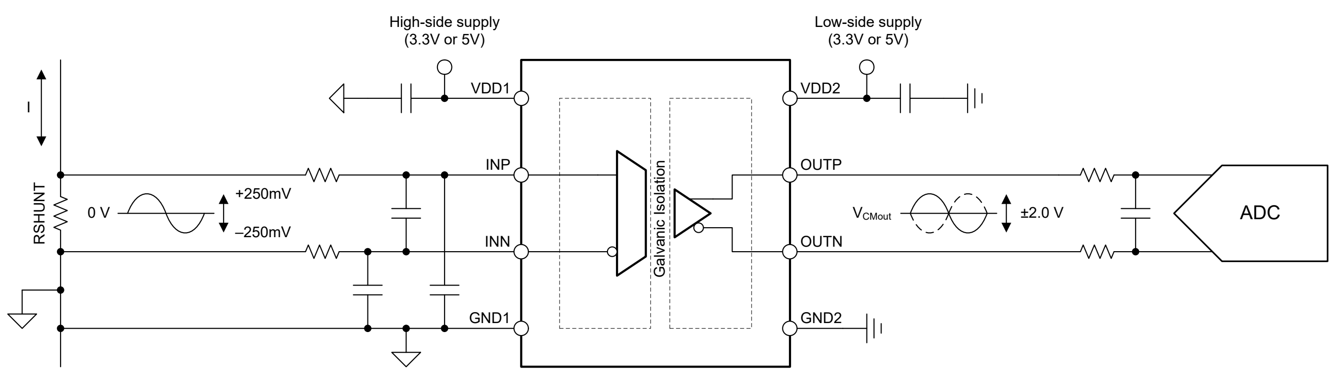
The AMC1200C outputs a differential signal proportional to the input voltage. The differential output is insensitive to ground shifts and enables routing the output signal over long distances.

The AMC1200C comes in 8-pin, wide-body SOIC and SOP packages. The device is fully specified over the temperature range from –40°C to +125°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
AMC1200C	DUB (SOP, 8)	9.5mm × 10.4mm
	DWV (SOIC, 8)	5.85mm × 11.5mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information* .
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application

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4 Pin Configuration and Functions

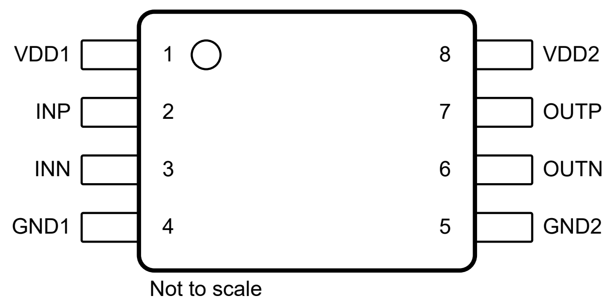


Figure 4-1. DWV and DUB Packages, 8-Pin SOIC and SOP (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VDD1	High-side power	High-side power supply(1)
2	INP	Analog input	Noninverting analog input(2)
3	INN	Analog Input	Inverting analog input(2)
4	GND1	High-side ground	High-side analog ground
5	GND2	Low-side ground	Low-side analog ground
6	OUTN	Analog output	Inverting analog output
7	OUTP	Analog output	Noninverting analog output
8	VDD2	Low-side power	Low-side power supply(1)

(1) See the *Power Supply Recommendations* section for power-supply decoupling recommendations.
(2) See the *Input Filter Design* section for input filter design.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Power-supply voltage	High-side VDD1 to GND1	–0.3	6.5	V
	Low-side VDD2 to GND2	–0.3	6.5	
Analog input voltage	INP, INN to GND1	GND1 – 4	VDD1 + 0.5	V
Analog output voltage	OUTP, OUTN to GND2	GND2 – 0.5	VDD2 + 0.5	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
VDD1	High-side power supply	VDD1 to GND1	3	5.0	5.5	V
VDD2	Low-side power supply	VDD2 to GND2	3	3.3	5.5	V
ANALOG INPUT						
$V_{Clipping}$	Nominal differential input voltage before clipping output	$V_{IN} = V_{INP} – V_{INN}$	–320		320	mV
V_{FSR}	Specified linear differential input voltage	$V_{IN} = V_{INP} – V_{INN}$	–250		250	mV
V_{CM}	Operating common-mode input voltage	$(V_{INP} + V_{INN}) / 2$ to GND1	–0.16		1	V
$C_{IN, EXT}$	Minimum external capacitance connected to the input	from INP to INN		10		nF
ANALOG OUTPUT						
C_{LOAD}	Capacitive load	OUTP or OUTN to GND2			500	pF
		OUTP to OUTN			250	
R_{LOAD}	Resistive load	OUTP or OUTN to GND2		10	1	kΩ
TEMPERATURE RANGE						
T_A	Specified ambient temperature	Specified ambient temperature	–40		125	°C

5.4 Thermal Information (DWV Package)

THERMAL METRIC[1]		DWV (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	14.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	61.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Thermal Information (DUB Package)

THERMAL METRIC[1]		DUB (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	75.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	27.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	39.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.6 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation (both sides)	VDD1 = VDD2 = 5.5V	91	mW
P_{D1}	Maximum power dissipation (high-side)	VDD1 = 5.5V	37	mW
P_{D2}	Maximum power dissipation (low-side)	VDD2 = 5.5V	54	mW

5.7 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
DWV PACKAGE				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	≥ 8.5	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	≥ 8.5	mm
DUB PACKAGE				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	≥ 7	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	≥ 7	mm
GENERAL				
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the insulation	≥ 15.4	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ $300V_{RMS}$	I-IV	
		Rated mains voltage ≤ $6000V_{RMS}$	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	2120	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	1500	V_{RMS}
		At DC voltage	2120	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification test), $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100% production test)	7000	V_{PK}
V_{IMP}	Maximum impulse voltage(3)	Tested in air, 1.2/50µs waveform per IEC 62368-1	7700	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	Tested in oil (qualification test), 1.2/50µs waveform per IEC 62368-1	10000	V_{PK}
q_{pd}	Apparent charge(5)	Method a, after input/output safety test subgroups 2 and 3, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 60s, $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 60s, $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s	≤ 5	
		Method b1, at preconditioning (type test) and routine test, $V_{pd(ini)} = 1.2x\ V_{IOTM}$, t_{ini} = 1s, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s	≤ 5	
		Method b2, at routine test (100% production)(7) $V_{pd(ini)} = V_{pd(m)} = 1.2 \times V_{IOTM}$, $t_{ini} = t_m$ = 1s	≤ 5	
C_{IO}	Barrier capacitance, input to output(6)	$V_{IO} = 0.5V_{PP}$ at 1MHz	≅1.5	pF
R_{IO}	Insulation resistance, input to output(6)	V_{IO} = 500V at T_A = 25°C	$> 10^{12}$	Ω
		V_{IO} = 500V at 100°C ≤ T_A ≤ 125°C	$> 10^{11}$	
		V_{IO} = 500V at T_S = 150°C	$> 10^{9}$	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification test), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production test)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Maintain the creepage and clearance distance of a board design to make sure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).

(6) All pins on each side of the barrier are tied together, creating a two-pin device.
(7) Either method b1 or b2 is used in production.

5.8 Safety-Related Certifications

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN IEC 62368-1 (VDE 0868-1), EN IEC 62368-1, IEC 62368-1 Clause : 5.4.3 ; 5.4.4.4 ; 5.4.9	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Basic Insulation	Single protection
Certificate number: Pending	File number: Pending

5.9 Safety Limiting Values (DWV Package)

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 102.8°C/W, VDDx = 5.5V, T_J = 150°C, T_A = 25°C			220	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 102.8°C/W, T_J = 150°C, T_A = 25°C			1210	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum supply voltage for high-side and low-side.

5.10 Safety Limiting Values (DUB Package)

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 75°C/W, VDDx = 5.5V, T_J = 150°C, T_A = 25°C			303	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 75°C/W, T_J = 150°C, T_A = 25°C			1666	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum supply voltage for high-side and low-side.

5.11 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD1 = 3.0V to 5.5V, VDD2 = 3.0V to 5.5V, V_{INP} = –250mV to +250mV, and V_{INN} = 0V; typical specifications are at T_A = 25°C, VDD1 = 5V, and VDD2 = 3.3V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
C_{IN}	Effective input sampling capacitance			1.8		pF
R_{IN}	Input impedance		25	27.5	30	kΩ
I_{INP}	Input current	$V_{IN} = (V_{INP} – V_{INN}) = V_{FSR, MAX}$		9		µA
I_{INN}	Input current	$V_{IN} = (V_{INP} – V_{INN}) = V_{FSR, MAX}$		–9		µA
CMTI	Common-mode transient immunity	|GND1 – GND2| = 1kV	150			V/ns
ANALOG OUTPUT						
	Nominal gain			8		V/V
V_{CMout}	Common-mode output voltage		1.39	1.44	1.49	V
$V_{CLIPout}$	Clipping differential output voltage	$V_{OUT} = (V_{OUTP} – V_{OUTN})$; $\|V_{IN}\| = \|V_{INP} – V_{INN}\| > \|V_{Clipping}\|$	–2.52	±2.49	2.52	V
$V_{FAILSAFE}$	Failsafe differential output voltage	VDD1 missing	–2.63	–2.57	2.53	V
R_{OUT}	Output resistance	On OUTP or OUTN		<0.2		Ω
	Output short-circuit current	On OUTP or OUTN, sourcing or sinking, INN = INP = GND1, outputs shorted to either GND2 or VDD2		11		mA
DC ACCURACY						
V_{OS}	Offset voltage(1) (2)	T_A = 25°C, INP = INN = GND1	–0.2	±0.01	0.2	mV
TCV_{OS}	Offset drift(1) (2) (4)		–2	±0.25	2	µV/°C
E_G	Gain error(1)	T_A = 25°C	–0.25%	±0.04%	0.25%	
TCE_G	Gain drift(1) (5)		–35	±5	35	ppm/°C
	Nonlinearity		–0.04%		0.04%	
	Output noise	INP = INN = GND1, f_{IN} = 0Hz, BW = 100kHz brickwall filter		400		$µV_{RMS}$
CMRR	Common-mode rejection ratio	f_{IN} = 0Hz, $V_{CM\ min} \le V_{CM} \le V_{CM\ max}$		–100		dB
		f_{IN} = 10kHz, $V_{CM\ min} \le V_{CM} \le V_{CM\ max}$		–87		
PSRR	Power-supply rejection ratio(2)	VDD1 DC PSRR, INP = INN = GND1, VDD1 from 3V to 5.5V		–89		dB
		VDD1 AC PSRR, INP = INN = GND1, VDD1 with 10kHz / 100mV ripple		–78		
		VDD2 DC PSRR, INP = INN = GND1, VDD2 from 3V to 5.5V		–110		
		VDD2 AC PSRR, INP = INN = GND1, VDD2 with 10kHz / 100mV ripple		–79		
AC ACCURACY						
BW	Output bandwidth		250	280		kHz
THD	Total harmonic distortion(3)	f_{IN} = 10 kHz		–82		dB
SNR	Signal-to-noise ratio	f_{IN} = 1kHz, BW = 10kHz	80.5	85		dB
		f_{IN} = 10kHz, BW = 100kHz		77		
POWER SUPPLY						
IDD1	High-side supply current			5.4	6.7	mA
IDD2	Low-side supply current			6.4	9.9	mA
$VDD1_{UV}$	High-side undervoltage detection threshold	VDD1 rising	2.5	2.6	2.7	V
		VDD1 falling	1.9	2.0	2.1	

5.11 Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD1 = 3.0V to 5.5V, VDD2 = 3.0V to 5.5V, V_{INP} = –250mV to +250mV, and V_{INN} = 0V; typical specifications are at T_A = 25°C, VDD1 = 5V, and VDD2 = 3.3V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$VDD2_{UV}$	Low-side undervoltage detection threshold	VDD2 rising	2.3	2.5	2.7	V
		VDD2 falling	1.9	2.05	2.2	

(1) The typical value includes one standard deviation (*sigma*) at nominal operating conditions.
(2) This parameter is input referred.
(3) THD is the ratio of the rms sum of the amplitues of first five higher harmonics to the amplitude of the fundamental.
(4) Offset error temperature drift is calculated using the box method, as described by the following equation: $TCV_{OS} = (V_{OS,MAX} - V_{OS,MIN}) / TempRange$ where $V_{OS,MAX}$ and $V_{OS,MIN}$ refer to the maximum and minimum V_{OS} values measured within the temperature range (–40 to 125℃).
(5) Gain error temperature drift is calculated using the box method, as described by the following equation: $TCE_G\ (ppm) = ((E_{G,MAX} - E_{G,MIN}) / TempRange) \times 10^4$ where $E_{G,MAX}$ and $E_{G,MIN}$ refer to the maximum and minimum E_G values (in %) measured within the temperature range (–40 to 125℃).

5.12 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output signal rise time			1.7		µs
t_f	Output signal fall time			1.7		µs
	V_{INx} to V_{OUTx} signal delay (50% - 10%)	Unfiltered output		0.8	1.3	µs
	V_{INx} to V_{OUTx} signal delay (50% - 50%)	Unfiltered output		1.6	2.1	µs
	V_{INx} to V_{OUTx} signal delay (50% - 90%)	Unfiltered output		2.5	3	µs
t_{AS}	Analog settling time	VDD1 step to 3.0V with VDD2 ≥ 3.0V, to V_{OUTP}, V_{OUTN} valid, 0.1% settling		20	100	µs

5.13 Timing Diagram

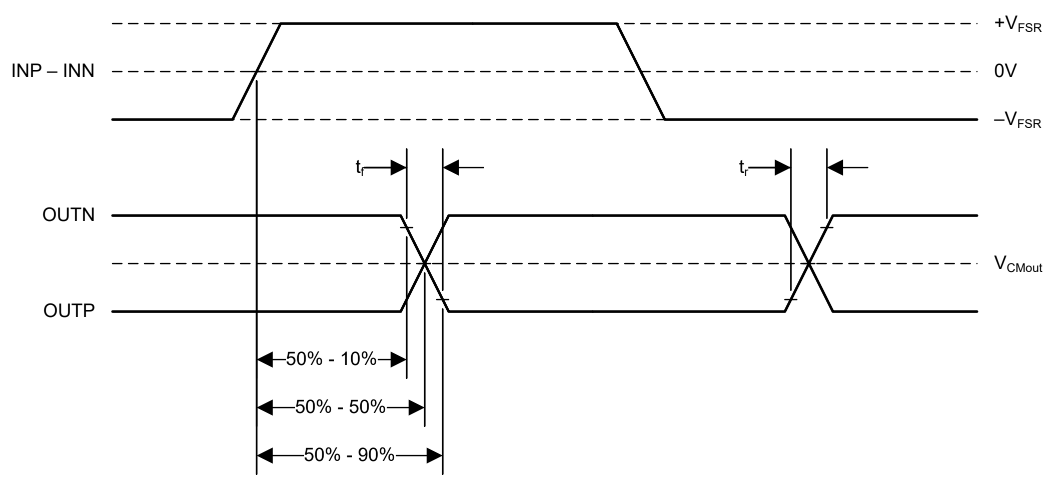


Figure 5-1. Rise, Fall, and Delay Time Waveforms

5.14 Insulation Characteristics Curves

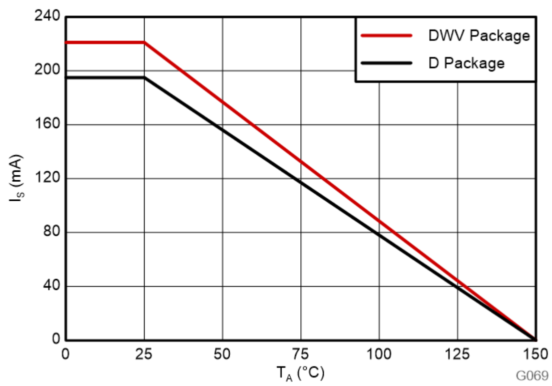


Figure 5-2. Thermal Derating Curve for Safety-Limiting Current per VDE

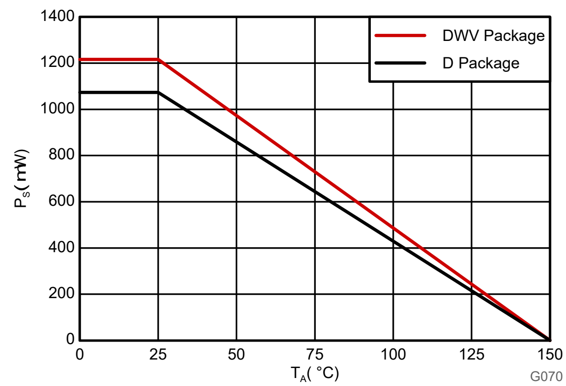
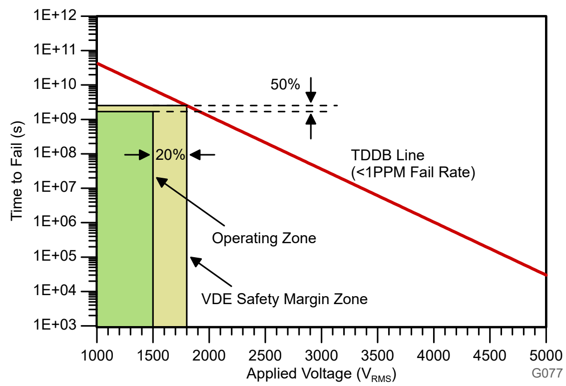


Figure 5-3. Thermal Derating Curve for Safety-Limiting Power per VDE



T_A up to 150°C, stress-voltage frequency = 60Hz, isolation working voltage = 1500V_{RMS}, projected operating lifetime ≥50 years

Figure 5-4. Isolation Capacitor Lifetime Projection

5.15 Typical Characteristics

at VDD1 = 5V, VDD2 = 3.3V, VINP = –250mV to 250mV, VINN = 0V, and f_{IN} = 10kHz (unless otherwise noted)

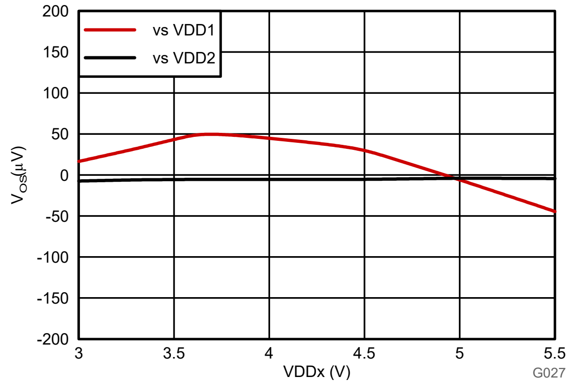


Figure 5-5. Input Offset Voltage vs Supply Voltage

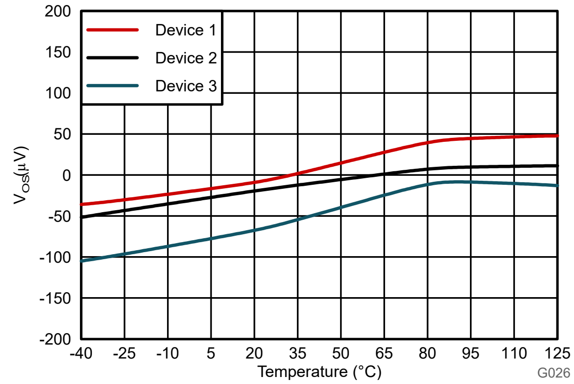


Figure 5-6. Input Offset Voltage vs Temperature

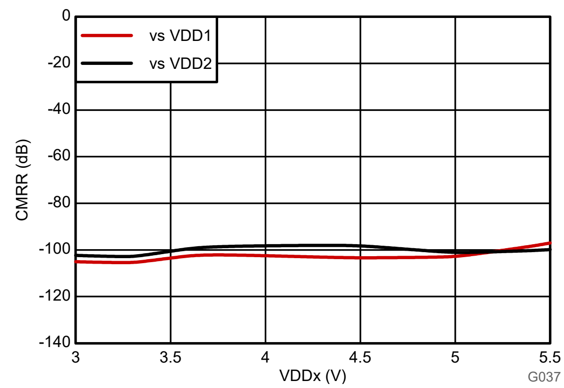


Figure 5-7. Common-Mode Rejection Ratio vs Supply Voltage

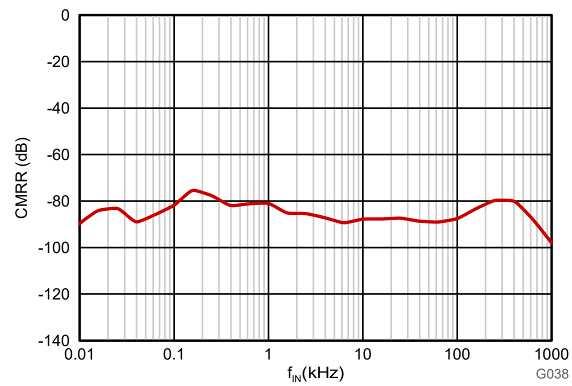


Figure 5-8. Common-Mode Rejection Ratio vs Input Frequency

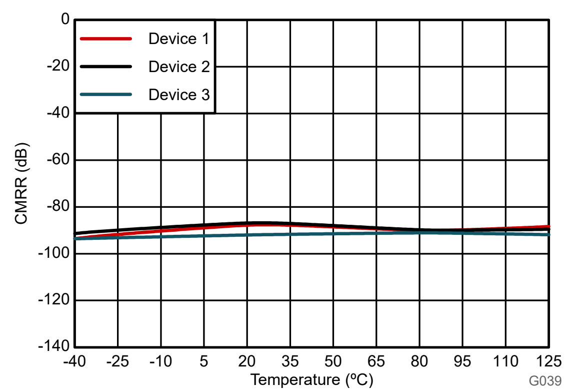


Figure 5-9. Common-Mode Rejection Ratio vs Temperature

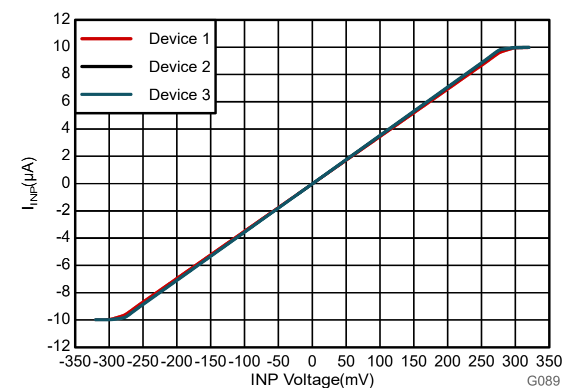


Figure 5-10. Input Current vs Input Voltage

5.15 Typical Characteristics (continued)

at VDD1 = 5V, VDD2 = 3.3V, VINP = –250mV to 250mV, VINN = 0V, and f_{IN} = 10kHz (unless otherwise noted)

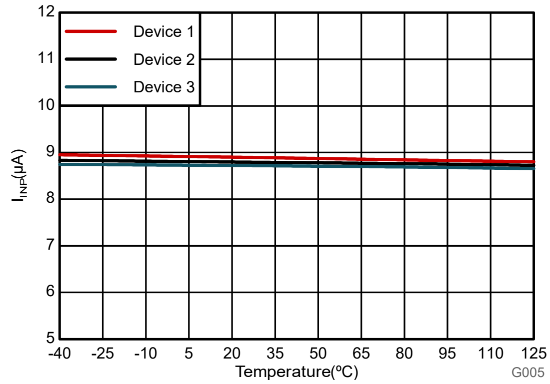


Figure 5-11. Input Current vs Temperature

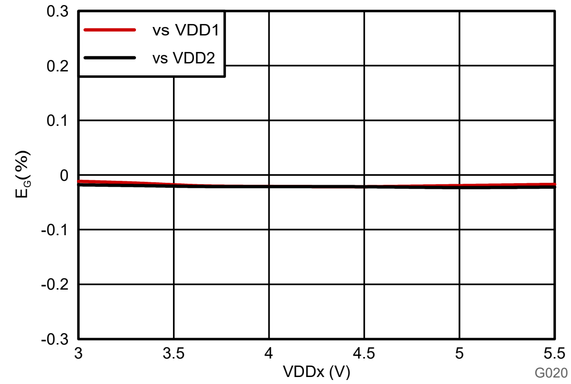


Figure 5-12. Gain Error vs Supply Voltage

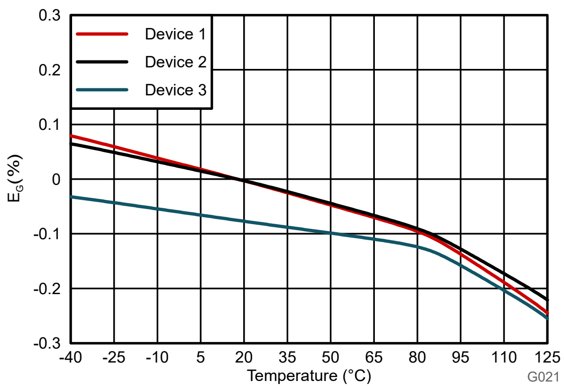


Figure 5-13. Gain Error vs Temperature

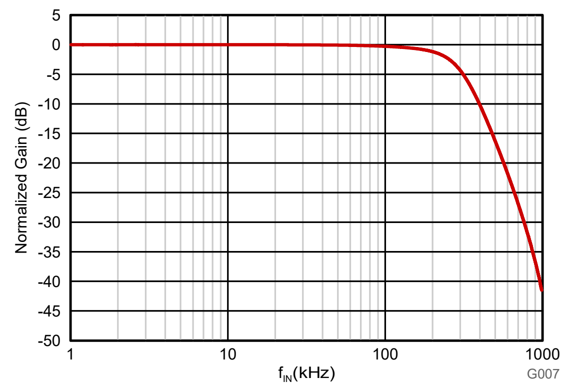


Figure 5-14. Normalized Gain vs Input Frequency

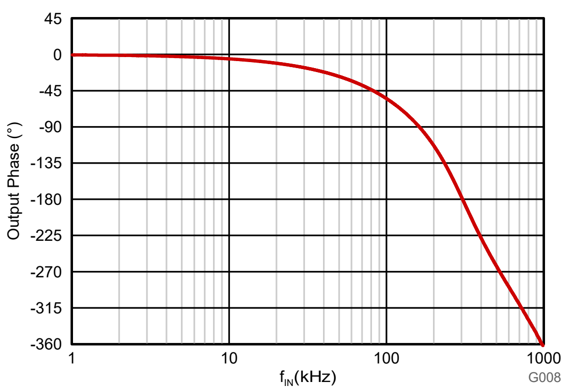


Figure 5-15. Output Phase vs Input Frequency

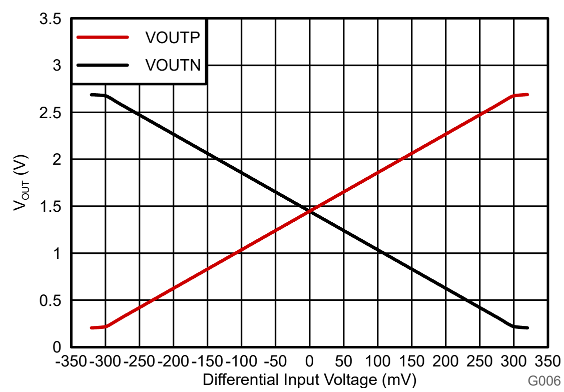
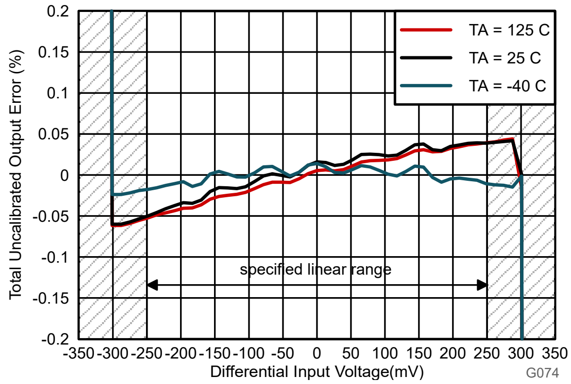


Figure 5-16. Output Voltage vs Input Voltage

5.15 Typical Characteristics (continued)

at VDD1 = 5V, VDD2 = 3.3V, VINP = –250mV to 250mV, VINN = 0V, and f_{IN} = 10kHz (unless otherwise noted)



Total uncalibrated output error is defined as: $(V_{OUT} / G - V_{IN}) / (V_{Clipping} \times 100)$, where G is the nominal gain of the device (8.0V/V) and $V_{Clipping}$ is 0.32V

Figure 5-17. Unadjusted Error vs Input Voltage

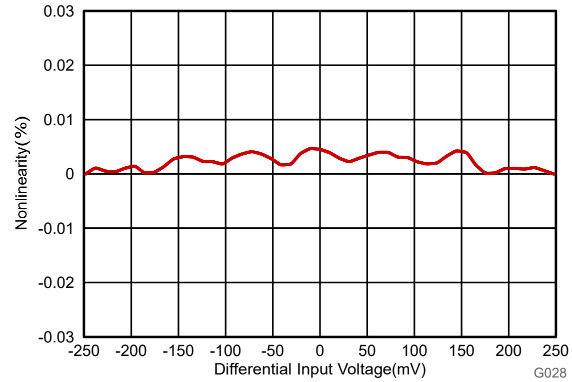


Figure 5-18. Nonlinearity vs Input Voltage

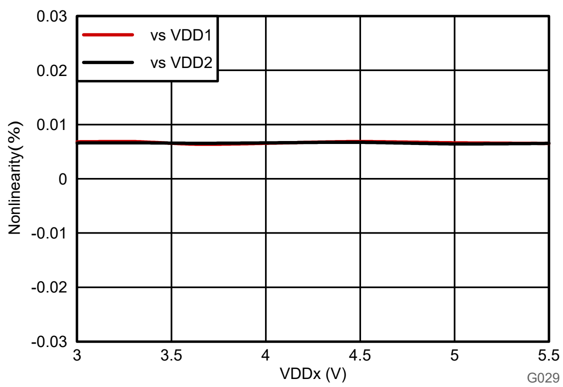


Figure 5-19. Nonlinearity vs Supply Voltage

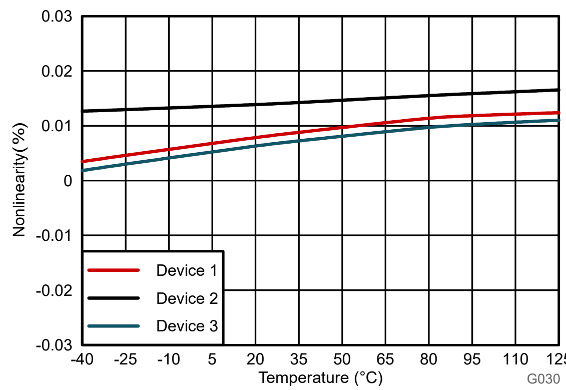


Figure 5-20. Nonlinearity vs Temperature

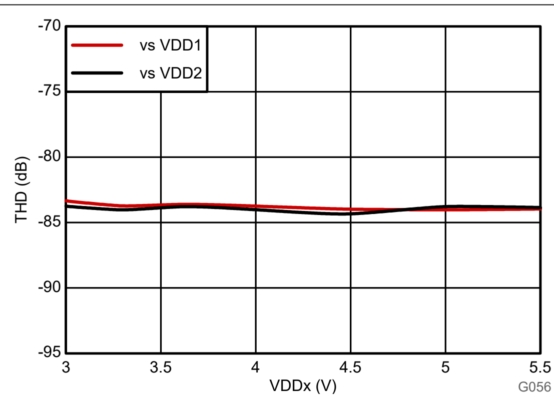


Figure 5-21. Total Harmonic Distortion vs Supply Voltage

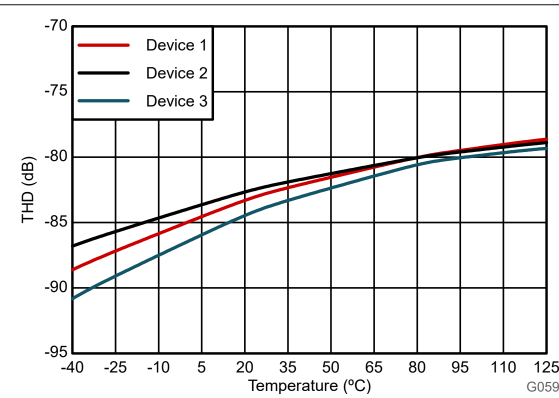


Figure 5-22. Total Harmonic Distortion vs Temperature

5.15 Typical Characteristics (continued)

at VDD1 = 5V, VDD2 = 3.3V, VINP = –250mV to 250mV, VINN = 0V, and f_{IN} = 10kHz (unless otherwise noted)

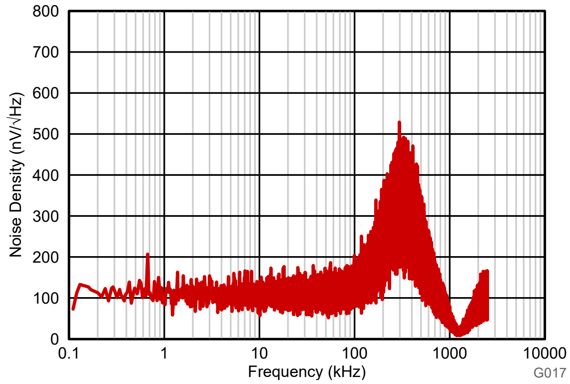


Figure 5-23. Input-Referred Noise Density vs Frequency

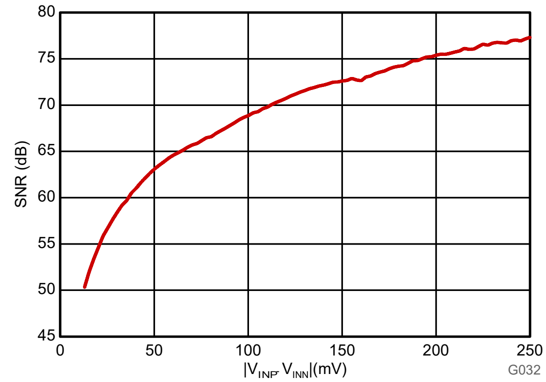


Figure 5-24. Signal-to-Noise Ratio vs Input Voltage

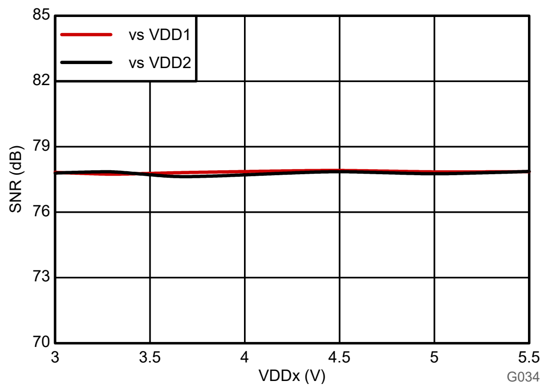


Figure 5-25. Signal-to-Noise Ratio vs Supply Voltage

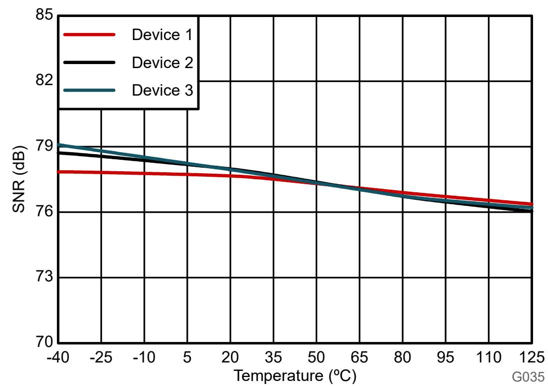


Figure 5-26. Signal-to-Noise Ratio vs Temperature

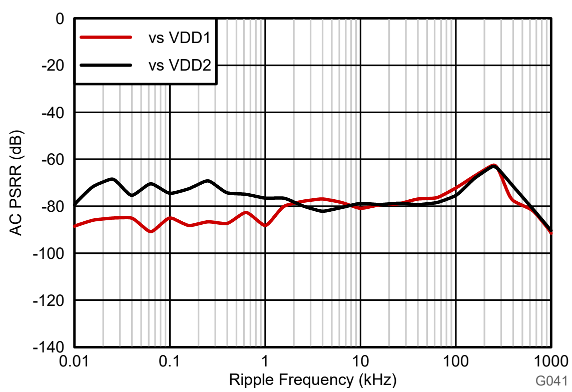


Figure 5-27. Power-Supply Rejection Ratio vs Ripple Frequency

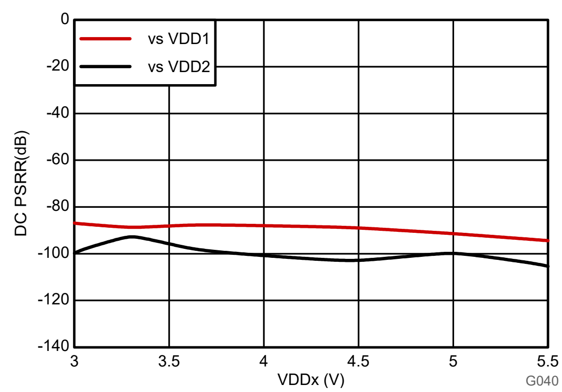


Figure 5-28. Power-Supply Rejection Ratio vs Supply Voltage

5.15 Typical Characteristics (continued)

at VDD1 = 5V, VDD2 = 3.3V, VINP = –250mV to 250mV, VINN = 0V, and f_{IN} = 10kHz (unless otherwise noted)

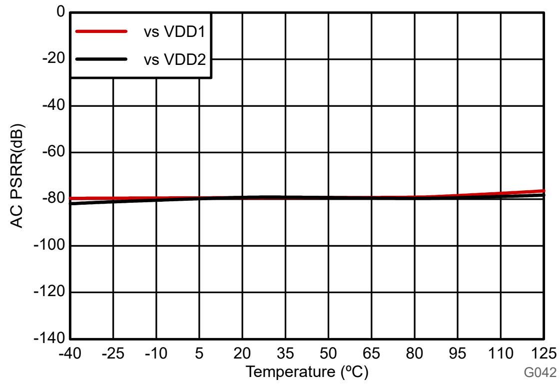


Figure 5-29. Power-Supply Rejection Ratio vs Temperature

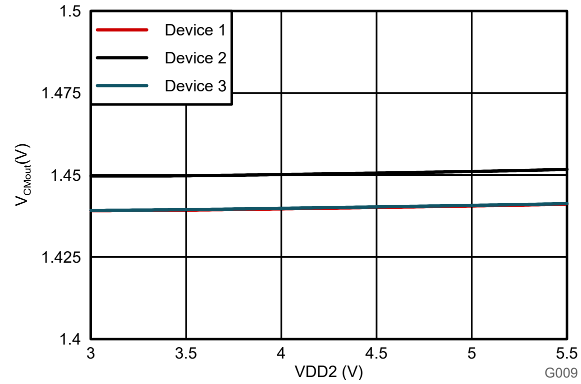


Figure 5-30. Output Common-Mode Voltage vs Low-Side Supply Voltage

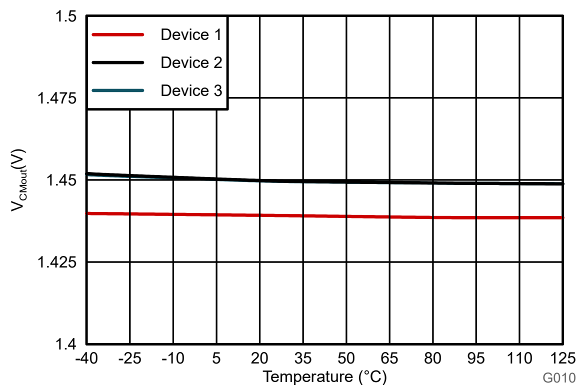


Figure 5-31. Output Common-Mode Voltage vs Temperature

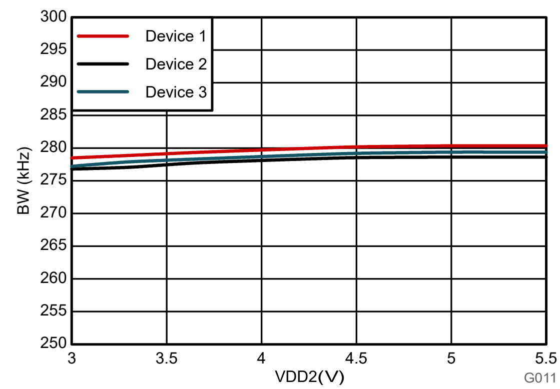


Figure 5-32. Output Bandwidth vs Low-Side Supply Voltage

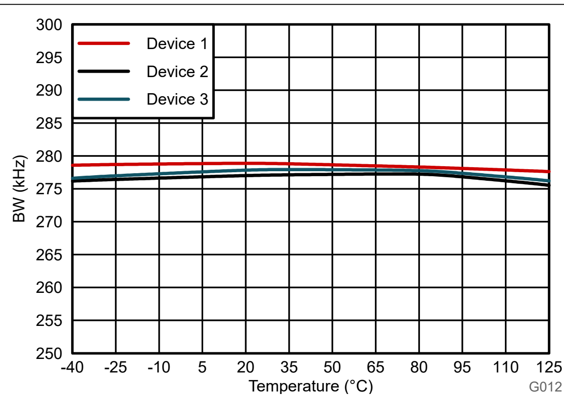


Figure 5-33. Output Bandwidth vs Temperature

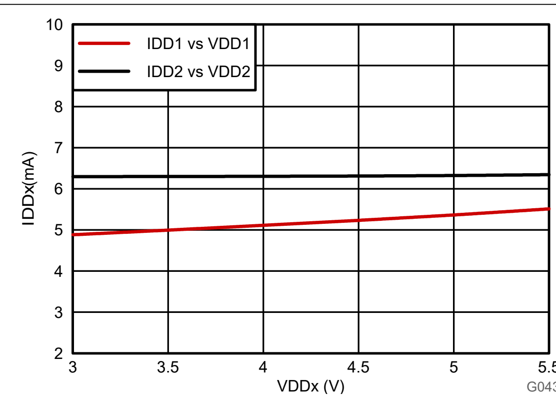


Figure 5-34. Supply Current vs Supply Voltage

5.15 Typical Characteristics (continued)

at VDD1 = 5V, VDD2 = 3.3V, VINP = –250mV to 250mV, VINN = 0V, and f_{IN} = 10kHz (unless otherwise noted)

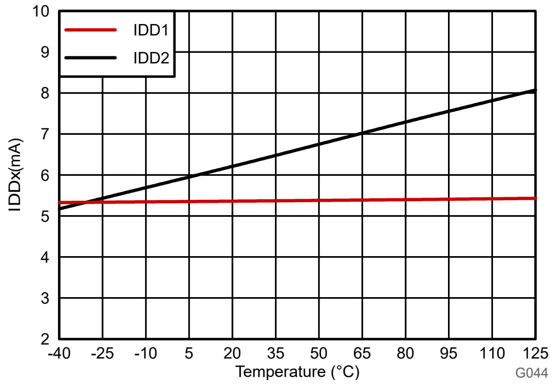


Figure 5-35. Supply Current vs Temperature

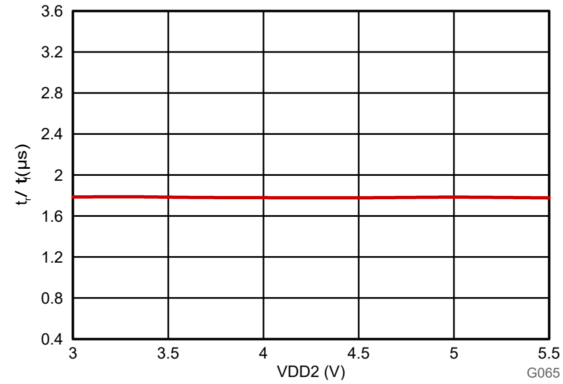


Figure 5-36. Output Rise and Fall Time vs Low-Side Supply

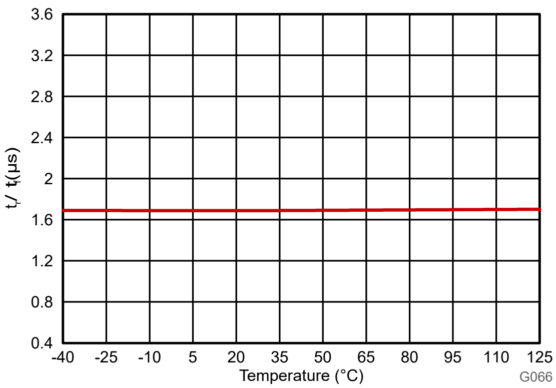


Figure 5-37. Output Rise and Fall Time vs Temperature

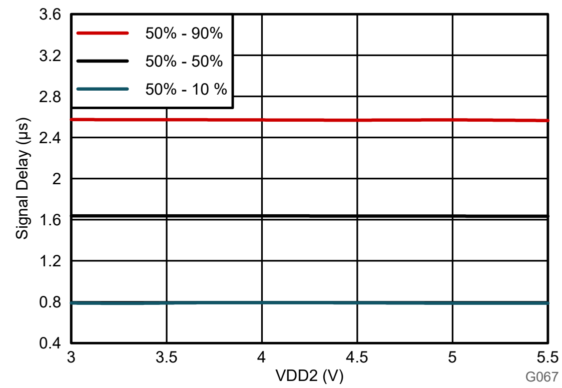


Figure 5-38. V_{IN} to V_{OUT} Signal Delay vs Low-Side Supply Voltage

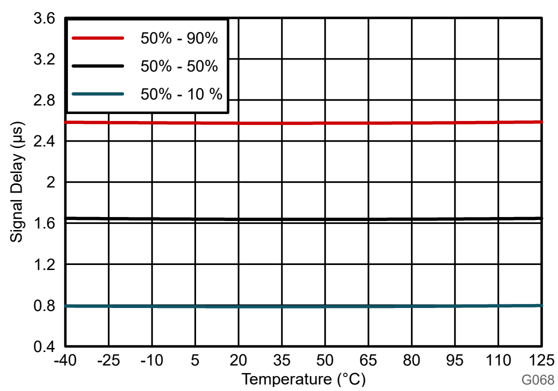


Figure 5-39. V_{IN} to V_{OUT} Signal Delay vs Temperature

6 Detailed Description

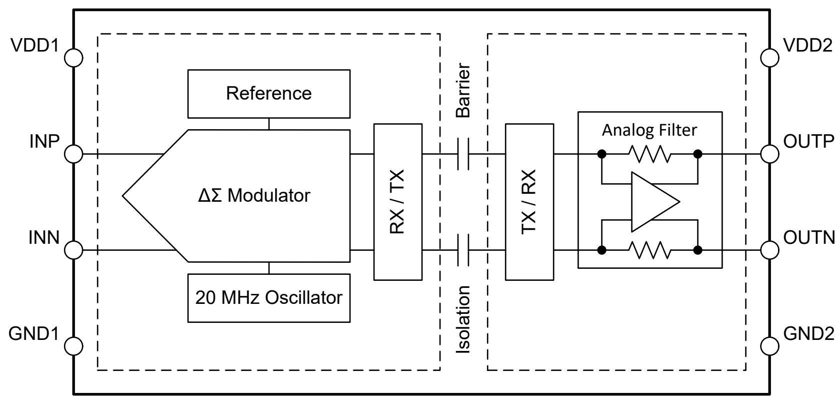
6.1 Overview

The AMC1200C is a precision, galvanically isolated amplifier with a ±250mV, differential input and differential output. The input stage of the device drives a second-order, delta-sigma (ΔΣ) modulator. The modulator converts the analog input signal into a digital bitstream that is transferred across the isolation barrier that separates the high-side from the low-side.

On the low-side, the received bitstream is processed by a fourth-order analog filter that outputs a differential signal at the OUTP and OUTN pins. This differential output signal is proportional to the input signal.

The SiO_2-based, capacitive isolation barrier supports a high level of magnetic field immunity, as described in the *ISO72x Digital Isolator Magnetic-Field Immunity* application note. The digital modulation used in the AMC1200C transmits data across the isolation barrier. This modulation, and the isolation barrier characteristics, result in high reliability and high common-mode transient immunity.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Analog Input

The high-impedance input buffer on the INP pin feeds a second-order, switched-capacitor, feed-forward ΔΣ modulator. The modulator converts the analog signal into a bitstream that is transferred across the isolation barrier, as described in the *Isolation Channel Signal Transmission* section.

There are two restrictions on the analog input signal. First, if the input voltage exceeds the value specified in the *Absolute Maximum Ratings* table, the input current must be limited to 10mA. This limitation is caused by the device input electrostatic discharge (ESD) diodes turning on. Second, linearity and noise performance are specified only when the input voltage is within the linear full-scale range (V_{FSR}). V_{FSR} is specified in the *Recommended Operating Conditions* table.

6.3.2 Isolation Channel Signal Transmission

As shown in Figure 6-1, the AMC1200C uses an on-off keying (OOK) modulation scheme to transmit the modulator output bitstream across the SiO_2-based isolation barrier. The transmit driver (TX) is illustrated in the *Functional Block Diagram* . TX transmits an internally generated, high-frequency carrier across the isolation barrier to represent a digital *one*. However, TX does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC1200C is 480MHz.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and provides the input to the analog filter. The AMC1200C transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and the lowest level of radiated emissions. The high-frequency carrier and RX/TX buffer switching cause these emissions.

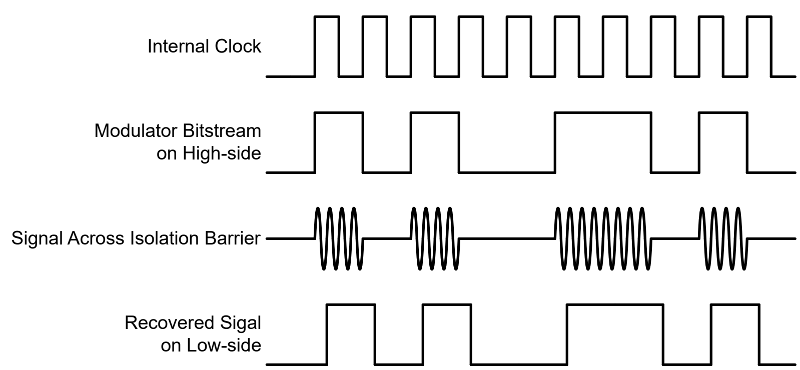


Figure 6-1. OOK-Based Modulation Scheme

6.3.3 Analog Output

The AMC1200C provides a differential analog output voltage on the OUTP and OUTN pins proportional to the input voltage. For input voltages in the range from $V_{FSR, MIN}$ to $V_{FSR, MAX}$, the device has a linear response with an output voltage equal to:

$$V_{OUT} = V_{OUTP} - V_{OUTN} = 8.0 \times V_{IN} = 8.0 \times (V_{INP} - V_{INN}) \quad (1)$$

At zero input, both pins output the same common-mode output voltage V_{CMout}, as specified in the *Electrical Characteristics* table. For absolute input voltages greater than $|V_{FSR}|$ but less than $|V_{Clipping}|$, the differential output voltage continues to increase in magnitude, but with reduced linearity performance. The outputs saturate at a differential output voltage of $V_{CLIPout}$, as shown in Figure 6-2, if the input voltage exceeds the $V_{Clipping}$ value.

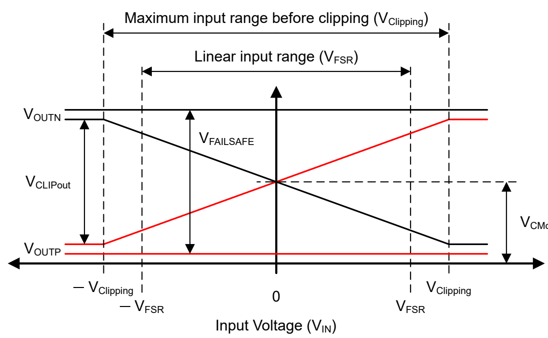


Figure 6-2. Input to Output Transfer Curve of the AMC1200C

The AMC1200C output offers a fail-safe feature that simplifies diagnostics on a system level. Figure 6-2 shows the behavior in fail-safe mode, in which the AMC1200C outputs a negative differential output voltage that does not occur under normal operating conditions. The fail-safe output is active:

- When the high-side supply VDD1 of the AMC1200C device is missing
- When the high-side supply VDD1 falls below the undervoltage threshold $VDD1_{UV}$

Use the maximum $V_{FAILSAFE}$ voltage specified in the *Electrical Characteristics* table as a reference value for fail-safe detection on a system level.

6.4 Device Functional Modes

The AMC1200C operates in one of the following states:

- Off-state: The low-side supply (VDD2) is below the $VDD2_{UV}$ threshold. The device is not responsive. OUTP and OUTN are in Hi-Z state. Internally, OUTP and OUTN are clamped to VDD2 and GND2 by ESD protection diodes.
- Missing high-side supply: The low-side of the device (VDD2) is supplied and within recommended operating conditions. The high-side supply (VDD1) is below the $VDD1_{UV}$ threshold. The device outputs the $V_{FAILSAFE}$ voltage.
- Analog input overrange (positive full-scale input): VDD1 and VDD2 are within recommended operating conditions but the analog input voltage V_{IN} is above the maximum clipping voltage $V_{Clipping, MAX}$. The device outputs positive $V_{CLIPout}$.
- Analog input underrange (negative full-scale input): VDD1 and VDD2 are within recommended operating conditions but the analog input voltage V_{IN} is below the minimum clipping voltage $V_{Clipping, MIN}$. The device outputs negative $V_{CLIPout}$.
- Normal operation: VDD1, VDD2, and V_{IN} are within the recommended operating conditions. The device outputs a differential voltage that is proportional to the input voltage.

Table 6-1 lists the operating modes.

Table 6-1. Device Operational Modes

OPERATING CONDITION	VDD1	VDD2	V_{IN}	DEVICE RESPONSE
Off	Don't care	VDD2 < $VDD2_{UV}$	Don't care	OUTP and OUTN are in Hi-Z state. Internally, OUTP and OUTN are clamped to VDD2 and GND2 by ESD protection diodes.
Missing high-side supply	VDD1 < $VDD1_{UV}$	Valid[1]	Don't care	The device outputs the $V_{FAILSAFE}$ voltage.
Input overrange	Valid[1]	Valid[1]	$V_{IN} > V_{Clipping, MAX}$	The device outputs positive $V_{CLIPout}$.
Input underrange	Valid[1]	Valid[1]	$V_{IN} < V_{Clipping, MIN}$	The device outputs negative $V_{CLIPout}$.
Normal operation	Valid[1]	Valid[1]	Valid[1]	The device outputs a differential voltage that is proportional to the input voltage.

(1) *Valid* denotes operation within the recommended operating conditions.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The AMC1200C has low analog input voltage range, high accuracy, low temperature drift, and high common-mode transient immunity. The AMC1200C is primarily designed for shunt-based current-sensing applications where accurate current monitoring is required in the presence of high common-mode voltages. The AMC1200C is preferred for isolated current sensing in motor drives, frequency inverters, and uninterruptible power-supply applications.

7.2 Typical Application

The following image shows the AMC1200C in a typical application. The load current flowing through an external shunt resistor RSHUNT produces a voltage drop. The AMC1200C high-side circuitry senses the voltage drop across the shunt resistor, then digitizes and transfers data across the isolation barrier to the low side. Low-side circuitry reconstructs the digitized data into an analog signal and provides the signal as a differential voltage on the output pins.

The differential input, differential output, and high common-mode transient immunity (CMTI) of the AMC1200C provide reliable and accurate operation even in high-noise environments.

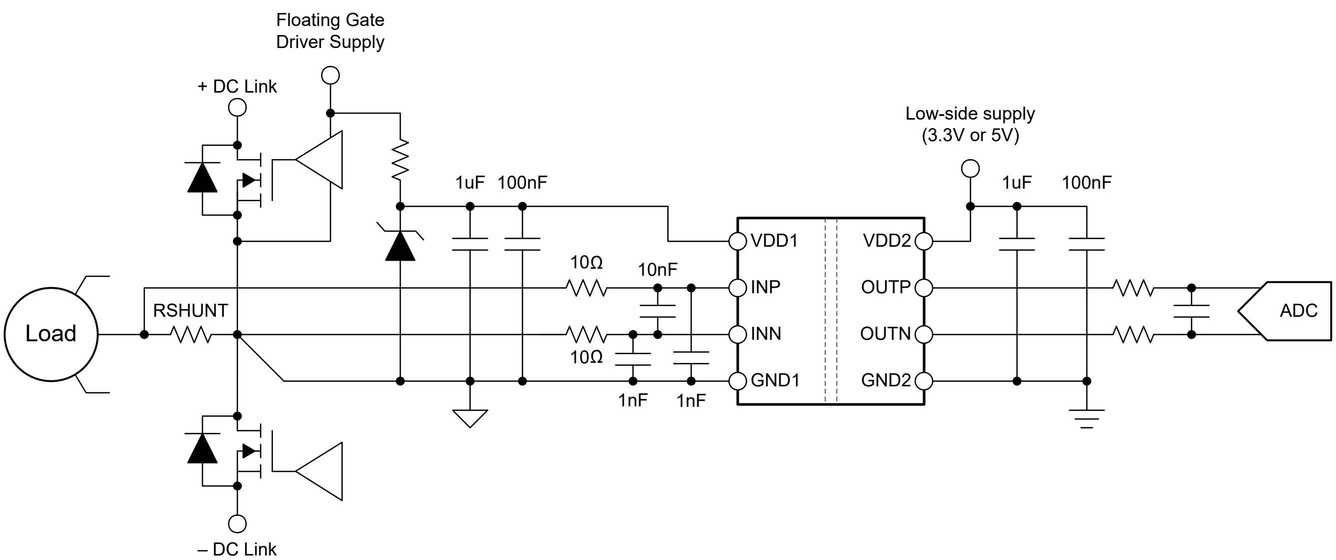


Figure 7-1. Using the AMC1200C for Current Sensing in a Typical Application

7.2.1 Design Requirements

Table 7-1 lists the parameters for this typical application.

Table 7-1. Design Requirements

PARAMETER	VALUE
High-side supply voltage	3.3V or 5V
Low-side supply voltage	3.3V or 5V
Voltage drop across RSHUNT for a linear response	±250mV(maximum)

7.2.2 Detailed Design Procedure

In the *Typical Application* figure, the high-side power supply (VDD1) for the AMC1200C is derived from the floating power supply of the upper gate driver.

The floating ground reference (GND1) is derived from the end of the shunt resistor that is connected to the negative input of the AMC1200C (INN). If a four-pin shunt is used, the inputs of the AMC1200C are connected to the inner leads. GND1 is then connected to the outer lead on the INN-side of the shunt. To minimize offset and improve accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor. Do not short GND1 to INN directly at the device input; see the *Layout Example* section for more details.

Use Ohm's Law to calculate the voltage drop across the shunt resistor (V_{SHUNT}) for the desired measured current:

$$V_{SHUNT} = I \times RSHUNT \tag{2}$$

Select a RSHUNT value to satisfy the following two conditions:

- First, the voltage drop caused by the nominal current range does not exceed the recommended differential input voltage range of $V_{SHUNT} \le \pm 250mV$.
- Secondly, the voltage drop caused by the maximum allowed overcurrent does not exceed the input voltage that causes a clipping output. Keep $V_{SHUNT} \le V_{Clipping}$.

7.2.2.1 Input Filter Design

Place a differential RC filter (R1, R2, C5) in front of the isolated amplifier to improve signal-to-noise performance of the signal path. Design the input filter such that:

- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency (20MHz) of the ΔΣ modulator
- The input bias current does not generate significant voltage drop across the DC impedance of the input filter
- The impedances measured from the analog inputs are equal

Place capacitors C6 and C7 to improve common-mode rejection at high frequencies (>1MHz) and to improve offset voltage performance. For best performance, verify C6 matches the value of C7 and that both capacitors are 10 to 20 times lower in value than C5. NP0-type capacitors offer low temperature drift and low voltage coefficients, and are preferred for common-mode filtering.

For most applications, the structure shown in Figure 7-2 achieves excellent performance.

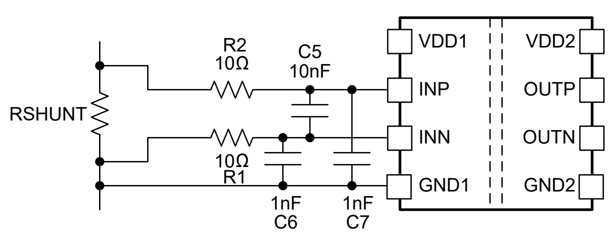


Figure 7-2. Input Filter

7.2.2.2 Differential-to-Single-Ended Output Conversion

Many systems use ADCs with single-ended inputs that cannot connect directly to the differential output of the AMC1200C. Figure 7-3 shows a circuit for converting the differential output signal into a single-ended signal in front of the ADC. For R1 = R3 and R2 = R4, the output voltage equals (R2 / R1) × (V_{OUTP} – V_{OUTN}) + V_{REF}. For C1 = C2 the bandwidth of the filter becomes 1 / (2 × π × C1 × R1). Configure the bandwidth of the filter to match the bandwidth requirement of the system. For best linearity, use capacitors with low voltage coefficients (such as NP0-type capacitors). For most applications, R1 = R2 = R3 = R4 = 3.3kΩ and C1 = C2 = 330pF yield good performance.

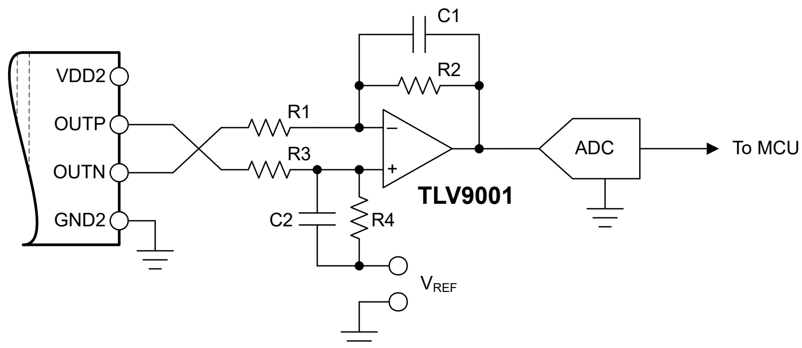


Figure 7-3. Connecting the AMC1200C Output to a Single-Ended Input ADC

The following reference guides provide further information on the general procedure to design the filtering and driving stages of SAR ADCs. These reference guides are available for download at www.ti.com.

- *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* reference guide
- *18-Bit Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guide

7.2.3 Application Curve

One important aspect of power-stage design is the effective detection of an overcurrent condition to protect the switching devices and passive components from damage. To power off the system quickly in the event of an overcurrent condition, the isolated amplifier is required to have low signal delay. Figure 7-4 shows the typical full-scale step response of the AMC1200C.

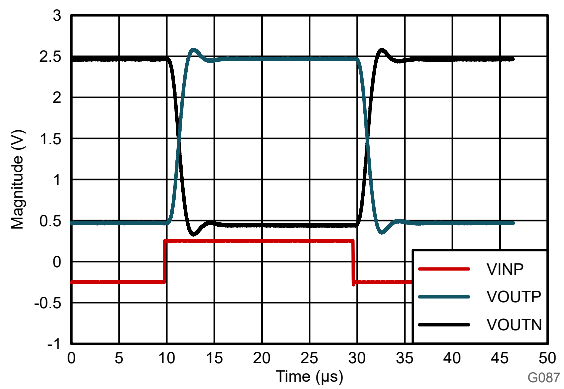


Figure 7-4. Step Response of the AMC1200C

7.3 Best Design Practices

Place a minimum 10nF capacitor at the device input (from INP to INN). This capacitor helps avoid voltage droop at the input during the sampling period of the switched-capacitor input stage.

Do not short GND1 to INN directly at the device input. For best accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor. See the *Layout Example* section for more details.

Do not leave the inputs of the AMC1200C unconnected (floating) when the device is powered up. If the device inputs are left floating, the input bias current potentially drives the inputs to a positive value that exceeds the operating common-mode input voltage. This condition causes the device to output the fail-safe voltage described in the *Analog Output* section.

Connect the high-side ground (GND1) to INN, either by a hard short or through a resistive path. A DC current path between INN and GND1 is required to define the input common-mode voltage. Do not exceed the input common-mode range specified in the *Recommended Operating Conditions* table.

7.4 Power Supply Recommendations

In a typical application, the high-side power supply (VDD1) for the AMC1200C is generated from the low-side supply (VDD2) by an isolated DC/DC converter. A low-cost option is based on the push-pull driver SN6501 and a transformer that supports the desired isolation voltage ratings.

The AMC1200C does not require any specific power-up sequencing. The high-side power supply (VDD1) is decoupled with a low-ESR, 100nF capacitor (C1) parallel to a low-ESR, 1µF capacitor (C2). The low-side power supply (VDD2) is equally decoupled with a low-ESR, 100nF capacitor (C3) parallel to a low-ESR, 1µF capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible. Figure 7-5 shows a decoupling diagram for the AMC1200C.

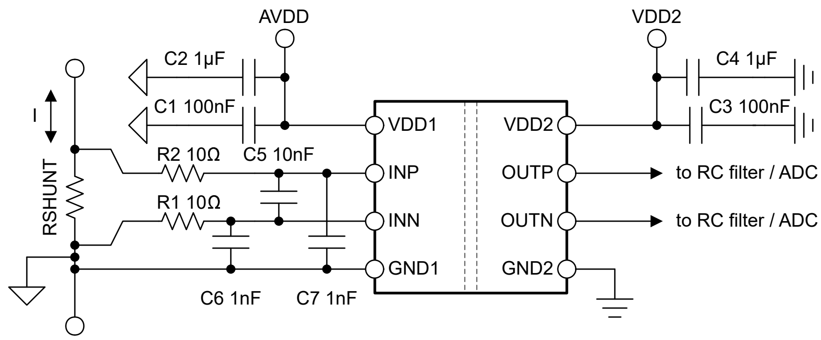


Figure 7-5. Decoupling of the AMC1200C

Verify capacitors provide adequate *effective* capacitance under the applicable DC bias conditions experienced in the application. Multilayer ceramic capacitors (MLCC) typically exhibit only a fraction of the nominal capacitance under real-world conditions. Consider this factor when selecting these capacitors. This issue is especially acute in low-profile capacitors, where the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

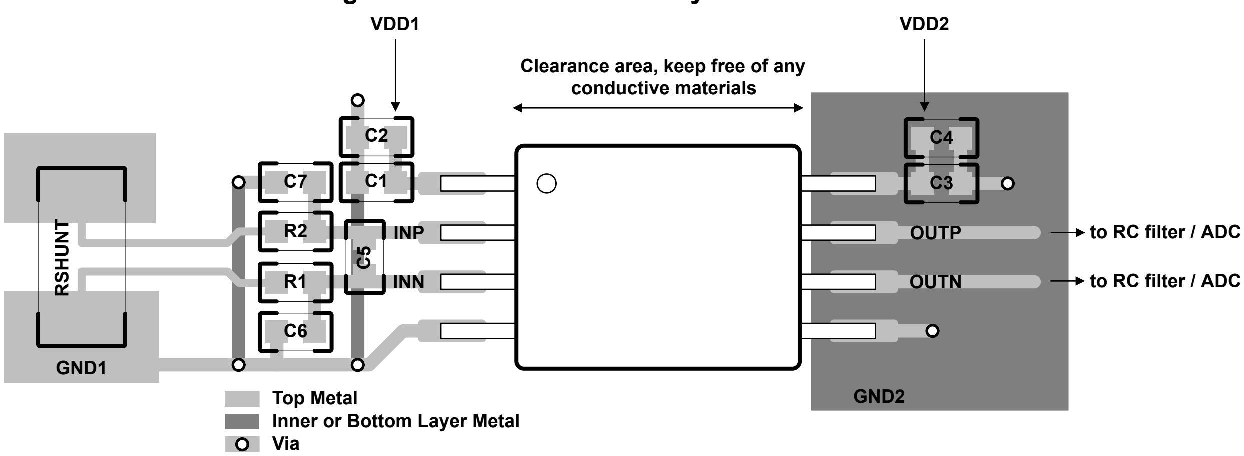
7.5 Layout

7.5.1 Layout Guidelines

The *Layout Example* section details a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC1200C supply pins). This example also depicts the placement of other components required by the device.

7.5.2 Layout Example

Figure 7-6. Recommended Layout of the AMC1200C



8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Isolation Glossary* application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application note
- Texas Instruments, *TLV900x Low-Power, RRIO, 1MHz Operational Amplifier for Cost-Sensitive Systems* data sheet
- Texas Instruments, *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* reference guide
- Texas Instruments, *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guide
- Texas Instruments, *Isolated Amplifier Voltage Sensing Excel Calculator* design tool
- Texas Instruments, *Isolated Amplifier Current Sensing Excel Calculator* design tool

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2025	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AMC1200CDUBR	Active	Production	SOP (DUB) | 8	350 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	C1200C
AMC1200CDWVR	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	C1200C

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

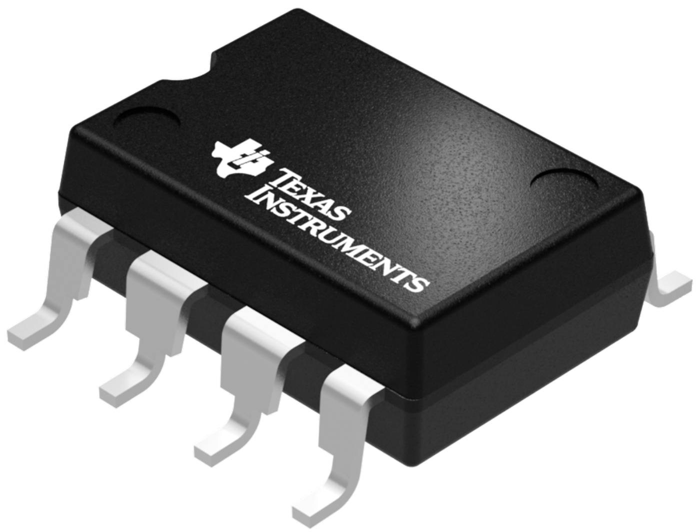
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

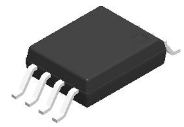
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DUB 8 SOP - 4.85 mm max height

SMALL OUTLINE PACKAGE



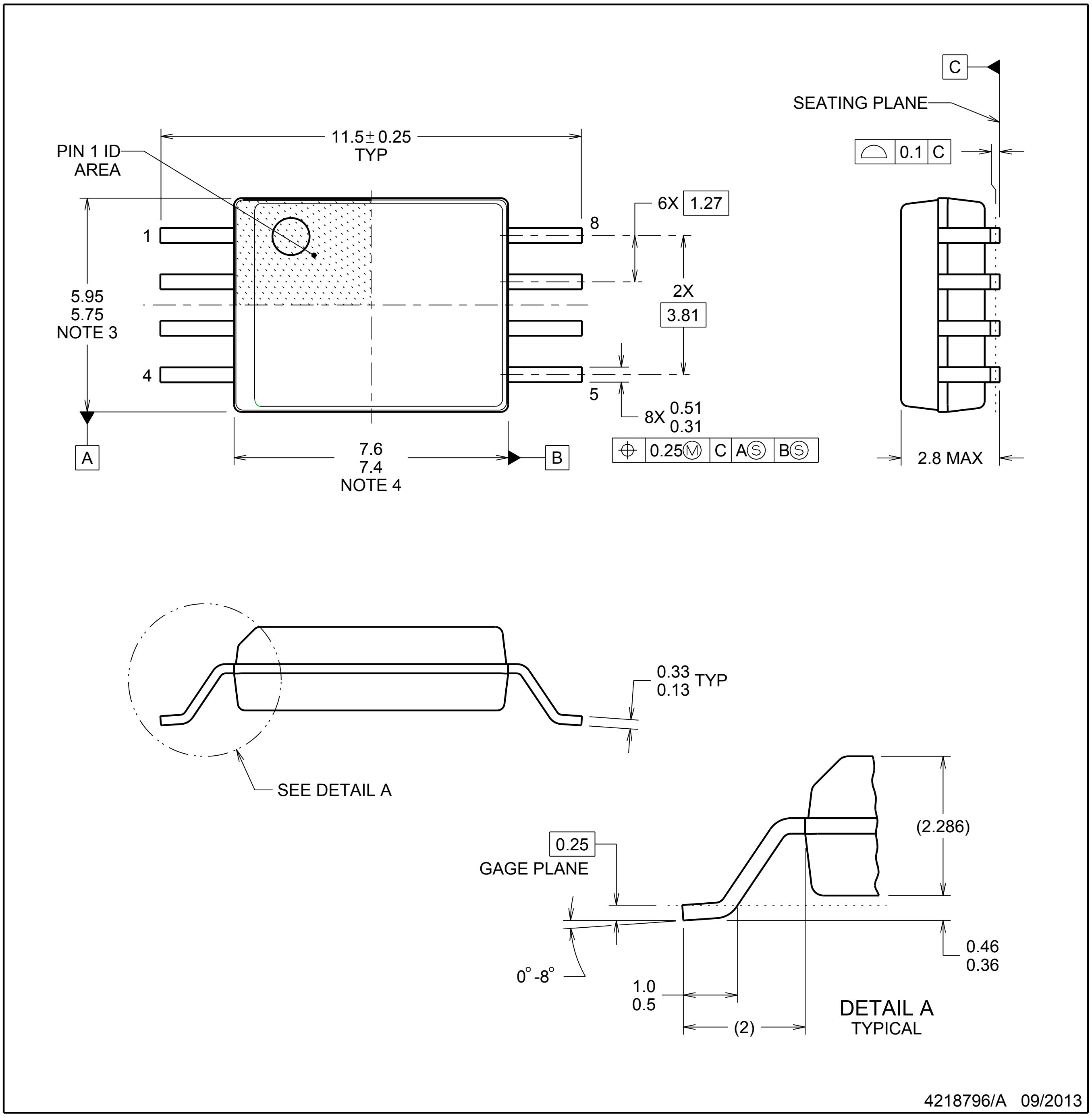
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



DWV0008A

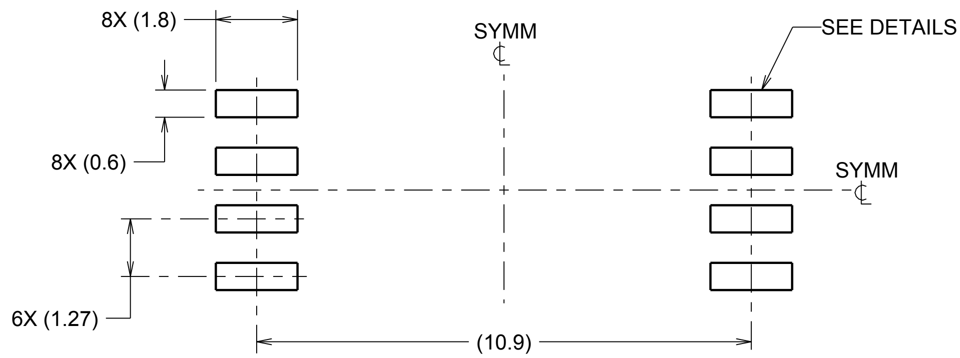
SOIC - 2.8 mm max height

SOIC

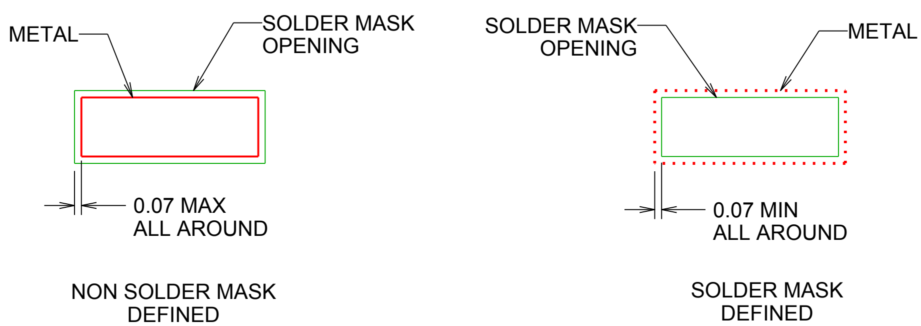


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



SOLDER MASK DETAILS

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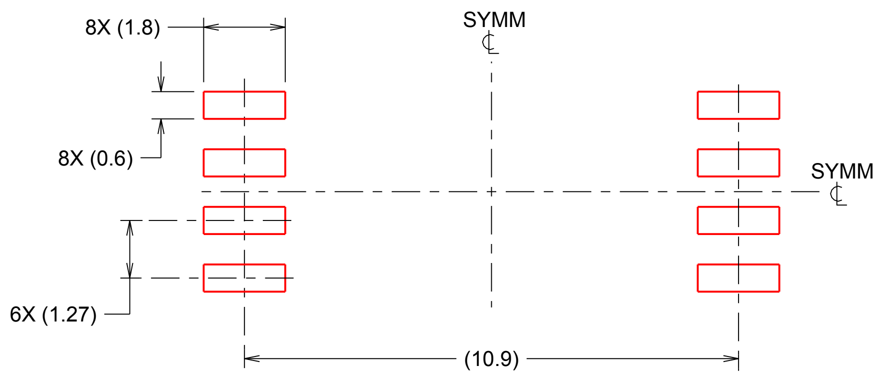
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.