

# AMC0x30R-Q1 Automotive, Precision, ±1V Input, Basic and Reinforced Isolated Amplifiers with Single-Ended, Ratiometric Output

#### 1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: -40°C to +125°C, T<sub>A</sub>
- · Linear input voltage range: ±1V
- High input impedance: 2.4GΩ (typical)
- · Supply voltage range:
  - High-side (VDD1): 3.0V to 5.5V
  - Low-side (VDD2): 3.0V to 5.5V
- Single-ended output, ratiometric to V<sub>REFIN</sub>
  - Reference Input: 2.7V to 5.5V
- · Low DC errors:
  - Offset error: ±1.5mV (maximum)
  - Offset drift: ±20µV/°C (maximum)
  - Gain error: ±0.25% (maximum)
  - Gain drift: ±40ppm/°C (maximum)
  - Nonlinearity: ±0.025% (maximum)
- High CMTI: 150V/ns (minimum)
- Low EMI: Meets CISPR-11 and CISPR-25 standards
- Isolation ratings:
  - AMC0230R-Q1: Basic isolation
  - AMC0330R-Q1: Reinforced isolation
- Safety-related certifications:
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL1577

# 2 Applications

- Traction inverters
- · Onboard chargers
- DC/DC converters

# 3 Description

The AMC0x30R-Q1 is a precision, galvanically isolated amplifier with a ±1V, high-impedance input and single-ended ratiometric output. The high-impedance input is optimized for connection to a high-impedance resistive divider or other voltage signal source with high output resistance.

The isolation barrier separates parts of the system that operate on different common-mode voltage levels. The isolation barrier is highly resistant to magnetic interference. This barrier is certified to provide reinforced isolation up to 5kV<sub>RMS</sub> (DWV package) and basic isolation up to 3kV<sub>RMS</sub> (D package) (60s).

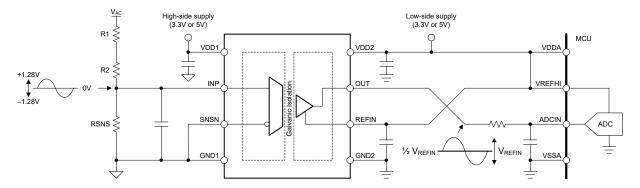
The AMC0x30R-Q1 outputs a single-ended signal proportional to the input voltage. The full-scale output is set by the voltage applied to the REFIN pin. The output of the AMC0x30R-Q1 is designed to connect directly to the input of an ADC. Connect REFIN to the same reference voltage as the ADC to match the dynamic input voltage range of the ADC.

The AMC0x30R-Q1 comes in 8-pin, wide- and narrow-body SOIC packages, and is fully specified over the temperature range from -40°C to +125°C.

# **Package Information**

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE(2)
AMC0230R-Q1 (3)	D (SOIC, 8)	4.9mm × 6mm
AMC0330R-Q1	DWV (SOIC, 8)	5.85mm × 11.5mm

- For more information, see the Mechanical, Packaging, and Orderable Information addendum.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- 3) Product Preview information (not Production Data).



**Typical Application** 



# **Table of Contents**

1 Features1	6
2 Applications1	7 D
3 Description	7.
4 Device Comparison Table3	7.
5 Pin Configuration and Functions3	7.
6 Specifications4	7.
6.1 Absolute Maximum Ratings4	8 A
6.2 ESD Ratings4	8
6.3 Recommended Operating Conditions4	8
6.4 Thermal Information (D Package)5	8
6.5 Thermal Information (DWV Package)5	8
6.6 Power Ratings5	8
6.7 Insulation Specifications (Basic Isolation)6	9 D
6.8 Insulation Specifications (Reinforced Isolation)7	9.
6.9 Safety-Related Certifications (Basic Isolation)8	9.
6.10 Safety-Related Certifications (Reinforced	9.
Isolation)8	9.
6.11 Safety Limiting Values (D Package)9	9.
6.12 Safety Limiting Values (DWV Package)9	9.
6.13 Electrical Characteristics10	10 F
6.14 Switching Characteristics11	11 N
6.15 Timing Diagram11	Ir
6.16 Insulation Characteristics Curves 12	

6.17 Typical Characteristics	. 13
Detailed Description	.15
7.1 Overview	. 15
7.2 Functional Block Diagram	. 15
7.3 Feature Description	
7.4 Device Functional Modes	19
B Application and Implementation	.20
8.1 Application Information	. 20
8.2 Typical Application	. 20
8.3 Best Design Practices	.23
8.4 Power Supply Recommendations	
8.5 Layout	. 24
Device and Documentation Support	25
9.1 Documentation Support	. 25
9.2 Receiving Notification of Documentation Updates	
9.3 Support Resources	. 25
9.4 Trademarks	. 25
9.5 Electrostatic Discharge Caution	
9.6 Glossary	
0 Revision History	. 25
1 Mechanical, Packaging, and Orderable	
Information	. 25



# **4 Device Comparison Table**

PARAMETER	AMC0230R-Q1 (1)	AMC0330R-Q1
Isolation rating per VDE 0884-17	Basic	Reinforced
Package	Narrow-body SOIC (D)	Wide-body SOIC (DWV)

<sup>(1)</sup> Product Preview information (not Production Data).

# **5 Pin Configuration and Functions**

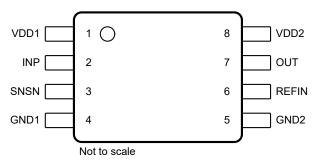


Figure 5-1. DWV and D Packages, 8-Pin SOIC (Top View)

Table 5-1. Pin Functions

	14510 0 111 1111 4110110110				
PIN		TYPE	DESCRIPTION		
NO.	NAME	1175	DESCRIPTION		
1	VDD1	High-side power	High-side power supply <sup>(1)</sup>		
2	INP	Analog input	Analog input		
3	SNSN	Analog input	GND1 sense pin and inverting analog input to the amplifier. Connect to GND1.		
4	GND1	High-side ground	High-side analog ground		
5	GND2	Low-side ground	Low-side analog ground		
6	REFIN	Analog input	The voltage applied to this pin sets the full-scale output of the device. Internally, a $90k\Omega$ resistor is connected from REFIN to GND2.		
7	OUT	Analog output	Analog output		
8	VDD2	Low-side power	Low-side power supply <sup>(1)</sup>		

<sup>(1)</sup> See the *Power Supply Recommendations* section for power-supply decoupling recommendations.



# 6 Specifications

# **6.1 Absolute Maximum Ratings**

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
D	High-side VDD1 to GND1	-0.3	6.5	V
Power-supply voltage	Low-side VDD2 to GND2	-0.3	6.5	V
Analog input voltage	INP, SNSN to GND1	GND1 – 3	VDD1 + 0.5	V
Reference input voltage	REFIN to GND2	GND2 – 0.5	VDD2 + 0.5	V
Analog output voltage	OUT to GND2	GND2 – 0.5	VDD2 + 0.5	V
Input current	Continuous, any pin except power-supply pins	-10	10	mA
Temperature	Junction, T <sub>J</sub>		150	°C
	Storage, T <sub>stg</sub>	-65	150	C

<sup>(1)</sup> Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

# 6.2 ESD Ratings

			VALUE	UNIT
,,	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup> , HBM ESD classification level 2	±2000		
V <sub>(ESD)</sub>	Electrostatic discharge	Charged-device model (CDM), per AEC Q100-011, CDM ESD classification level C6	±1000	V

<sup>(1)</sup> AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

# **6.3 Recommended Operating Conditions**

over operating ambient temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
SUPPLY		•			
High-side power supply	VDD1 to GND1	3	5.0	5.5	V
Low-side power supply	VDD2 to GND2	3	3.3	5.5	V
INPUT		•			
Nominal input voltage before clipping output	$V_{IN} = V_{INP} - V_{SNSN}$	-1.28		1.28	V
Specified linear input voltage	V <sub>IN</sub> = V <sub>INP</sub> - V <sub>SNSN</sub>	-1		1	V
Reference input voltage	REFIN to GND2	2.7		VDD2	V
OUTPUT	·	•			
Capacitive load	OUT to GND2			500	pF
Resistive load	OUT to GND2		10	1	kΩ
ATURE RANGE		•			
Specified ambient temperature		-40		125	°C
	High-side power supply  Low-side power supply  INPUT  Nominal input voltage before clipping output  Specified linear input voltage  Reference input voltage  OUTPUT  Capacitive load  Resistive load  ATURE RANGE	High-side power supply  Low-side power supply  VDD2 to GND2  INPUT  Nominal input voltage before clipping output  V <sub>IN</sub> = V <sub>INP</sub> - V <sub>SNSN</sub> Specified linear input voltage  V <sub>IN</sub> = V <sub>INP</sub> - V <sub>SNSN</sub> Reference input voltage  REFIN to GND2  OUTPUT  Capacitive load  OUT to GND2  ATURE RANGE	High-side power supply   VDD1 to GND1   3	High-side power supply   VDD1 to GND1   3   5.0	High-side power supply   VDD1 to GND1   3   5.0   5.5     Low-side power supply   VDD2 to GND2   3   3.3   5.5     INPUT     Nominal input voltage before clipping output   V <sub>IN</sub> = V <sub>INP</sub> - V <sub>SNSN</sub>   -1.28   1.28     Specified linear input voltage   V <sub>IN</sub> = V <sub>INP</sub> - V <sub>SNSN</sub>   -1   1     Reference input voltage   REFIN to GND2   2.7   VDD2     OUTPUT     Capacitive load   OUT to GND2   500     Resistive load   OUT to GND2   10   1     ATURE RANGE



# 6.4 Thermal Information (D Package)

	THERMAL METRIC(1)	D (SOIC)	LINIT
	I TERMAL METRIC	8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.5	°C/W
R <sub>0JC(top)</sub>	Junction-to-case (top) thermal resistance	52.8	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	58.9	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	19.4	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	58.0	°C/W
R <sub>0JC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	°C/W

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

# 6.5 Thermal Information (DWV Package)

	THERMAL METRIC(1)	DWV (SOIC)	LINUT
	THERMAL METRIC	8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102.8	°C/W
R <sub>0</sub> JC(top)	Junction-to-case (top) thermal resistance	45.1	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	63.0	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	14.3	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	61.1	°C/W
R <sub>0JC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	°C/W

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

# 6.6 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P <sub>D</sub>	Maximum power dissipation (both sides)	VDD1 = VDD2 = 5.5V	72	mW
P <sub>D1</sub>	Maximum power dissipation (high-side)	VDD1 = 5.5V	31	mW
P <sub>D2</sub>	Maximum power dissipation (low-side)	VDD2 = 5.5V	41	mW



## 6.7 Insulation Specifications (Basic Isolation)

over operating ambient temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	VALUE	UNIT
GENER	AL			
CLR	External clearance <sup>(1)</sup>	Shortest pin-to-pin distance through air	≥ 4	mm
CPG	External creepage <sup>(1)</sup>	Shortest pin-to-pin distance across the package surface	≥ 4	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the insulation	≥ 15.4	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	1	
	Overvoltage category	Rated mains voltage ≤ 300V <sub>RMS</sub>	I-IV	
	per IEC 60664-1	Rated mains voltage ≤ 600V <sub>RMS</sub>	1-111	
DIN EN	IEC 60747-17 (VDE 0884-17)(2)		1	
V <sub>IORM</sub>	Maximum repetitive peak isolation voltage	At AC voltage	1130	V <sub>PK</sub>
\ /	Maximum-rated isolation	At AC voltage (sine wave)	800	V <sub>RMS</sub>
$V_{IOWM}$	working voltage	At DC voltage	1130	$V_{DC}$
V <sub>IOTM</sub>	Maximum transient isolation voltage	V <sub>TEST</sub> = V <sub>IOTM</sub> , t = 60s (qualification test), V <sub>TEST</sub> = 1.2 × V <sub>IOTM</sub> , t = 1s (100% production test)	4250	V <sub>PK</sub>
V <sub>IMP</sub>	Maximum impulse voltage <sup>(3)</sup>	Tested in air, 1.2/50µs waveform per IEC 62368-1	5000	V <sub>PK</sub>
V <sub>IOSM</sub>	Maximum surge isolation voltage <sup>(4)</sup>	Tested in oil (qualification test), 1.2/50µs waveform per IEC 62368-1	10000	V <sub>PK</sub>
		Method a, after input/output safety test subgroups 2 and 3, $V_{pd(ini)} = V_{IOTM}$ , $t_{ini} = 60s$ , $V_{pd(m)} = 1.2 \times V_{IORM}$ , $t_m = 10s$	≤ 5	
~	Apparent shares (5)	Method a, after environmental tests subgroup 1, $V_{pd(ini)} = V_{IOTM}$ , $t_{ini} = 60s$ , $V_{pd(m)} = 1.3 \times V_{IORM}$ , $t_m = 10s$	≤ 5	
q <sub>pd</sub>	Apparent charge <sup>(5)</sup>	Method b1, at preconditioning (type test) and routine test, $V_{pd(ini)} = V_{IOTM}$ , $t_{ini} = 1s$ , $V_{pd(m)} = 1.5 \times V_{IORM}$ , $t_m = 1s$	≤ 5	— pC
		Method b2, at routine test (100% production) <sup>(7)</sup> , $V_{pd(ini)} = V_{IOTM} = V_{pd(m)}$ , $t_{ini} = t_m = 1s$	≤ 5	
C <sub>IO</sub>	Barrier capacitance, input to output <sup>(6)</sup>	$V_{IO} = 0.5V_{PP}$ at 1MHz	≅1.5	pF
		V <sub>IO</sub> = 500V at T <sub>A</sub> = 25°C	> 10 <sup>12</sup>	
R <sub>IO</sub>	Insulation resistance, input to output <sup>(6)</sup>	V <sub>IO</sub> = 500V at 100°C ≤ T <sub>A</sub> ≤ 125°C	> 10 <sup>11</sup>	Ω
	input to output(*/	V <sub>IO</sub> = 500V at T <sub>S</sub> = 150°C	> 10 <sup>9</sup>	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577	<u>'</u>	-		
V <sub>ISO</sub>	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ , t = 60s (qualification test), $V_{TEST} = 1.2 \times V_{ISO}$ , t = 1s (100% production test)	3000	V <sub>RMS</sub>

- (1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Maintain the creepage and clearance distance of a board design to make sure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air to determine the surge immunity of the package.
- (4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
- (5) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (6) All pins on each side of the barrier are tied together, creating a two-pin device.
- (7) Either method b1 or b2 is used in production.



# 6.8 Insulation Specifications (Reinforced Isolation)

over operating ambient temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	VALUE	UNIT
GENER	AL			
CLR	External clearance <sup>(1)</sup>	Shortest pin-to-pin distance through air	≥ 8.5	mm
CPG	External creepage <sup>(1)</sup>	Shortest pin-to-pin distance across the package surface	≥ 8.5	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation	≥ 15.4	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	1	
	Overvoltage category	Rated mains voltage ≤ 300V <sub>RMS</sub>	I-IV	
	per IEC 60664-1	Rated mains voltage ≤ 6000V <sub>RMS</sub>	1-111	
DIN EN	IEC 60747-17 (VDE 0884-17)(2)			
V <sub>IORM</sub>	Maximum repetitive peak isolation voltage	At AC voltage	2120	V <sub>PK</sub>
V	Maximum-rated isolation	At AC voltage (sine wave)	1500	V <sub>RMS</sub>
$V_{IOWM}$	working voltage	At DC voltage	2120	V <sub>DC</sub>
$V_{IOTM}$	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$ , t = 60s (qualification test), $V_{TEST} = 1.2 \times V_{IOTM}$ , t = 1s (100% production test)	7000	V <sub>PK</sub>
V <sub>IMP</sub>	Maximum impulse voltage <sup>(3)</sup>	Tested in air, 1.2/50µs waveform per IEC 62368-1	7700	V <sub>PK</sub>
V <sub>IOSM</sub>	Maximum surge isolation voltage <sup>(4)</sup>	Tested in oil (qualification test), 1.2/50µs waveform per IEC 62368-1	10000	V <sub>PK</sub>
		Method a, after input/output safety test subgroups 2 and 3, $V_{pd(ini)} = V_{IOTM}, t_{ini} = 60s, V_{pd(m)} = 1.2 \times V_{IORM}, t_m = 10s$	≤ 5	
<b>a</b>	Apparent charge <sup>(5)</sup>	Method a, after environmental tests subgroup 1, $V_{pd(ini)} = V_{IOTM}$ , $t_{ini} = 60s$ , $V_{pd(m)} = 1.6 \times V_{IORM}$ , $t_m = 10s$	≤ 5	200
q <sub>pd</sub>	Apparent charge	Method b1, at preconditioning (type test) and routine test, $V_{pd(ini)} = 1.2 \times V_{IOTM}$ , $t_{ini} = 1$ s, $V_{pd(m)} = 1.875 \times V_{IORM}$ , $t_m = 1$ s	≤ 5	pC
		Method b2, at routine test (100% production) <sup>(7)</sup> $V_{pd(ini)} = V_{pd(m)} = 1.2 \times V_{IOTM}, t_{ini} = t_m = 1s$	≤ 5	
C <sub>IO</sub>	Barrier capacitance, input to output <sup>(6)</sup>	V <sub>IO</sub> = 0.5V <sub>PP</sub> at 1MHz	<b>≅1.5</b>	pF
		V <sub>IO</sub> = 500V at T <sub>A</sub> = 25°C	> 10 <sup>12</sup>	
R <sub>IO</sub>	Insulation resistance, input to output <sup>(6)</sup>	V <sub>IO</sub> = 500V at 100°C ≤ T <sub>A</sub> ≤ 125°C	> 10 <sup>11</sup>	Ω
		V <sub>IO</sub> = 500V at T <sub>S</sub> = 150°C	> 10 <sup>9</sup>	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				,
V <sub>ISO</sub>	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ , t = 60s (qualification test), $V_{TEST} = 1.2 \times V_{ISO}$ , t = 1s (100% production test)	5000	V <sub>RMS</sub>

<sup>(1)</sup> Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Maintain the creepage and clearance distance of a board design to make sure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.

- (3) Testing is carried out in air to determine the surge immunity of the package.
- (4) Testing is carried in oil to determine the intrinsic surge immunity of the isolation barrier.
- (5) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (6) All pins on each side of the barrier are tied together, creating a two-pin device.
- (7) Either method b1 or b2 is used in production.

<sup>(2)</sup> This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.



# 6.9 Safety-Related Certifications (Basic Isolation)

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN 61010-1 (VDE 0411-1) Clause : 6.4.3 ; 6.7.1.3 ; 6.7.2.1 ; 6.7.2.2 ; 6.7.3.4.2 ; 6.8.3.1	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Basic insulation	Single protection
Certificate number: Pending	File number: Pending

# 6.10 Safety-Related Certifications (Reinforced Isolation)

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN IEC 62368-1 (VDE 0868-1), EN IEC 62368-1, IEC 62368-1 Clause : 5.4.3 ; 5.4.4.4 ; 5.4.9	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
Certificate number: Pending	File number: Pending



## 6.11 Safety Limiting Values (D Package)

Safety limiting<sup>(1)</sup> intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>S</sub>	Safety input, output, or supply current	$R_{\theta JA} = 116.5^{\circ}C/W$ , VDDx = 5.5V, $T_J = 150^{\circ}C$ , $T_A = 25^{\circ}C$			195	mA
Ps	Safety input, output, or total power	$R_{\theta JA} = 116.5$ °C/W, $T_J = 150$ °C, $T_A = 25$ °C			1070	mW
T <sub>S</sub>	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T<sub>S</sub>, has the same value as the maximum junction temperature, T<sub>J</sub>, specified for the device. The I<sub>S</sub> and P<sub>S</sub> parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I<sub>S</sub> and P<sub>S</sub>. These limits vary with the ambient temperature, T<sub>A</sub>.

The junction-to-air thermal resistance,  $R_{\theta JA}$ , in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

 $T_J = T_A + R_{\theta JA} \times P$ , where P is the power dissipated in the device.

 $T_{J(max)}$  =  $T_S$  =  $T_A$  +  $R_{\theta JA}$  ×  $P_S$ , where  $T_{J(max)}$  is the maximum junction temperature.

 $P_S = I_S \times VDD_{max}$ , where  $VDD_{max}$  is the maximum supply voltage for high-side and low-side.

## 6.12 Safety Limiting Values (DWV Package)

Safety limiting<sup>(1)</sup> intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Is	Safety input, output, or supply current	R <sub>θJA</sub> = 102.8°C/W, VDDx = 5.5V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			220	mA
Ps	Safety input, output, or total power	$R_{\theta JA} = 102.8^{\circ}C/W, T_J = 150^{\circ}C, T_A = 25^{\circ}C$			1210	mW
Ts	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T<sub>S</sub>, has the same value as the maximum junction temperature, T<sub>J</sub>, specified for the device. The I<sub>S</sub> and P<sub>S</sub> parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I<sub>S</sub> and P<sub>S</sub>. These limits vary with the ambient temperature, T<sub>A</sub>.

The junction-to-air thermal resistance,  $R_{\theta JA}$ , in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

 $T_J = T_A + R_{\theta JA} \times P$ , where P is the power dissipated in the device.

 $T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$ , where  $T_{J(max)}$  is the maximum junction temperature.

 $P_S = I_S \times VDD_{max}$ , where  $VDD_{max}$  is the maximum supply voltage for high-side and low-side.



#### **6.13 Electrical Characteristics**

minimum and maximum specifications apply from  $T_A = -40^{\circ}\text{C}$  to +125°C, VDD1 = 3.0V to 5.5V, VDD2 = 3.0V to 5.5V, VREFIN = 3.3V, SNSN = GND1,  $V_{INP} = -1\text{V}$  to 1V (unless otherwise noted); typical specifications are at  $T_A = 25^{\circ}\text{C}$ , VDD1 = 5V, and VDD2 = 3.3V

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG	INPUT					
C <sub>IN</sub>	Input capacitance			2		pF
R <sub>INP</sub>	Input impedance	INP pin, T <sub>A</sub> = 25°C	0.05	2.4		GΩ
I <sub>IB</sub>	Input bias current	INP = GND1, T <sub>A</sub> = 25°C	-10	±3	10	nA
CMTI	Common-mode transient immunity		150			V/ns
ANALOG	OUTPUT					
	Nominal gain			V <sub>REFIN</sub> / 2 /  V <sub>Clipping</sub>		V/V
R <sub>OUT</sub>	Output resistance	OUTP or OUTN		<0.2		Ω
	Output short-circuit current	sourcing or sinking, INP = GND1, output shorted to either GND or VDD2		11		mA
DC ACCU	IRACY					
V <sub>OS</sub>	Input offset voltage <sup>(1) (2)</sup>	INP = GND1, VDD2 = 3.3V, V <sub>REFIN</sub> = 3.3V, T <sub>A</sub> = 25°C	-1.5	±0.1	1.5	mV
TCV <sub>OS</sub>	Input offset thermal drift <sup>(1)</sup> (2) (4)		-20	±2	20	μV/°C
E <sub>G</sub>	Gain error <sup>(1)</sup>	T <sub>A</sub> = 25°C	-0.25%	±0.04%	0.25%	
TCE <sub>G</sub>	Gain error drift <sup>(1) (5)</sup>		-40	±5	40	ppm/°C
	Nonlinearity <sup>(1)</sup>		-0.025%	±0.01%	0.025%	
	Output noise	INP = GND1, BW = 50kHz		160		μVrms
	Power-supply rejection ratio <sup>(2)</sup>	VDD1 DC PSRR, INP = GND1, VDD1 from 3V to 5.5V		<b>–77</b>		
PSRR		VDD1 AC PSRR, INP = GND1, VDD1 with 10kHz / 100mV ripple		-60		dB
FORK		VDD2 DC PSRR, INP = GND1, VDD2 from 3V to 5.5V		-100		uБ
		VDD2 AC PSRR, INP = GND1, VDD2 with 10kHz / 100mV ripple		-74		
AC ACCU	IRACY					
BW	Output bandwidth		120	145		kHz
THD	Total harmonic distortion <sup>(3)</sup>	$V_{INP} = 2V_{PP}, V_{INP} > 0V,$ $f_{INP} = 10kHz, BW = 100kHz$		-80	<b>–</b> 75	dB
		$V_{INP} = 2.25V_{PP}$ , $f_{INP} = 1kHz$ , BW = $10kHz$	78	82		
SNR	Signal-to-noise ratio	$V_{INP}$ = 2.25 $V_{PP}$ , $f_{INP}$ = 10kHz, BW = 50kHz		75		dB
POWER S	SUPPLY					
I <sub>DD1</sub>	High-side supply current			4.3	5.6	mA
I <sub>DD2</sub>	Low-side supply current			4.8	7.4	mA
VDD4	High-side undervoltage detection	VDD1 rising	2.4	2.6	2.8	V
VDD1 <sub>UV</sub>	threshold	VDD1 falling	1.9	2.05	2.2	V
VDD2	Low-side undervoltage detection	VDD2 rising	2.3	2.5	2.7	V
VDD2 <sub>UV</sub>	threshold	VDD2 falling	1.9	2.05	2.2	V

- (1) The typical value includes one standard deviation (*sigma*) at nominal operating conditions.
- (2) This parameter is input referred.
- (3) THD is the ratio of the rms sum of the amplitudes of first five higher harmonics to the amplitude of the fundamental.
- (4) Offset error temperature drift is calculated using the box method, as described by the following equation:

 $TCV_{OS} = (Value_{MAX} - Value_{MIN}) / TempRange$ 

Gain error temperature drift is calculated using the box method, as described by the following equation:  $TCE_G(ppm) = (Value_{MAX} - Value_{MIN}) / (Value_{(T=25)^c)} \times TempRange) \times 10^6$ 

# **6.14 Switching Characteristics**

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>r</sub>	Output signal rise time	10% to 90%, unfiltered output		2.6		μs
t <sub>f</sub>	Output signal fall time	10% to 90%, unfiltered output		2.6		μs
	V <sub>INP</sub> to V <sub>OUT</sub> signal delay (50% – 10%)	Unfiltered output		1.6		μs
	V <sub>INP</sub> to V <sub>OUT</sub> signal delay (50% – 50%)	Unfiltered output		2.9	3.2	μs
	V <sub>INP</sub> to V <sub>OUT</sub> signal delay (50% – 90%)	Unfiltered output		4.3		μs
t <sub>AS</sub>	Analog settling time	VDD1 step to 3.0V with VDD2 $\geq$ 3.0V to $V_{OUT}$ valid, 0.1% settling		20	100	μs

# **6.15 Timing Diagram**

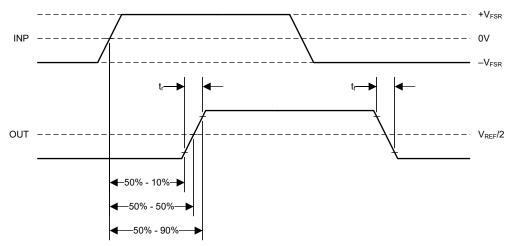
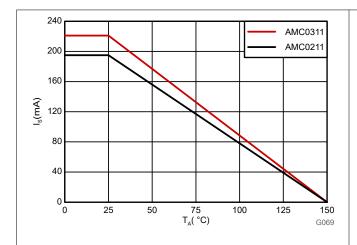


Figure 6-1. Rise, Fall, and Delay Time Definition

#### **6.16 Insulation Characteristics Curves**



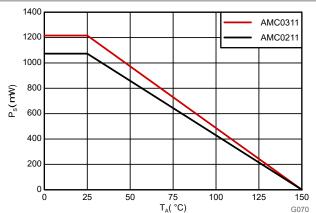
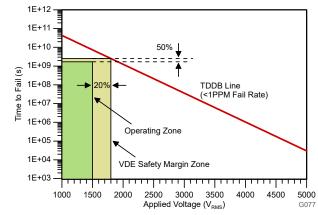
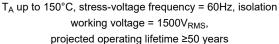
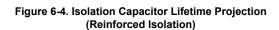


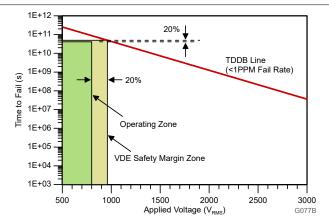
Figure 6-2. Thermal Derating Curve for Safety-Limiting Current per VDE

Figure 6-3. Thermal Derating Curve for Safety-Limiting Power per VDE









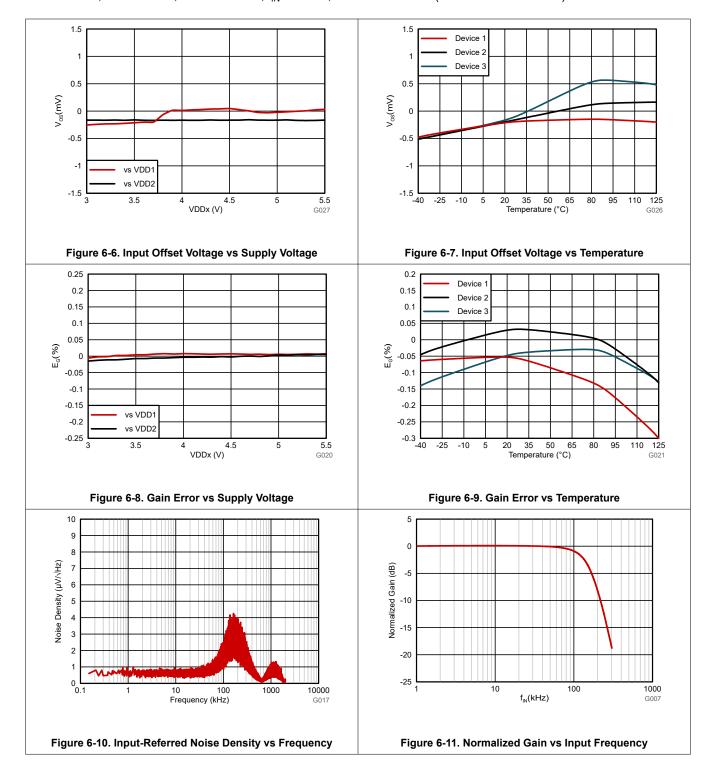
T<sub>A</sub> up to 150°C, stress-voltage frequency = 60Hz, isolation working voltage = 800V<sub>RMS</sub>, projected operating lifetime >>100 years

Figure 6-5. Isolation Capacitor Lifetime Projection (Basic Isolation)



## **6.17 Typical Characteristics**

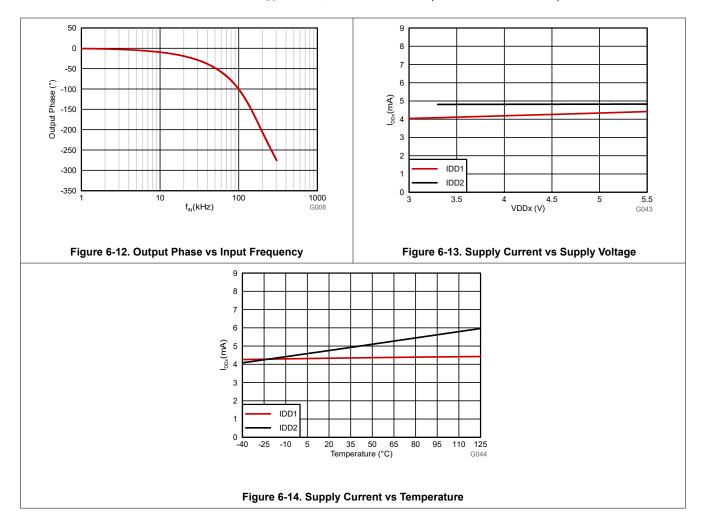
at VDD1 = 5V, VDD2 = 3.3V, SNSN = GND1, f<sub>IN</sub> = 10kHz, and BW = 100kHz (unless otherwise noted)





# **6.17 Typical Characteristics (continued)**

at VDD1 = 5V, VDD2 = 3.3V, SNSN = GND1, f<sub>IN</sub> = 10kHz, and BW = 100kHz (unless otherwise noted)





# 7 Detailed Description

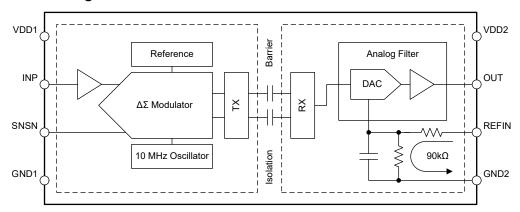
#### 7.1 Overview

The AMC0x30R-Q1 is a precision, galvanically isolated amplifier with a  $\pm 1V$ , high-impedance input and single-ended ratiometric output. The input stage of the device drives a second-order, delta-sigma ( $\Delta\Sigma$ ) modulator. The modulator converts the analog input signal into a digital bitstream that is transferred across the isolation barrier that separates the high-side from the low-side.

On the low-side, the received bitstream is processed by an analog filter that outputs a GND2-referenced, single-ended signal at the OUT pin. This single-ended output signal is proportional to the input signal. The full-scale output voltage of the isolated amplifier is equal to the voltage applied to the REFIN pin.

The SiO<sub>2</sub>-based, capacitive isolation barrier supports a high level of magnetic field immunity, as described in the *ISO72x Digital Isolator Magnetic-Field Immunity* application note. The digital modulation used in the AMC0x30R-Q1 transmits data across the isolation barrier. This modulation, and the isolation barrier characteristics, result in high reliability and high common-mode transient immunity.

## 7.2 Functional Block Diagram



#### 7.3 Feature Description

#### 7.3.1 Analog Input

The high-impedance input buffer on the INP pin feeds a second-order, switched-capacitor, feed-forward  $\Delta\Sigma$  modulator. The modulator converts the analog signal into a bitstream that is transferred across the isolation barrier, as described in the *Isolation Channel Signal Transmission* section.

There are two restrictions on the analog input signal. First, if the input voltage exceeds the value specified in the *Absolute Maximum Ratings* table, the input current must be limited to 10mA. This limitation is caused by the device input electrostatic discharge (ESD) diodes turning on. Second, linearity and noise performance are specified only when the input voltage is within the linear full-scale range (V<sub>FSR</sub>). V<sub>FSR</sub> is specified in the *Recommended Operating Conditions* table.

# 7.3.2 Isolation Channel Signal Transmission

As shown in Figure 7-1, the AMC0x30R-Q1 uses an on-off keying (OOK) modulation scheme to transmit the modulator output bitstream across the  $SiO_2$ -based isolation barrier. The transmit driver (TX) is illustrated in the *Functional Block Diagram*. TX transmits an internally generated, high-frequency carrier across the isolation barrier to represent a digital *one*. However, TX does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC0x30R-Q1 is 480MHz.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and provides the input to the analog filter. The AMC0x30R-Q1 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and the lowest level of radiated emissions. The high-frequency carrier and RX/TX buffer switching cause these emissions.

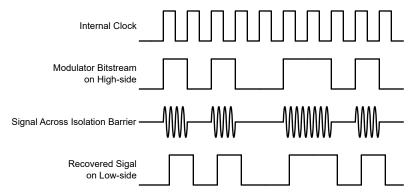


Figure 7-1. OOK-Based Modulation Scheme



# 7.3.3 Analog Output

The AMC0x30R-Q1 provides a single-ended analog output voltage proportional to the input voltage. The output is referred to GND2 and is galvanically isolated from the input of the device. The output is designed to connect directly to the input of an ADC.

The full-scale output voltage is set by the REFIN pin. For any input voltage within the specified linear input range, the device outputs a voltage equal to:

$$V_{OUT} = V_{IN} / V_{Clipping} \times V_{REFIN} / 2 + V_{REFIN} / 2 = (V_{INP} - V_{SNSN}) / V_{Clipping} \times V_{REFIN} / 2 + V_{REFIN} / 2$$
(1)

Connect REFIN to the same reference voltage as a downstream ADC to match the ADC dynamic input voltage range. With a shared reference voltage, the ADC outputs a negative full-scale code when the negative clipping voltage is applied to the input of the AMC0x30R-Q1. The ADC outputs the mid-range code when 0V is applied to the input of the AMC0x30R-Q1. The ADC outputs a positive full-scale code when the positive clipping voltage is applied to the input of the AMC0x30R-Q1.

The device is linear within the specified linear full-scale range. Beyond the linear full-scale range, the output continues to follow the input, but with reduced linearity performance. The output clips when the input voltage reaches the clipping voltage. Figure 7-2 shows the input-to-output transfer characteristic.

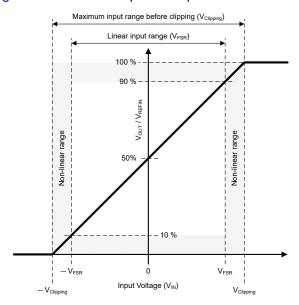


Figure 7-2. Input-to-Output Transfer Curve of the AMC0x30R-Q1

#### 7.3.4 Reference Input

The voltage applied to the REFIN pin determines the output voltage range of the OUT pin, as described in the *Analog Output* section.

The output buffer is linear in the range of  $250 \text{mV} < V_{\text{OUT}} < (\text{VDD2} - 250 \text{mV})$ . Outside this range, the output continues to follow the input, but with reduced linearity performance. Eventually the output voltage clips, because the output buffer requires a minimum headroom to GND2 and VDD2. The input-referred linear range that the output buffer supports is a function of  $V_{\text{REFIN}}$  and is calculated as follows:

$$V_{IN, MIN} = (2 \times V_{OUT, MIN} / V_{REFIN} - 1) \times V_{Clipping, MIN}$$
(2)

$$V_{IN, MAX} = (2 \times V_{OUT, MAX} / V_{REFIN} - 1) \times V_{Clipping, MAX}$$
(3)

For a worst-case calculation, set  $V_{OUT, MIN} = 250 \text{mV}$ ,  $V_{OUT, MAX} = VDD2_{MIN} - 250 \text{mV} = 2.75 \text{V}$ , and  $V_{REFIN} \ge 2.7 \text{V}$ . Under these worst-case assumptions, the output buffer supports an input voltage range from -1.04 V to 1.33 V. This range is larger than the specified linear input voltage range of the device. Therefore, the reference voltage is not a limiting item.



#### 7.4 Device Functional Modes

The AMC0x30R-Q1 operates in one of the following states:

- Off-state: The low-side supply (VDD2) is below the VDD2<sub>UV</sub> threshold. The device is not responsive. OUT is in Hi-Z state. Internally, OUT is clamped to VDD2 and GND2 by ESD protection diodes.
- Missing high-side supply: The low-side of the device (VDD2) is supplied and within recommended operating
  conditions. The high-side supply (VDD1) is below the VDD1<sub>UV</sub> threshold. The OUT pin is driven to V<sub>REFIN</sub> / 2.
- Analog input overrange (positive full-scale input): VDD1 and VDD2 are within recommended operating
  conditions but the analog input voltage V<sub>IN</sub> is above the maximum clipping voltage V<sub>Clipping, MAX</sub>. The device
  outputs V<sub>REFIN</sub> at the OUT pin.
- Analog input underrange (negative full-scale input): VDD1 and VDD2 are within recommended operating
  conditions but the analog input voltage V<sub>IN</sub> is below the minimum clipping voltage V<sub>Clipping, MIN</sub>. The OUT pin
  is driven to GND2.
- Normal operation: VDD1, VDD2, and V<sub>IN</sub> are within the recommended operating conditions. The device
  outputs a voltage that is proportional to the input voltage.

Table 7-1 lists the operating modes.

Table 7-1. Device Operational Modes

OPERATING CONDITION	VDD1	VDD2	V <sub>IN</sub>	DEVICE RESPONSE
Off	Don't care	VDD2 < VDD2 <sub>UV</sub>	Don't care	OUT is in Hi-Z state. Internally, OUT is clamped to VDD2 and GND2 by ESD protection diodes.
Missing high-side supply	VDD1 < VDD1 <sub>UV</sub>	Valid <sup>(1)</sup>	Don't care	The OUT pin is driven to V <sub>REFIN</sub> / 2.
Input overrange	Valid <sup>(1)</sup>	Valid <sup>(1)</sup>	V <sub>IN</sub> > V <sub>Clipping, MAX</sub>	The device outputs $V_{REFIN}$ at the OUT pin.
Input underrange	Valid <sup>(1)</sup>	Valid <sup>(1)</sup>	V <sub>IN</sub> < V <sub>Clipping, MIN</sub>	The OUT pin is driven to GND2.
Normal operation	Valid <sup>(1)</sup>	Valid <sup>(1)</sup>	Valid <sup>(1)</sup>	The device outputs a voltage that is proportional to the input voltage.

<sup>(1)</sup> Valid denotes operation within the recommended operating conditions.



# 8 Application and Implementation

#### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

# 8.1 Application Information

AC powered systems such as onboard chargers (OBC) are divided into two or more voltage domains that are galvanically isolated from each other. For example, one high-voltage domain includes the AC grid, DC link, and the power stage for power-factor correction (PFC). A second high-voltage domain contains the DC bus and high-voltage battery. The PFC controller is referenced to DC link (–) and measures the value of the AC line voltage while remaining galvanically isolated from the AC mains for functional reasons. With the high-impedance input and galvanically isolated output, the AMC0x30R-Q1 enables this measurement.

# 8.2 Typical Application

illustrates a simplified schematic of a circuit that senses the line voltages of a three-phase AC system. All three voltages are measured against neutral. This configuration allows the three AMC0x30R-Q1 devices to share a common isolated power supply on the input side.

The AC line voltage on phase L1 is divided down to a ±1V level across the bottom resistor (RSNS) of a high-impedance resistive divider. The voltage across RSNS is sensed by the AMC0x30R-Q1 (*device 1*). On the opposite side of the isolation barrier *device 1* outputs a voltage proportional to the L1-to-neutral voltage. In the same way, *device 2* and *device 3* sense the L2 and L3 line voltages, respectively. A common VDD1 supply is generated from the low-voltage side by an isolated DC/DC converter circuit. A low-cost design is based on the push-pull driver SN6501-Q1 and a transformer that supports the desired isolation voltage ratings.

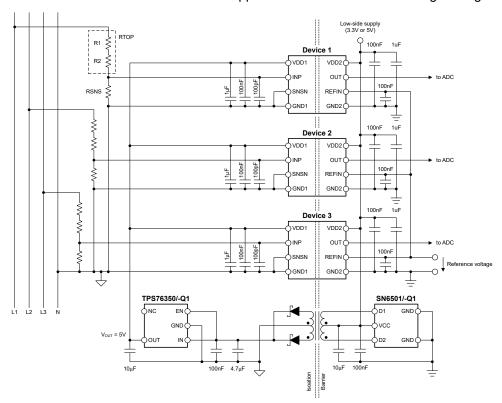


Figure 8-1. Using the AMC0x30R-Q1 in a Typical Application



#### 8.2.1 Design Requirements

Table 8-1 lists the parameters for this typical application.

Table 8-1. Design Requirements

PARAMETER	VALUE
System input voltage (phase to neutral)	230V <sub>RMS</sub> ±10%, 50Hz
High-side supply voltage	5V
Low-side supply voltage	3.3V
Maximum resistor operating voltage	125V
Voltage drop across the sense resistor (RSNS) for a linear response	±1V (maximum)
Current through the resistive divider, I <sub>CROSS</sub>	200μA (maximum)

## 8.2.2 Detailed Design Procedure

The peak input voltage is  $230\text{V} \times \sqrt{2} \times 1.1 = 360\text{V}$ . The  $200\mu\text{A}$  maximum cross-current requirement determines that the total impedance of the resistive divider is  $1.8M\Omega$ . The impedance of the resistive divider is dominated by the top resistors, shown exemplary as R1 and R2 in Figure 1-1 . The maximum allowed voltage drop per unit resistor is specified as 125V. Therefore, the minimum number of unit resistors in the top portion of the resistive divider is  $360\text{V} / 125\text{V} \cong 3$ . The calculated unit value is  $1.8M\Omega / 3 = 600\text{k}\Omega$  and the next closest value from the E96 series is  $604\text{k}\Omega$ .

Size RSNS such that the voltage drop at the maximum input voltage (360V) equals  $V_{FSR}$ .  $V_{FSR}$  is the linear full-scale voltage and specified as ±1V. RSNS is calculated as RSNS =  $V_{FSR}$  / ( $V_{Peak} - V_{FSR}$ ) ×  $R_{TOP}$ .  $R_{TOP}$  is the total value of the top resistor string (3 × 604k $\Omega$  = 1.812M $\Omega$ ). RSNS results in a value of 5.05k $\Omega$ . The next closest value from the E96 series is 4.99k $\Omega$ .

Table 8-2 summarizes the design of the resistive divider.

**Table 8-2. Resistor Value Examples** 

PARAMETER	VALUE
Unit resistor value, R <sub>TOP</sub>	604kΩ
Number of unit resistors in R <sub>TOP</sub>	3
Sense resistor value, RSNS	4.99kΩ
Total resistance value (R <sub>TOP</sub> + RSNS)	1.817ΜΩ
Resulting current through resistive divider, I <sub>CROSS</sub>	198.1μΑ
Resulting full-scale voltage drop across sense resistor RSNS	989mV
Peak power dissipated in R <sub>TOP</sub> unit resistor	23.7mW
Total peak power dissipated in resistive divider	71.3mW

#### 8.2.2.1 Input Filter Design

Place an RC filter in front of the device to improve signal-to-noise performance of the signal path. Input noise with a frequency close to the  $\Delta\Sigma$  modulator sampling frequency (typically 10MHz) is folded back into the low-frequency range by the modulator. The purpose of the RC filter is to attenuate high-frequency noise below the desired noise level of the measurement. In practice, a cutoff frequency that is two orders of magnitude lower than the modulator frequency yields good results.

Most voltage-sensing applications use high-impedance resistive dividers to scale down the input voltage. In this case, a single capacitor, as shown in Figure 8-2, is sufficient to filter the input signal. For (R1 + R2) >> RSNS, the cutoff frequency of the input filter is 1 / (2 ×  $\pi$  × RSNS × C5). For example, RSNS = 10k $\Omega$  and C5 = 100pF results in a cutoff frequency of 160kHz.

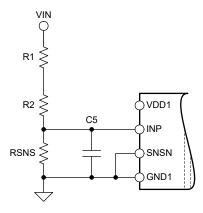


Figure 8-2. Input Filter

#### 8.2.2.2 Connecting the REFIN Pin

The reference input has an internal,  $90k\Omega$  impedance connected to GND2. Consider this impedance when driving the REFIN pin from a high-impedance source. Connect a 100nF capacitor from REFIN to GND2 to filter out high-frequency noise at the reference input. Figure 8-3 shows different options for connecting the REFIN pin.

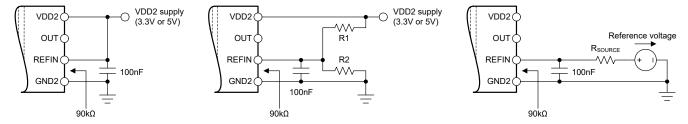


Figure 8-3. Connecting the REFIN Pin

In the first example, REFIN is shorted to VDD2. In the second example,  $V_{REFIN}$  is derived from VDD2 through a resistive divider consisting of R1 and the internal  $90k\Omega$  input impedance. In the third example, an external voltage source drives the reference input pin.



## 8.2.3 Application Curve

Figure 8-4 shows the typical full-scale step response of the AMC0x30R-Q1.

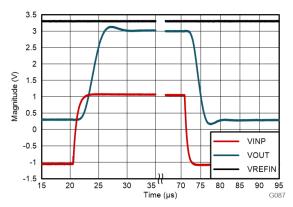


Figure 8-4. Step Response of the AMC0x30R-Q1

# 8.3 Best Design Practices

Do not leave the analog input (INP pin) of the AMC0x30R-Q1 unconnected (floating) when the device is powered up. If the device input is left floating, the device output is not valid.

Do not connect protection diodes to the input (INP pin) of the AMC0x30R-Q1. Diode leakage current potentially introduces significant measurement error especially at high temperatures. The input pin is protected against high voltages by the ESD protection circuit and the high impedance of the external resistive divider.



## 8.4 Power Supply Recommendations

In a typical application, the high-side power supply (VDD1) for the AMC0x30R-Q1 is generated from the low-side supply (VDD2) by an isolated DC/DC converter. A low-cost option is based on the push-pull driver SN6501-Q1 and a transformer that supports the desired isolation voltage ratings.

The AMC0x30R-Q1 does not require any specific power-up sequencing. The high-side power supply (VDD1) is decoupled with a low-ESR, 100nF capacitor (C1) parallel to a low-ESR, 1µF capacitor (C2). The low-side power supply (VDD2) is equally decoupled with a low-ESR, 100nF capacitor (C3) parallel to a low-ESR, 1µF capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible. Figure 8-5 shows a decoupling diagram for the AMC0x30R-Q1.

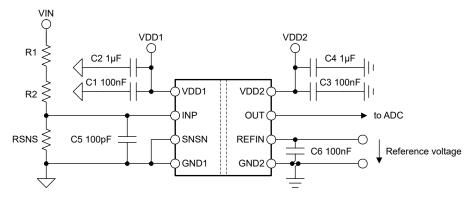


Figure 8-5. Decoupling of the AMC0x30R-Q1

Verify capacitors provide adequate *effective* capacitance under the applicable DC bias conditions experienced in the application. Multilayer ceramic capacitors (MLCC) typically exhibit only a fraction of the nominal capacitance under real-world conditions. Consider this factor when selecting these capacitors. This issue is especially acute in low-profile capacitors, where the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

#### 8.5 Layout

#### 8.5.1 Layout Guidelines

The Layout Example section details a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC0x30R-Q1 supply pins). This example also depicts the placement of other components required by the device.

#### 8.5.2 Layout Example

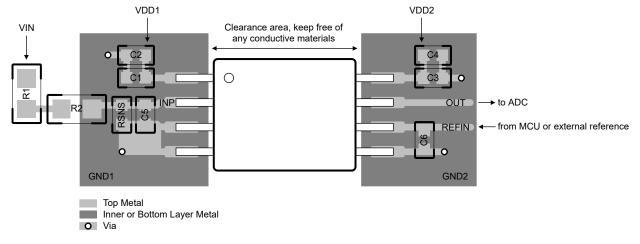


Figure 8-6. Recommended Layout of the AMC0x30R-Q1



# 9 Device and Documentation Support

# 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, Isolation Glossary application note
- Texas Instruments, Semiconductor and IC Package Thermal Metrics application note
- Texas Instruments, ISO72x Digital Isolator Magnetic-Field Immunity application note
- Texas Instrument, SN6501-Q1 Transformer Driver for Isolated Power Supplies data sheet
- Texas Instruments, Isolated Amplifier Voltage Sensing Excel Calculator design tool

## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

# 9.3 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### 9.4 Trademarks

TI E2E<sup>™</sup> is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

## 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 9.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

#### 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

# Changes from Revision \* (October 2024) to Revision A (July 2025)

Page

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

www.ti.com 14-Oct-2025

#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
AMC0330RQDWVRQ1	Active	Production	SOIC (DWV)   8	1000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	C0330R-Q
PAMC0330RQDWVRQ1.A	Active	Preproduction	SOIC (DWV)   8	1000   LARGE T&R	-	Call TI	Call TI	-40 to 125	
PAMC0330RQDWVRQ1.B	Active	Preproduction	SOIC (DWV)   8	1000   LARGE T&R	-	Call TI	Call TI	-40 to 125	

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF AMC0330R-Q1:

Catalog : AMC0330R

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No. RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



# **PACKAGE OPTION ADDENDUM**

www.ti.com 14-Oct-2025

NOTE: Qualified Version Definitions:

 $_{\bullet}$  Catalog - TI's standard catalog product

# **PACKAGE MATERIALS INFORMATION**

www.ti.com 1-Aug-2025

# TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	_	Package Drawing	l .	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC0330RQDWVRQ1	SOIC	DWV	8	1000	330.0	16.4	12.15	6.2	3.05	16.0	16.0	Q1

# **PACKAGE MATERIALS INFORMATION**

www.ti.com 1-Aug-2025



## \*All dimensions are nominal

Ì	Device	Package Type	Type Package Drawing		SPQ	Length (mm)	Width (mm)	Height (mm)	
ı	AMC0330RQDWVRQ1	SOIC	DWV	8	1000	353.0	353.0	32.0	



SOIC



#### NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
- per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



SOIC



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



#### NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



#### IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2025. Texas Instruments Incorporated