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SLLS948A - NOVEMBER 2008-REVISED JULY 2013

# LOW-VOLTAGE HIGH-SPEED QUADRUPLE DIFFERENTIAL LINE RECEIVER WITH ±15-kV IEC ESD PROTECTION

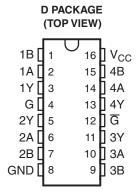
Check for Samples: AM26LV32E-EP

#### **FEATURES**

- Meets or Exceeds Standard TIA/EIA-422-B and ITU Recommendation V.11
- Operates From a Single 3.3-V Power Supply
- ESD Protection for RS422 Bus Pins
  - ±15-kV Human-Body Model (HBM)
  - ±8-kV IEC61000-4-2, Contact Discharge
  - ±15-kV IEC61000-4-2, Air-Gap Discharge
- Switching Rates up to 32 MHz
- Low Power Dissipation: 27 mW Typ
- Open-Circuit, Short-Circuit, and Terminated Fail-Safe
- ±7-V Common-Mode Input Voltage Range With ±200-mV Sensitivity
- Accepts 5-V Logic Inputs With 3.3-V Supply (Enable Inputs)
- Input Hysteresis: 35 mV Typ
- Pin-to-Pin Compatible With AM26C32, AM26LS32
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation

## SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Military (-55°C/125°C)
   Temperature Range (1)
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability



(1) Additional temperature ranges are available - contact factory

## **DESCRIPTION/ORDERING INFORMATION**

The AM26LV32E consists of quadruple differential line receivers with 3-state outputs. These differential receivers have ±15-kV ESD (HBM and IEC61000-4-2, Air-Gap Discharge) and ±8-kV ESD (IEC61000-4-2, Contact Discharge) protection for RS422 bus pins.

This device is designed to meet TIA/EIA-422-B and ITU recommendation V.11 drivers with reduced supply voltage. The device is optimized for balanced bus transmission at switching rates up to 32 MHz. The 3-state outputs permit connection directly to a bus-organized system.

The AM26LV32E has an internal fail-safe circuitry that prevents the device from putting an unknown voltage signal at the receiver outputs. In the open fail-safe, shorted fail-safe, and terminated fail-safe, a high state is produced at the respective output.

This device is supported for partial-power-down applications using  $I_{\text{off}}$ .  $I_{\text{off}}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The AM26LV32EM is characterized for operation from -55°C to 125°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



#### **Table 1. ORDERING INFORMATION**

| T <sub>A</sub> | T <sub>A</sub> PACKAGE <sup>(1)</sup> (2) | ORDERABLE PART NUMBER | TOP-SIDE MARKING |            |
|----------------|---|-----------------------|------------------|------------|
| -55°C to 125°C | SOIC - D                                  | Tape and reel         | AM26LV32EMDREP   | A26LV32EMP |

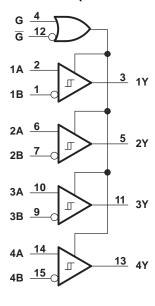
- Package drawings, thermal data, and symbolization are available at <a href="https://www.ti.com/packaging">www.ti.com/packaging</a>.
  For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

## **FUNCTION TABLE**<sup>(1)</sup> (each receiver)

|   | (000:: 1000: |      |          |
|---|--------------|------|----------|
| DIFFERENTIAL  | ENA          | BLES | CUITDUIT |
| INPUT   | G            | G    | OUTPUT   |
| V >02V  | Н            | Х    | Н        |
| V <sub>ID</sub> ≥ 0.2 V                                 | X            | L    | Н        |
| 0.01/ .1/ .001/   | Н            | Х    | ?        |
| $-0.2 \text{ V} < \text{V}_{\text{ID}} < 0.2 \text{ V}$ | X            | L    | ?        |
| V < 02V   | Н            | Х    | L        |
| V <sub>ID</sub> ≤ -0.2 V                                | Χ            | L    | L        |
| Open, shorted, or                                       | Н            | Х    | Н        |
| terminated  | Χ            | L    | Н        |
| X   | L            | Н    | Z        |

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

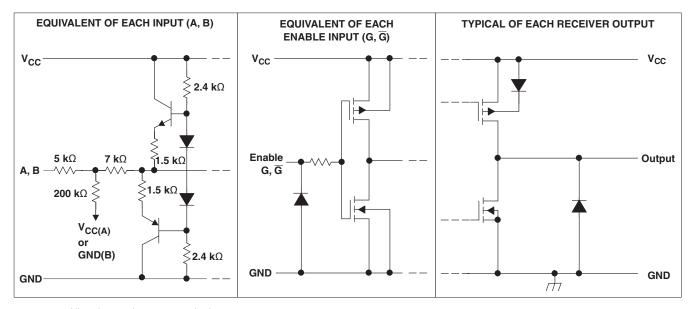
## **LOGIC DIAGRAM (POSITIVE LOGIC)**



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#### **SCHEMATIC**



All resistor values are nominal.

## ABSOLUTE MAXIMUM RATINGS(1) (2)

over operating free-air temperature range (unless otherwise noted)

|                  |  |                    | MIN  | MAX | UNIT |
|------------------|--|--------------------|------|-----|------|
| $V_{CC}$         | Supply voltage range (3)               |                    | -0.5 | 6   | V    |
| V                | lanut valtaga ranga                    | A or B inputs      | -14  | 14  | V    |
| VI               | Input voltage range                    | Enable Inputs      | -0.5 | 6   | V    |
| $V_{\text{ID}}$  | Differential input voltage (4)         |                    | -14  | 14  | V    |
| Vo               | Output voltage range                   |                    | -0.5 | 6   | V    |
| I <sub>IK</sub>  | Input clamp current range              | V <sub>I</sub> < 0 |      | -20 | mA   |
| I <sub>OK</sub>  | Output clamp current range             | V <sub>O</sub> < 0 |      | -20 | mA   |
| lo               | Maximum output current                 |                    |      | ±20 | mA   |
| $T_{J}$          | Operating virtual junction temperature |                    |      | 150 | °C   |
| $\theta_{JA}$    | Package thermal impedance (5) (6)      |                    |      | 73  | °C/W |
| T <sub>A</sub>   | Operating free-air temperature range   |                    | -55  | 125 | °C   |
| T <sub>stg</sub> | Storage temperature range              |                    | -65  | 150 | °C   |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) This device is designed to meet TIA/EIA-422-B and ITU.
- (3) All voltage values except differential input voltage are with respect to the network GND.
- (4) Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.
- (5) Maximum power dissipation is a function of  $T_{J(max)}$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_{J(max)} T_A)/\theta_{JA}$ . Selecting the maximum of 150°C can affect reliability.
- 6) The package thermal impedance is calculated in accordance with JESD 51-7.



## RECOMMENDED OPERATING CONDITIONS

|                 |                                 | MIN         | NOM | MAX        | UNIT |
|-----------------|---------------------------------|-------------|-----|------------|------|
| $V_{CC}$        | Supply voltage                  | 3           | 3.3 | 3.6        | ٧    |
| V <sub>IH</sub> | Enable high-level input voltage | 2           |     | 5.5        | ٧    |
| V <sub>IL</sub> | Enable low-level input voltage  | 0           |     | 8.0        | V    |
| V <sub>IC</sub> | Common-mode input voltage       | -7          |     | 7          | V    |
| $V_{ID}$        | Differential input voltage      | -7          |     | 7          | V    |
| I <sub>OH</sub> | High-level output current       |             |     | <b>–</b> 5 | mA   |
| I <sub>OL</sub> | Low-level output current        |             |     | 5          | mA   |
| T <sub>A</sub>  | Operating free-air temperature  | <b>-</b> 55 |     | 125        | °C   |

## **ELECTRICAL CHARACTERISTICS**

over recommended ranges of common-mode input, supply voltage, and operating free-air temperature (unless otherwise noted)

|                  | PARAMETER  | TEST   | CONDITIONS                | MIN  | TYP <sup>(1)</sup> | MAX  | UNIT |
|------------------|--|--|---------------------------|------|--------------------|------|------|
| V <sub>IT+</sub> | Positive-going input threshold voltage, differential input |  |                           |      |                    | 0.2  | V    |
| $V_{IT-}$        | Negative-going input threshold voltage, differential input |  |                           | -0.2 |                    |      | ٧    |
| $V_{hys}$        | Input hysteresis (V <sub>IT+</sub> - V <sub>IT-</sub> )    |  |                           |      | 35                 |      | mV   |
| $V_{IK}$         | Input clamp voltage, G and $\overline{G}$                  | I <sub>I</sub> = -18 mA                        |                           |      |                    | -1.5 | V    |
|                  |  | $V_{ID} = 200 \text{ mV}, I_{OH} = -$          | 5 mA                      | 2.4  | 3.2                |      | 1    |
| V <sub>OH</sub>  | High-level output voltage                                  | V <sub>ID</sub> = 200 mV, I <sub>OH</sub> = -  | V <sub>CC</sub> – 0.1     |      |                    | V    |      |
| .,               | Lave lave Lave Lave Lave Lave                              | $V_{ID} = -200 \text{ mV}, I_{OL} =$           |                           | 0.17 | 0.5                | V    |      |
| $V_{OL}$         |  | $V_{ID} = -200 \text{ mV}, I_{OL} =$           |                           |      | 0.1                | V    |      |
| l <sub>OZ</sub>  | High-impedance state output current                        | $V_O = V_{CC}$ or GND                          |                           |      |                    | ±50  | μΑ   |
| I <sub>off</sub> | Output current with power off                              | $V_{CC} = 0 \text{ V}, V_{O} = 0 \text{ or } $ | 5.5 V                     |      |                    | ±100 | μΑ   |
|                  | Line input number  | Other insult at 0.1/                           | V <sub>I</sub> = 10 V     |      |                    | 1.5  | A    |
| I <sub>I</sub>   | Line input current   | Other input at 0 V                             | V <sub>I</sub> = -10 V    |      |                    | -2.5 | mA   |
| I                | Enable input current, G and G                              | $V_I = V_{CC}$ or GND                          | •                         |      |                    | ±1   | μA   |
| r <sub>i</sub>   | Input resistance   | $V_{IC} = -7 \text{ V to 7 V, Oth}$            | er input at 0 V           | 4    | 17                 |      | kΩ   |
| I <sub>CC</sub>  | Supply current (total package)                             | $G, \overline{G} = V_{CC} \text{ or GND, N}$   | No load, Line inputs open |      | 8                  | 17   | mA   |
| C <sub>pd</sub>  | Power dissipation capacitance <sup>(2)</sup>               | One channel                                    |                           |      | 150                |      | pF   |

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<sup>(1)</sup> All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C. (2)  $C_{pd}$  determines the no-load dynamic current consumption:  $I_S$  =  $C_{pd}$  ×  $V_{CC}$  × f +  $I_{CC}$ 

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## **SWITCHING CHARACTERISTICS**

over recommended operating free-air temperature range (unless otherwise noted)

|                     | PARAMETER   | TEST CONDITIONS             | MIN | TYP <sup>(1)</sup> | MAX | UNIT |
|---------------------|---|-----------------------------|-----|--------------------|-----|------|
| t <sub>PLH</sub>    | Propagation delay time, low- to high-level output | Con Figure 4                | 8   | 16                 | 26  | ns   |
| t <sub>PHL</sub>    | Propagation delay time, high- to low-level output | See Figure 1                | 8   | 16                 | 26  | ns   |
| t <sub>t</sub>      | Transition time                                   | See Figure 1                |     | 5                  |     | ns   |
| t <sub>PZH</sub>    | Output-enable time to high level                  | See Figure 2                |     | 17                 | 40  | ns   |
| t <sub>PZL</sub>    | Output-enable time to low level                   | See Figure 3                |     | 10                 | 40  | ns   |
| t <sub>PHZ</sub>    | Output-disable time from high level               | See Figure 2                |     | 20                 | 40  | ns   |
| t <sub>PLZ</sub>    | Output-disable time from low level                | See Figure 3                |     | 16                 | 40  | ns   |
| t <sub>sk(p)</sub>  | Pulse skew  | See Figure 1 (2)            |     | 4                  | 6   | ns   |
| t <sub>sk(o)</sub>  | Pulse skew  | See Figure 1 (3)            |     | 4                  | 6   | ns   |
| t <sub>sk(pp)</sub> | Pulse skew (device to device)                     | See Figure 1 <sup>(4)</sup> |     | 6                  | 9   | ns   |
| f <sub>(max)</sub>  | Maximum operating frequency                       | See Figure 1                |     | 32                 |     | MHz  |

- All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .  $t_{sk(p)}$  is  $|t_{pLH} t_{pHL}|$  of each channel of same device.  $t_{sk(0)}$  is the maximum difference in propagation delay times between any two channels of same device switching in the same direction.  $t_{sk(pp)}$  is the maximum difference in propagation delay times between any two channels of any two devices switching in the same direction.

## **ESD PROTECTION**

| PARAMETER      | TEST CONDITIONS                 | TYP | UNIT |
|----------------|---------------------------------|-----|------|
|                | НВМ                             | ±15 |      |
| Receiver input | IEC61000-4-2, Air-Gap Discharge | ±15 | kV   |
|                | IEC61000-4-2, Contact Discharge | ±8  |      |

Product Folder Links: AM26LV32E-EP



#### PARAMETER MEASUREMENT INFORMATION

- A. C<sub>L</sub> includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 10 MHz, duty cycle = 50%,  $t_r = t_f \le 2ns$ .
- C. To test the active-low enable  $\overline{G}$ , ground G and apply an inverted waveform  $\overline{G}$ .

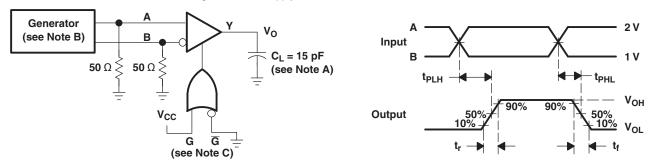


Figure 1. Test Circuit and Voltage Waveforms, tplH and tpHL

- A. C<sub>L</sub> includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 10 MHz, duty cycle = 50%,  $t_r = t_f \le 2ns$ .
- C. To test the active-low enable  $\overline{G}$ , ground G and apply an inverted waveform  $\overline{G}$ .

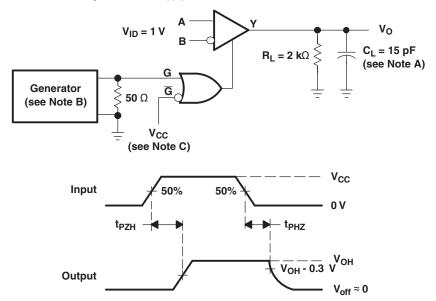


Figure 2. Test Circuit and Voltage Waveforms, tpzH and tpHZ

- A. C<sub>1</sub> includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 10 MHz, duty cycle = 50%,  $t_r = t_f \le 2ns$ .
- C. To test the active-low enable  $\overline{G}$ , ground G and apply an inverted waveform  $\overline{G}$ .

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## **PARAMETER MEASUREMENT INFORMATION (continued)**

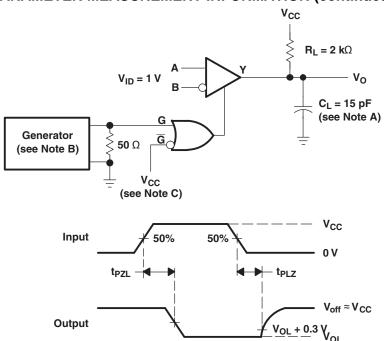


Figure 3. Test Circuit and Voltage Waveforms,  $t_{\text{PZL}}$  and  $t_{\text{PLZ}}$ 



## **REVISION HISTORY**

| Cł | hanges from Original (November 2008) to Revision A  | Page |
|----|---|------|
| •  | Changed units for V <sub>IC</sub> and V <sub>ID</sub> recommended operating conditions from mA to V | 4    |

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#### PACKAGING INFORMATION

| Orderable part number | Status | Material type | Package   Pins | Package qty   Carrier | <b>RoHS</b> (3) | Lead finish/<br>Ball material | MSL rating/<br>Peak reflow | Op temp (°C) | Part marking (6) |
|-----------------------|--------|---------------|----------------|-----------------------|-----------------|-------------------------------|----------------------------|--------------|------------------|
| AM26LV32EMDREP        | Active | Production    | SOIC (D)   16  | 2500   LARGE T&R      | Yes             | NIPDAU                        | Level-1-260C-UNLIM         | -55 to 125   | A26LV32EMP       |
| AM26LV32EMDREP.A      | Active | Production    | SOIC (D)   16  | 2500   LARGE T&R      | Yes             | NIPDAU                        | Level-1-260C-UNLIM         | -55 to 125   | A26LV32EMP       |
| V62/09602-01XE        | Active | Production    | SOIC (D)   16  | 2500   LARGE T&R      | Yes             | NIPDAU                        | Level-1-260C-UNLIM         | -55 to 125   | A26LV32EMP       |

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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#### OTHER QUALIFIED VERSIONS OF AM26LV32E-EP:

Catalog : AM26LV32E

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



## **PACKAGE OPTION ADDENDUM**

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NOTE: Qualified Version Definitions:

 $_{\bullet}$  Catalog - TI's standard catalog product

## **PACKAGE MATERIALS INFORMATION**

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## TAPE AND REEL INFORMATION





| A0 | Dimension designed to accommodate the component width     |
|----|---|
| В0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

| Device         |      | Package<br>Drawing |    | SPQ  | Reel<br>Diameter<br>(mm) | Reel<br>Width<br>W1 (mm) | A0<br>(mm) | B0<br>(mm) | K0<br>(mm) | P1<br>(mm) | W<br>(mm) | Pin1<br>Quadrant |
|----------------|------|--------------------|----|------|--------------------------|--------------------------|------------|------------|------------|------------|-----------|------------------|
| AM26LV32EMDREP | SOIC | D                  | 16 | 2500 | 330.0                    | 16.4                     | 6.5        | 10.3       | 2.1        | 8.0        | 16.0      | Q1               |

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## \*All dimensions are nominal

| Ì | Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ı | AM26LV32EMDREP | SOIC         | D               | 16   | 2500 | 353.0       | 353.0      | 32.0        |

## D (R-PDS0-G16)

## PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



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