AM26C32 Quadruple Differential Line Receiver

1 Features

- Meets or exceeds the requirements of ANSI TIA/EIA-422-B, TIA/EIA-423-B, and ITU recommendation V.10 and V.11
- Low power, I_{CC} = 10 mA typical
- ±7-V Common-mode range with ±200-mV sensitivity
- Input hysteresis: 60 mV typical
- t_{pd} = 17 ns typical
- Operates from a single 5-V supply
- 3-State outputs
- Input fail-safe circuitry
- Improved replacements for AM26LS32 device
- Available in Q-temp automotive

2 Applications

- High-reliability automotive applications
- Factory automation
- ATM and cash counters
- Smart grid
- AC and servo motor drives

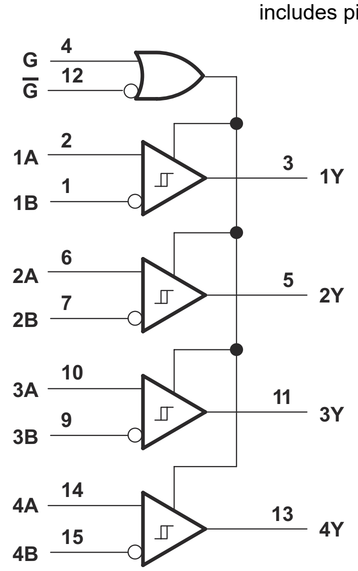
3 Description

The AM26C32 device is a quadruple differential line receiver for balanced or unbalanced digital data transmission. The enable function is common to all four receivers and offers a choice of active-high or active-low input. The 3-state outputs permit connection directly to a bus-organized system. Fail-safe design specifies that if the inputs are open, the outputs always are high. The AM26C32 devices are manufactured using a BiCMOS process, which is a combination of bipolar and CMOS transistors. This process provides the high voltage and current of bipolar with the low power of CMOS to reduce the power consumption to about one-fifth that of the standard AM26LS32, while maintaining AC and DC performance.

Package Information

PART NUMBER	PACKAGE[(1)]	PACKAGE SIZE[(2)]
AM26C32	PDIP (N, 16)	19.3 mm × 9.4 mm
	SO (NS, 16)	10.2 mm × 7.8 mm
	SOIC (D, 16)	9.9 mm × 6 mm
	SSOP (DB, 16)	6.2mm × 7.8mm
	TSSOP (PW, 16)	5 mm × 6.4 mm
	CDIP (J, 16)	mm × 6.92 mm
	CFP (W, 16)	10.3 mm × 6.73 mm
	LCCC (FK, 20)	8.90 mm × 8.90 mm

(1) For more Information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Pin Configuration and Functions

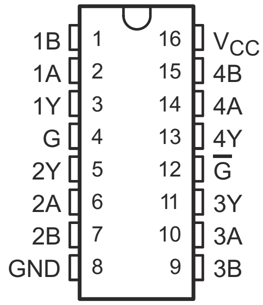


Figure 4-1. D, DB, N, NS, PW, J or W Package 16-Pin SOIC, PDIP, SO, TSSOP, CDIP, or CFP (Top View)

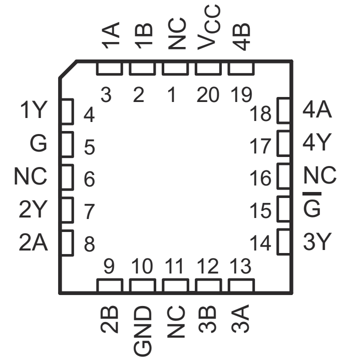


Figure 4-2. FK Package, 20-Pin LCCC (Top View)

PIN			I/O	DESCRIPTION
NAME	LCCC	SOIC, PDIP, SO, TSSOP, CFP, or CDIP		
1A	3	2	I	RS422/RS485 differential input (noninverting)
1B	2	1	I	RS422/RS485 differential input (inverting)
1Y	4	3	O	Logic level output
2A	8	6	I	RS422/RS485 differential input (noninverting)
2B	9	7	I	RS422/RS485 differential input (inverting)
2Y	7	5	O	Logic level output
3A	13	10	I	RS422/RS485 differential input (noninverting)
3B	12	9	I	RS422/RS485 differential input (inverting)
3Y	14	11	O	Logic level output
4A	18	14	I	RS422/RS485 differential input (noninverting)
4B	19	15	I	RS422/RS485 differential input (inverting)
4Y	17	13	O	Logic level output
G	5	4	I	Active-high select
$\overline{G}$	15	12	I	Active-low select
GND	10	8	—	Ground
NC[1]	1	—	—	Do not connect
	6			
	11			
	16			
V_{CC}	20	16	—	Power Supply

(1) NC – no internal connection.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [(1)]

			MIN	MAX	UNIT
V_{CC}	Supply voltage[(2)]			7	V
V_I	Input voltage	A or B inputs	–11	14	V
		G or $\overline{G}$ inputs	–0.5	V_{CC} + 0.5	
V_{ID}	Differential input voltage		–14	14	V
V_O	Output voltage		–0.5	V_{CC} + 0.5	V
I_O	Output current			±25	mA
T_{stg}	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the network ground terminal.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2		V_{cc}	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{IC}	Common-mode input voltage		-7		+7	V
I_{OH}	High-level output current				–6	mA
I_{OL}	Low-level output current				6	mA
T_A	Operating free-air temperature	AM26C32C	0		70	°C
		AM26C32I	–40		85	
		AM26C32Q	–40		125	
		AM26C32M	–55		125	

5.4 Thermal Information

THERMAL METRIC(1)		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	UNIT
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.6	102.6	60.6	88.5	107.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	43.5	48.7	48.1	46.2	38.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.2	54.3	40.6	50.7	53.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	10.4	11.8	27.5	13.5	3.2	°C/W
Ψ_{JB}	Junction-to-bottom characterization parameter	42.8	53.5	40.3	50.3	53.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.5 Thermal Information

THERMAL METRIC(1)		J (CDIP)	FK (LCCC)	W (CFP)	UNIT
		16 PINS	20 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.6	61.6	99.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	54.6	36.8	51.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.1	36.1	86.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	22.9	31	23.7	°C/W
Ψ_{JB}	Junction-to-bottom characterization parameter	41.6	36	80.2	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	4.2	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Differential input high-threshold voltage	$V_O = V_{OH(min)}$, I_{OH} = –440 µA	V_{IC} = –7 V to 7 V			0.2	V
			V_{IC} = 0 V to 5.5 V			0.1	
V_{IT-}	Differential input low-threshold voltage	V_O = 0.45 V, I_{OL} = 8 mA	V_{IC} = –7 V to 7 V	–0.2(2)			V
			V_{IC} = 0 V to 5.5 V	–0.1(2)			
V_{hys}	Hysteresis voltage ($V_{IT+} – V_{IT-}$)				60		mV
V_{IK}	Enable input clamp voltage	V_{CC} = 4.5 V, I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = –6 mA		3.8			V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, I_{OL} = 6 mA			0.2	0.3	V
I_{OZ}	OFF-state (high-impedance state) output current	$V_O = V_{CC}$ or GND			±0.5	±5	µA
I_I	Line input current	V_I = 10 V, Other input at 0 V				1.5	mA
		V_I = –10 V, Other input at 0 V				–2.5	mA
I_{IH}	High-level enable current	V_I = 2.7 V				20	µA
I_{IL}	Low-level enable current	V_I = 0.4 V				–100	µA
r_i	Input resistance	One input to ground		12	17		kΩ
I_{CC}	Quiescent supply current	V_{CC} = 5.5 V			10	15	mA

(1) All typical values are at V_{CC} = 5 V, V_{IC} = 0, and T_A = 25°C.

(2) The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage.

5.7 Switching Characteristics

over operating free-air temperature range, C_L = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	AM26C32C AM26C32I			AM26C32Q AM26C32M			UNIT
			MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 6-1	9	17	27	9	17	27	ns
t_{PHL}	Propagation delay time, high- to low-level output		9	17	27	9	17	27	ns
t_{TLH}	Output transition time, low- to high-level output	See Figure 6-1		4	9		4	10	ns
t_{THL}	Output transition time, high- to low-level output			4	9		4	9	ns
t_{PZH}	Output enable time to high-level	See Figure 6-2		13	22		13	22	ns
t_{PZL}	Output enable time to low-level			13	22		13	22	ns
t_{PHZ}	Output disable time from high-level	See Figure 6-2		13	22		13	26	ns
t_{PLZ}	Output disable time from low-level			13	22		13	25	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

5.8 Typical Characteristics

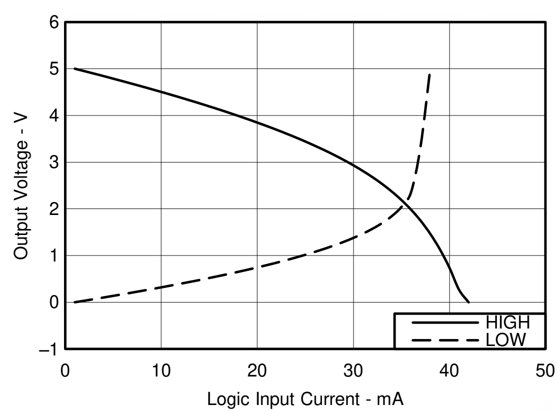
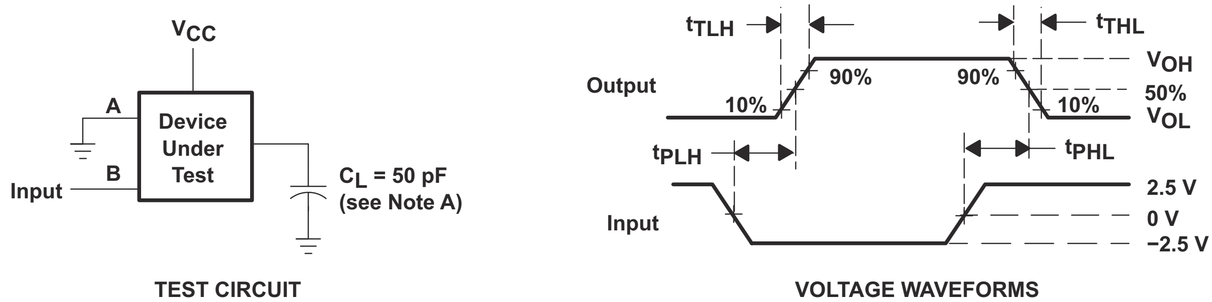


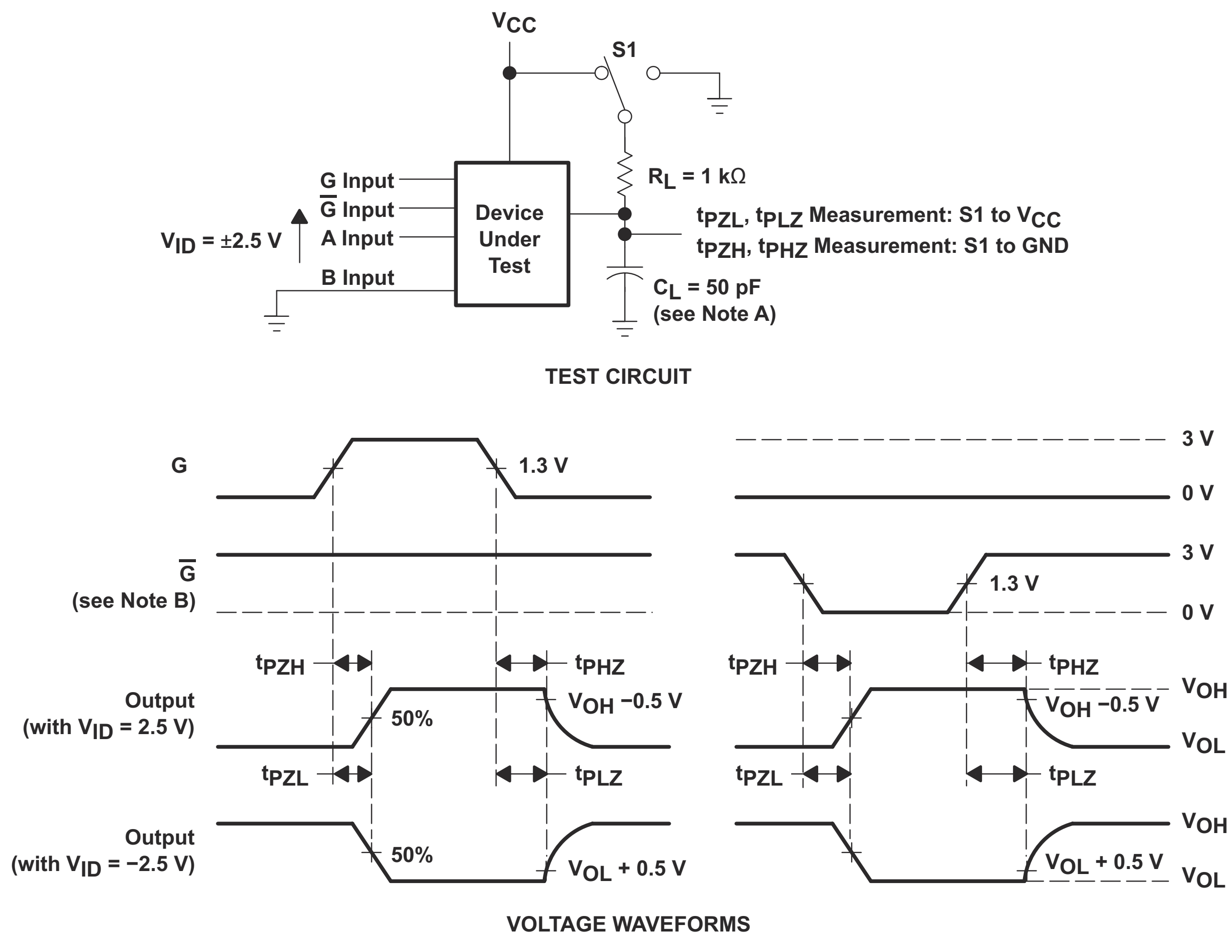
Figure 5-1. Output Voltage vs Input Current

6 Parameter Measurement Information



A. C_L includes probe and jig capacitance.

Figure 6-1. Switching Test Circuit and Voltage Waveforms



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ≤ 50%, $t_r = t_f$ = 6 ns.

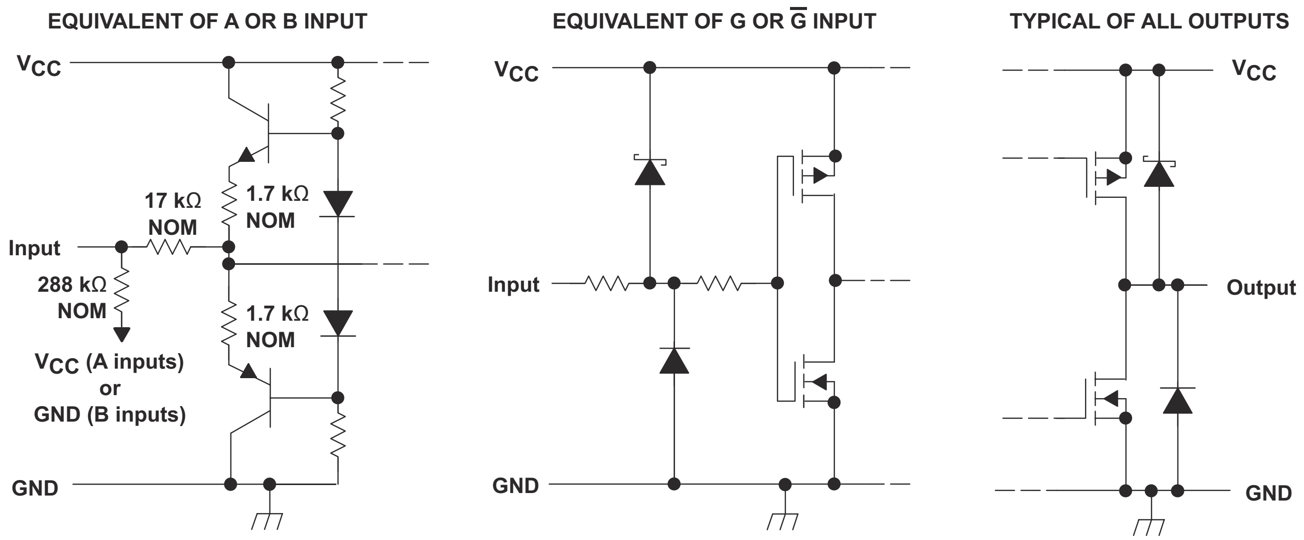
Figure 6-2. Enable/Disable Time Test Circuit and Output Voltage Waveforms

7 Detailed Description

7.1 Overview

The AM26C32 is a quadruple differential line receiver that meets the necessary requirements for NSI TIA/EIA-422-B, TIA/EIA-423-B, and ITU Recommendation V.10 and V.11. This device allows a low power or low voltage MCU to interface with heavy machinery, subsystems and other devices through long wires of up to 1000m, giving any design a reliable and easy to use connection. As any RS422 interface, the AM26C32 works in a differential voltage range, which enables very good signal integrity.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 ±7-V Common-Mode Range With ±200-mV Sensitivity

For a common-mode voltage varying from -7V to 7V, the input voltage is acceptable in low ranges greater than 200 mV as a standard.

7.3.2 Input Fail-Safe Circuitry

RS-485 specifies that the receiver output state should be logic high for differential input voltages of V_{AB} ≥ +200 mV and logic low for V_{AB} ≤ –200 mV. For input voltages in between these limits, a receiver's output state is not defined and can randomly assume high or low. Removing the uncertainty of random output states, modern transceiver designs include internal biasing circuits that put the receiver output into a defined state (typically high) in the absence of a valid input signal.

A loss of input signal can be caused by an pen circuit caused by a wire break or the unintentional disconnection of a transceiver from the bus. The AM26C32 has an internal circuit that ensures functionality during an idle bus.

7.3.3 Active-High and Active-Low

The device can be configure using the G and $\overline{G}$ logic inputs to select receiver output. The high voltage or logic 1 on the G pin, allows the device to operate on an active-high and having a low voltage or logic 0 on the $\overline{G}$ enables active low operation. These are simply a way to configure the logic to match that of the receiving or transmitting controller or microprocessor.

7.3.4 Operates from a Single 5-V Supply

Both the logic and receivers operate from a single 5-V rail, making designs much more simple. The line drivers and receivers can operate off the same rail as the host controller or a similar low voltage supply, thus simplifying power structure.

7.4 Device Functional Modes

7.4.1 Enable and Disable

The receivers implemented in these RS422 devices can be configured using the G and $\overline{G}$ pins to be enabled or disabled. This allows users to ignore or filter out transmissions as desired.

Table 7-1. Function Table (Each Receiver)

DIFFERENTIAL INPUT	ENABLES[1]		OUTPUT
A/B	G	$\overline{G}$	Y
$V_{ID} \geq V_{IT+}$	H	X	H
	X	L	H
$V_{IT} < V_{ID} < V_{IT+}$	H	X	?
	X	L	?
$V_{ID} \leq V_{IT-}$	H	X	L
	X	L	L
X	L	H	Z

(1) H = High level, L = Low level, X = Irrelevant, Z = High impedance (off), ? = Indeterminate

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

When designing a system that uses drivers, receivers, and transceivers that comply with RS-422 or RS-485, proper cable termination is essential for highly reliable applications with reduced reflections in the transmission line. Because RS-422 allows only one driver on the bus, if termination is used, it is placed only at the end of the cable near the last receiver. In general, RS-485 requires termination at both ends of the cable. Factors to consider when determining the type of termination usually are performance requirements of the application and the ever-present factor, cost. The different types of termination techniques discussed are unterminated lines, parallel termination, AC termination, and multipoint termination. Laboratory waveforms for each termination technique (except multipoint termination) illustrate the usefulness and robustness of RS-422 (and, indirectly, RS-485). Similar results can be obtained if 485-compliant devices and termination techniques are used. For laboratory experiments, 100 feet of 100-Ω, 24-AWG, twisted-pair cable (Bertek) was used. A single driver and receiver, TI AM26C31C and AM26C32C, respectively, were tested at room temperature with a 5-V supply voltage. Two plots per termination technique are shown. In each plot, the top waveform is the driver input and the bottom waveform is the receiver output. To show voltage waveforms related to transmission-line reflections, the first plot shows output waveforms from the driver at the start of the cable; the second plot shows input waveforms to the receiver at the far end of the cable.

8.2 Typical Application

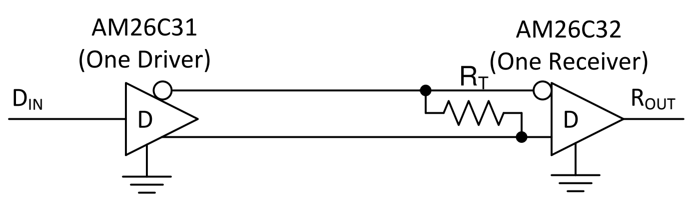


Figure 8-1. Differential Terminated Configuration

8.2.1 Design Requirements

Resistor and capacitor (if used) termination values are shown for each laboratory experiment, but vary from system to system. For example, the termination resistor, R_T, must be within 20% of the characteristic impedance, Zo , of the cable and can vary from about 80 Ω to 120 Ω.

8.2.2 Detailed Design Procedure

Figure 8-1 shows a configuration with no termination. Although reflections are present at the receiver inputs at a data signaling rate of 200 kbps with no termination, the RS-422-compliant receiver reads only the input differential voltage and produces a clean signal at the output.

8.2.3 Application Curve

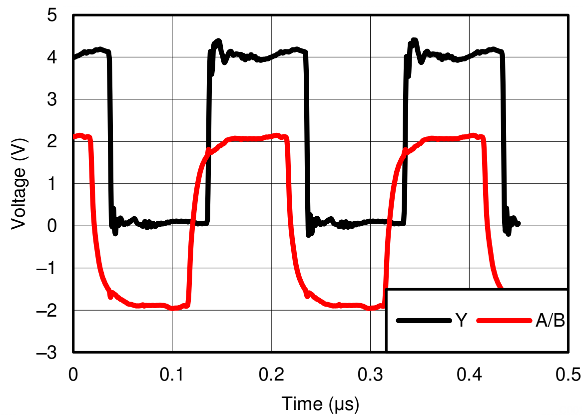


Figure 8-2. Differential 120-Ω Terminated Output Waveforms (Cat 5E Cable)

8.3 Power Supply Recommendations

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies.

8.4 Layout

8.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

8.4.2 Layout Example

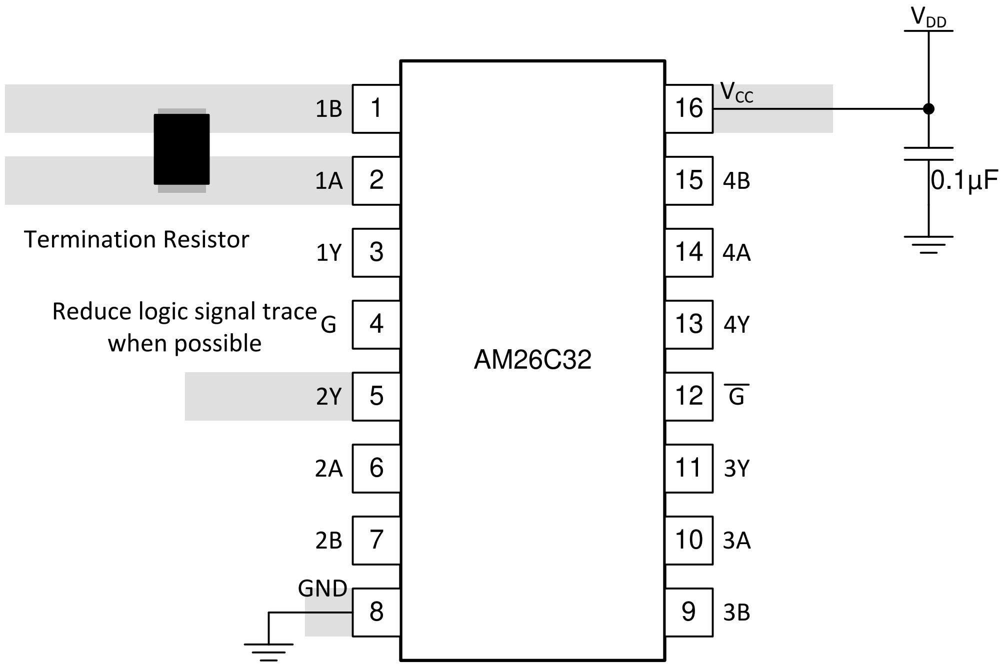


Figure 8-3. Trace Layout on PCB and Recommendations

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision K (October 2018) to Revision M (October 2023) — **Page**

- Changed Device Information table to the *Package Information* table.......... 1
- Updated the *Thermal Information* table.......... 5

Changes from Revision K (June 2015) to Revision L (October 2018) — **Page**

- Changed I_I unit value From: µA To: mA in the *Electrical Characteristics* table.......... 5

Changes from Revision J (February 2014) to Revision K (June 2015) — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.......... 1

Changes from Revision I (September 2004) to Revision J (February 2014) — **Page**

- Updated document to new TI data sheet format - no specification changes.......... 1
- Deleted *Ordering Information* table.......... 1
- Updated *Features* 1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9164001Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9164001Q2A AM26C32 MFKB
5962-9164001QEA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9164001QE A AM26C32MJB
5962-9164001QFA	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9164001QF A AM26C32MWB
AM26C32CD	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	0 to 70	AM26C32C
AM26C32CDBR	Obsolete	Production	SSOP (DB) | 16	-	-	Call TI	Call TI	-	26C32
AM26C32CDR	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	0 to 70	AM26C32C
AM26C32CN	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	AM26C32CN
AM26C32CN.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	AM26C32CN
AM26C32CNE4	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	AM26C32CN
AM26C32CNSR	Obsolete	Production	SOP (NS) | 16	-	-	Call TI	Call TI	0 to 70	26C32
AM26C32ID	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-40 to 85	AM26C32I
AM26C32IDBR	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(26C32, 26C32I)
AM26C32IDBR.A	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(26C32, 26C32I)
AM26C32IDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26C32I
AM26C32IDR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26C32I
AM26C32IDRE4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26C32I
AM26C32IDRG4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26C32I
AM26C32IN	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	AM26C32IN
AM26C32IN.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	AM26C32IN
AM26C32INSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C32I
AM26C32INSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C32I
AM26C32IPW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-40 to 85	26C32I
AM26C32IPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C32I
AM26C32IPWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C32I

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AM26C32IPWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C32I
AM26C32MFKB	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9164001Q2A AM26C32 MFKB
AM26C32MFKB.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9164001Q2A AM26C32 MFKB
AM26C32MJB	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9164001QE A AM26C32MJB
AM26C32MJB.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9164001QE A AM26C32MJB
AM26C32MWB	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9164001QF A AM26C32MWB
AM26C32MWB.A	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9164001QF A AM26C32MWB
AM26C32QD	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-40 to 125	AM26C32Q
AM26C32QDG4	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-40 to 125	26C32Q
AM26C32QDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AM26C32Q
AM26C32QDR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AM26C32Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF AM26C32, AM26C32M :

- Catalog : AM26C32

- Enhanced Product : AM26C32-EP, AM26C32-EP

- Military : AM26C32M

NOTE: Qualified Version Definitions:

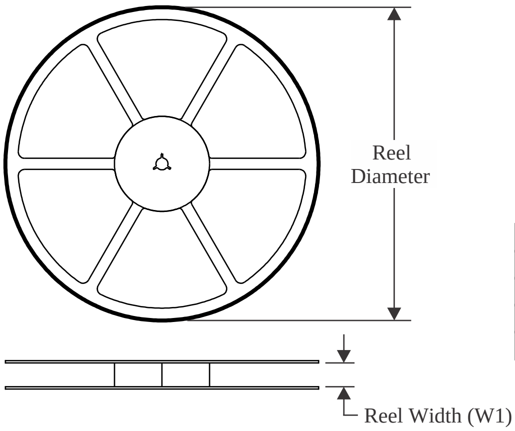
- Catalog - TI's standard catalog product

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

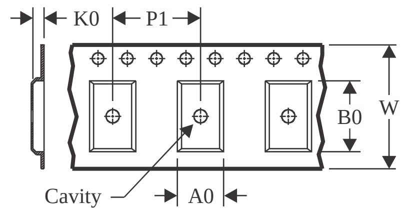
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

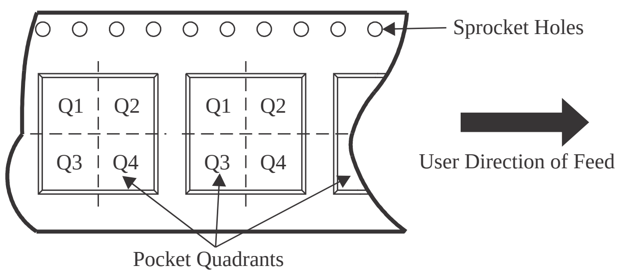


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

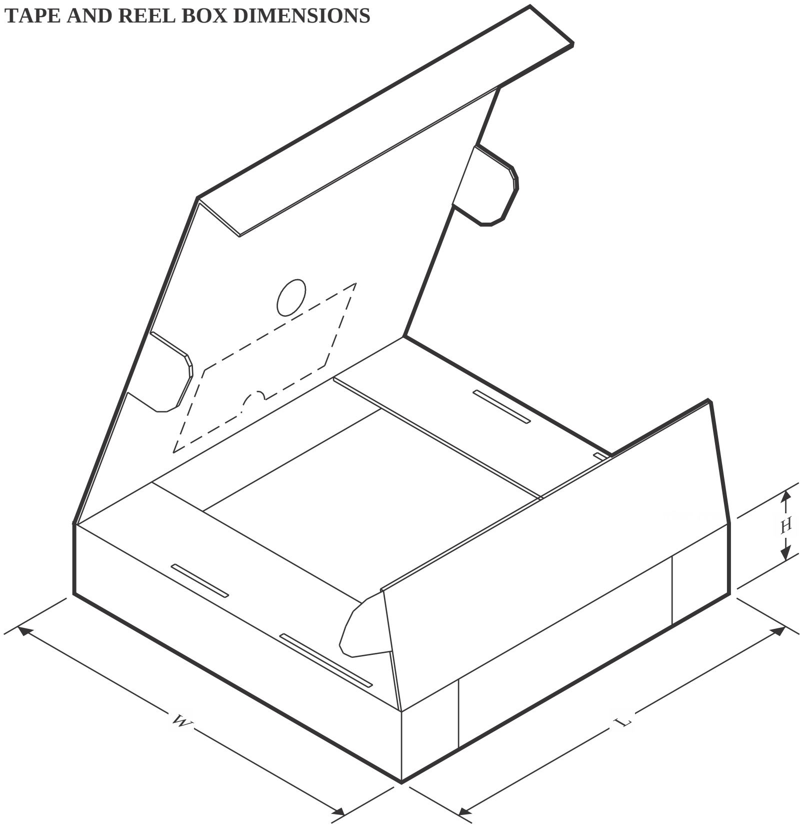
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM26C32IDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
AM26C32IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26C32INSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
AM26C32IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
AM26C32QDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

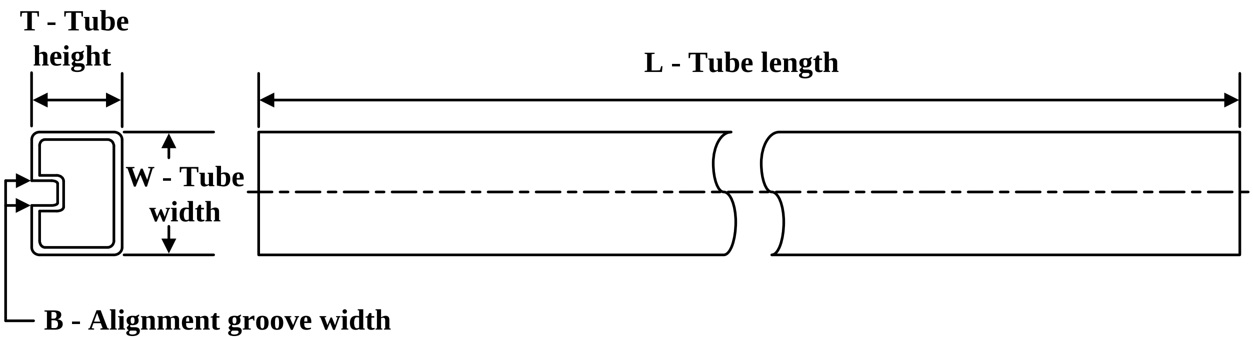
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

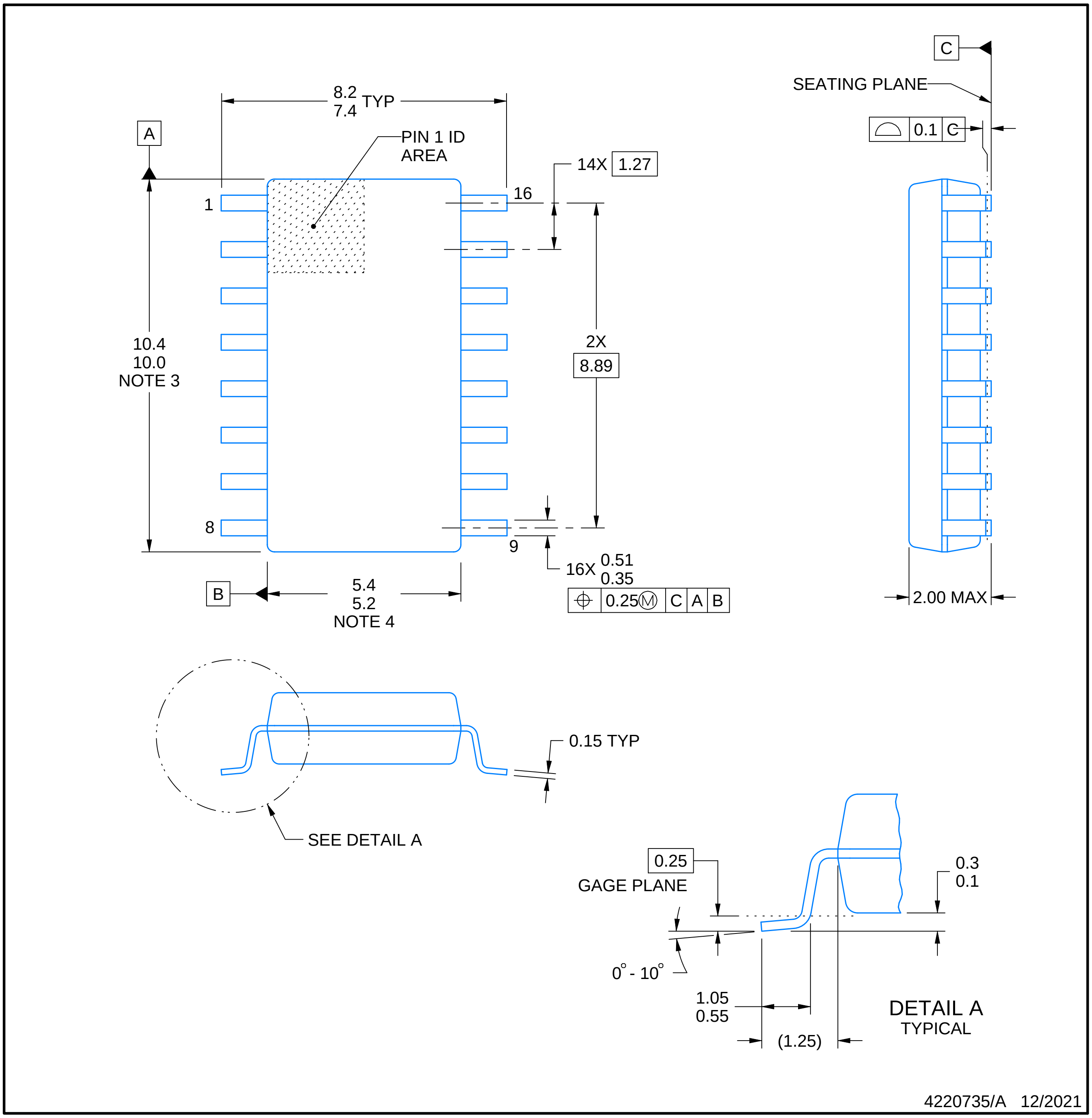
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM26C32IDBR	SSOP	DB	16	2000	353.0	353.0	32.0
AM26C32IDR	SOIC	D	16	2500	340.5	336.1	32.0
AM26C32INSR	SOP	NS	16	2000	353.0	353.0	32.0
AM26C32IPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
AM26C32QDR	SOIC	D	16	2500	353.0	353.0	32.0

TUBE



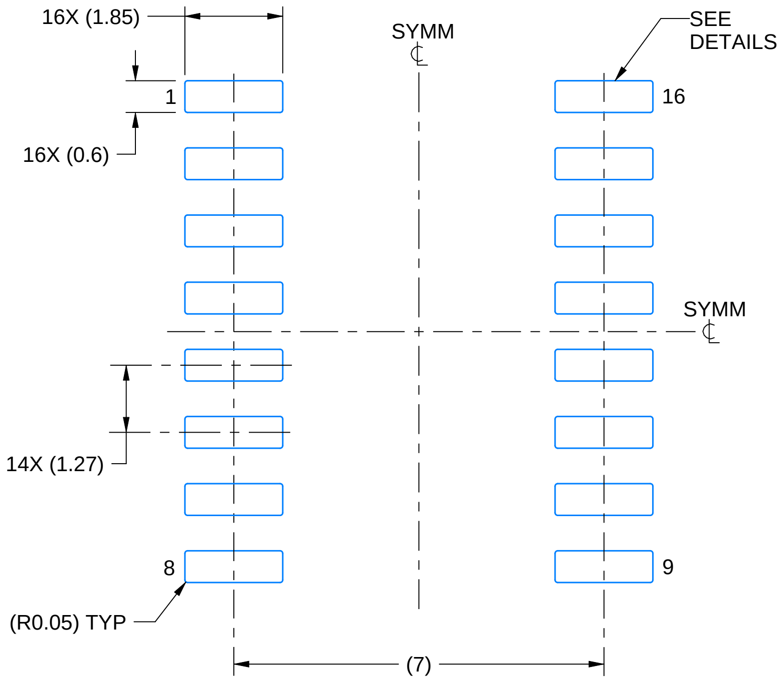
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9164001Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9164001QFA	W	CFP	16	25	506.98	26.16	6220	NA
AM26C32CN	N	PDIP	16	25	506	13.97	11230	4.32
AM26C32CN	N	PDIP	16	25	506	13.97	11230	4.32
AM26C32CN.A	N	PDIP	16	25	506	13.97	11230	4.32
AM26C32CN.A	N	PDIP	16	25	506	13.97	11230	4.32
AM26C32CNE4	N	PDIP	16	25	506	13.97	11230	4.32
AM26C32CNE4	N	PDIP	16	25	506	13.97	11230	4.32
AM26C32IN	N	PDIP	16	25	506	13.97	11230	4.32
AM26C32IN.A	N	PDIP	16	25	506	13.97	11230	4.32
AM26C32MFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
AM26C32MFKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA
AM26C32MWB	W	CFP	16	25	506.98	26.16	6220	NA
AM26C32MWB.A	W	CFP	16	25	506.98	26.16	6220	NA

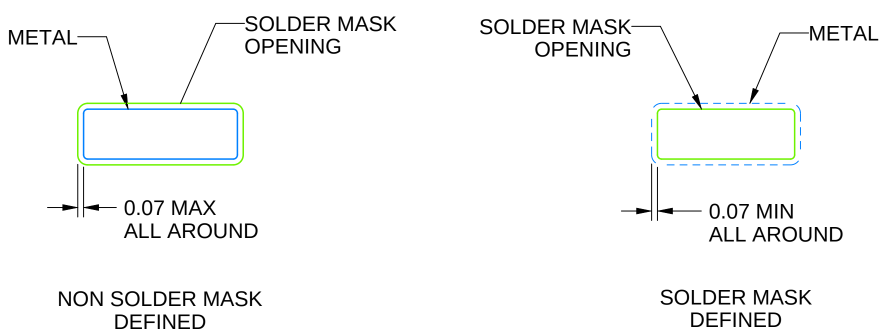


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X

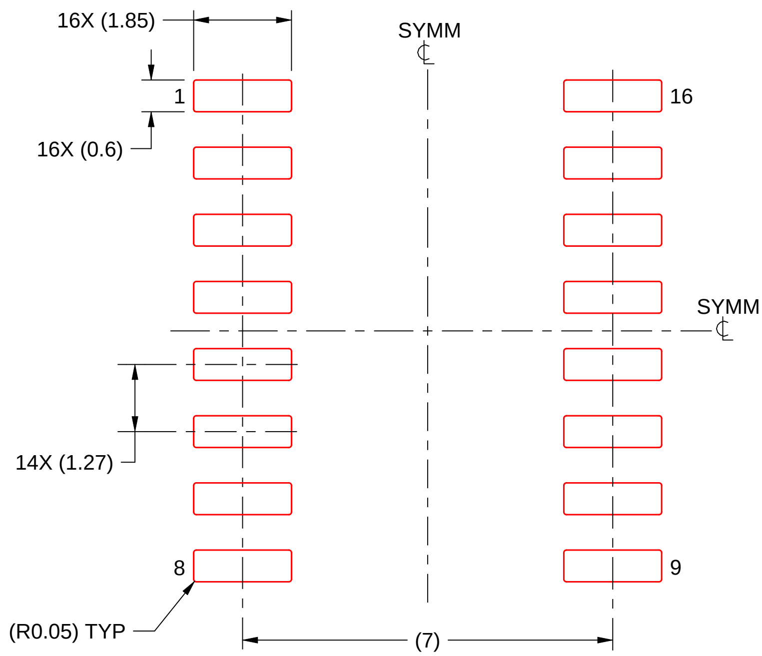


SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



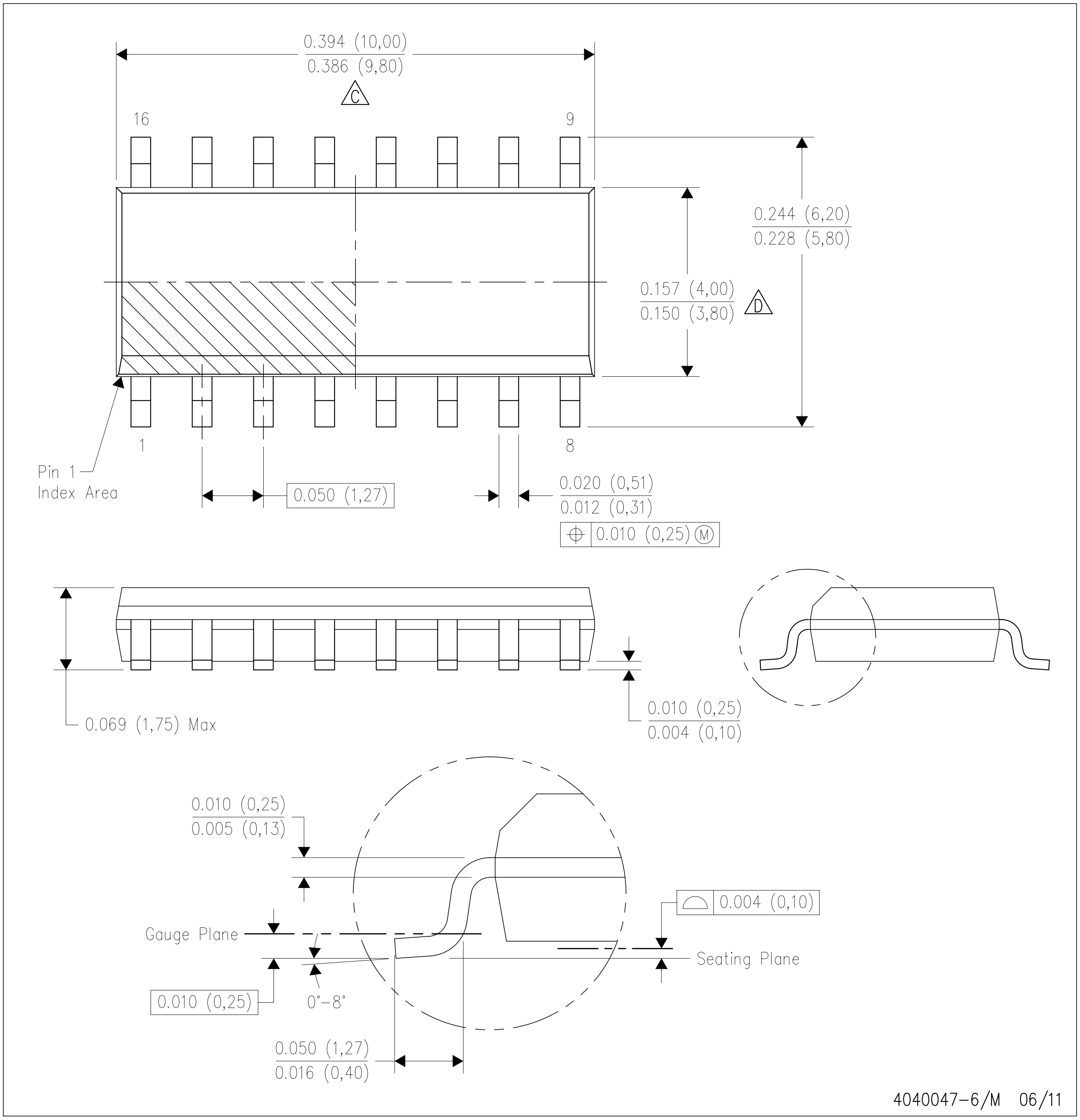
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

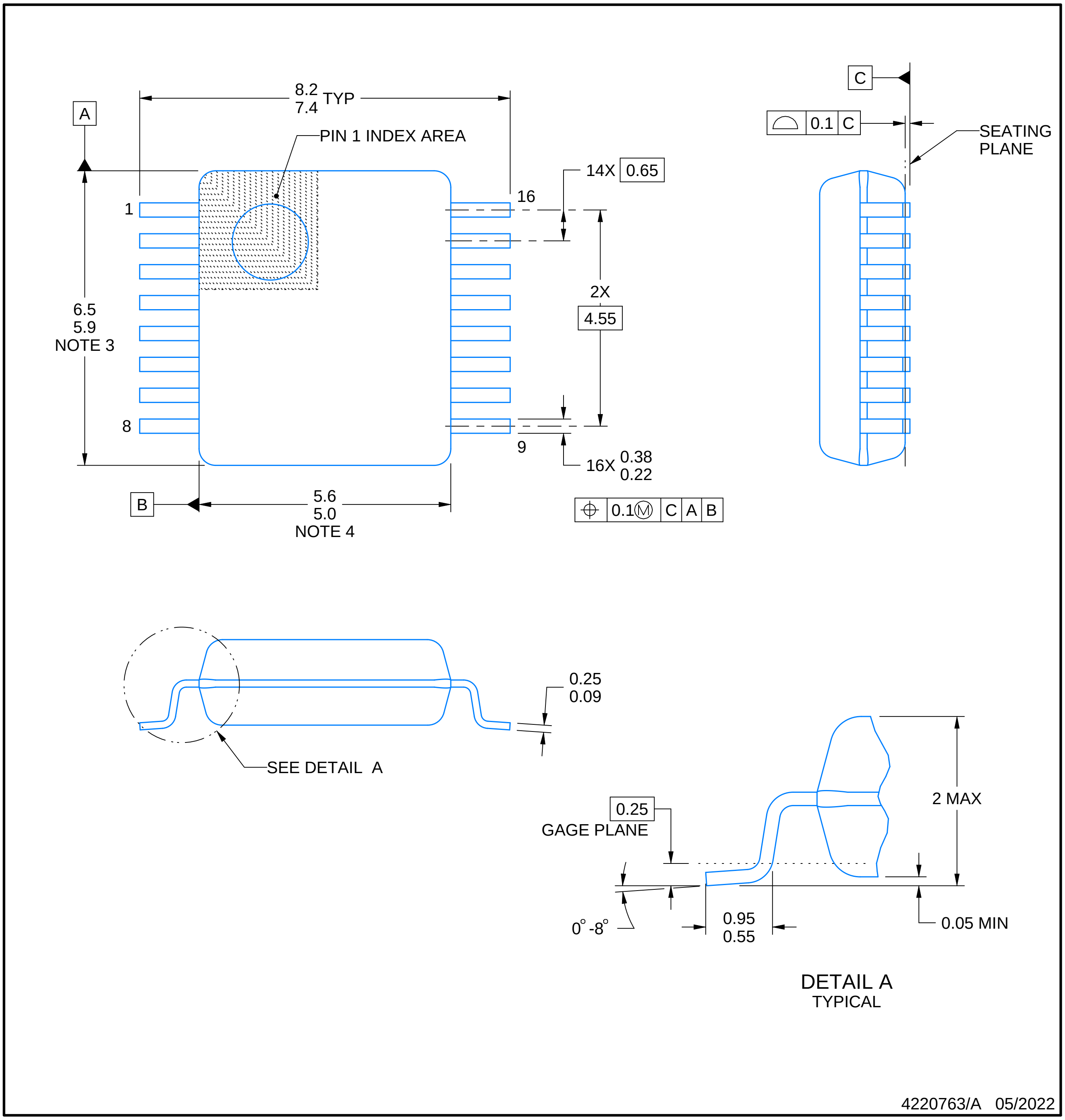


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AC.

PACKAGE OUTLINE

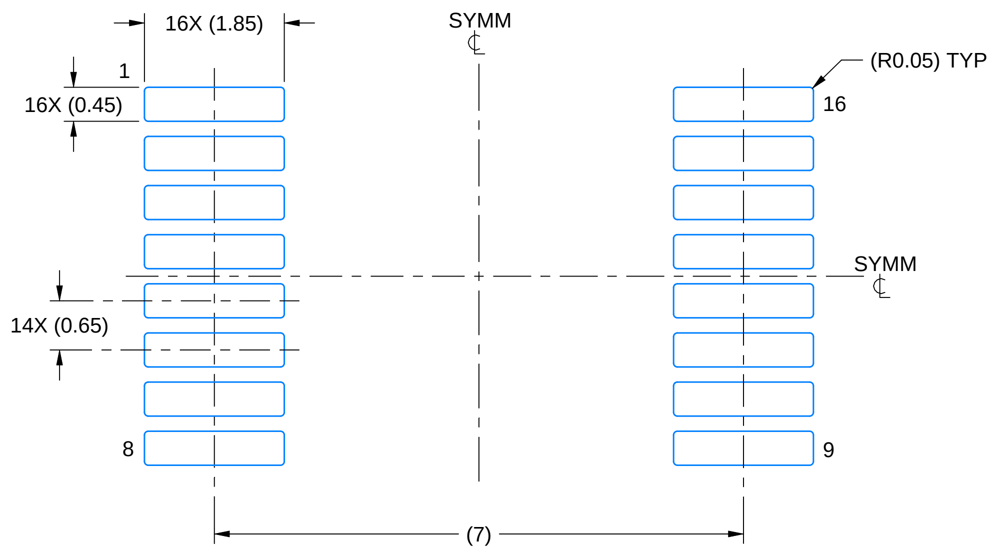
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

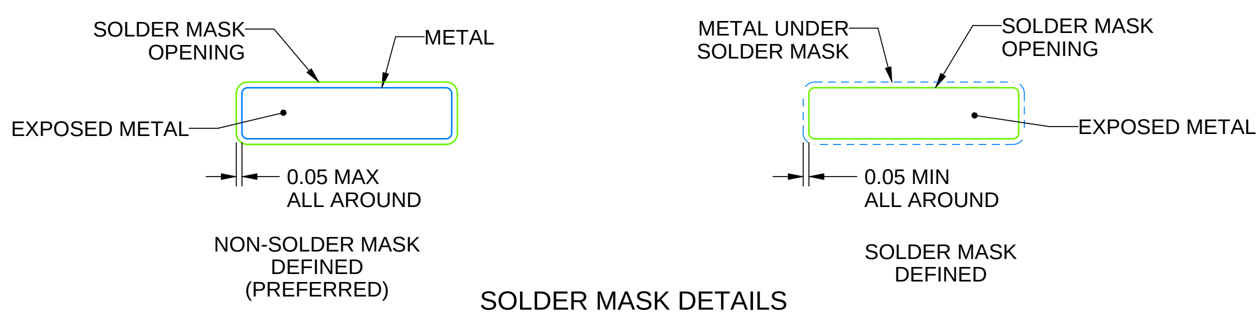


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

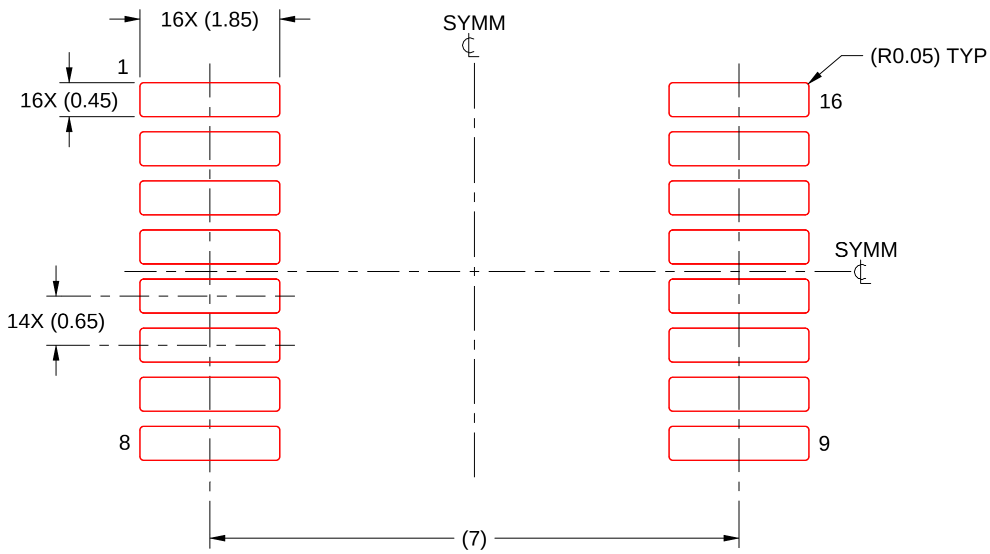


SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



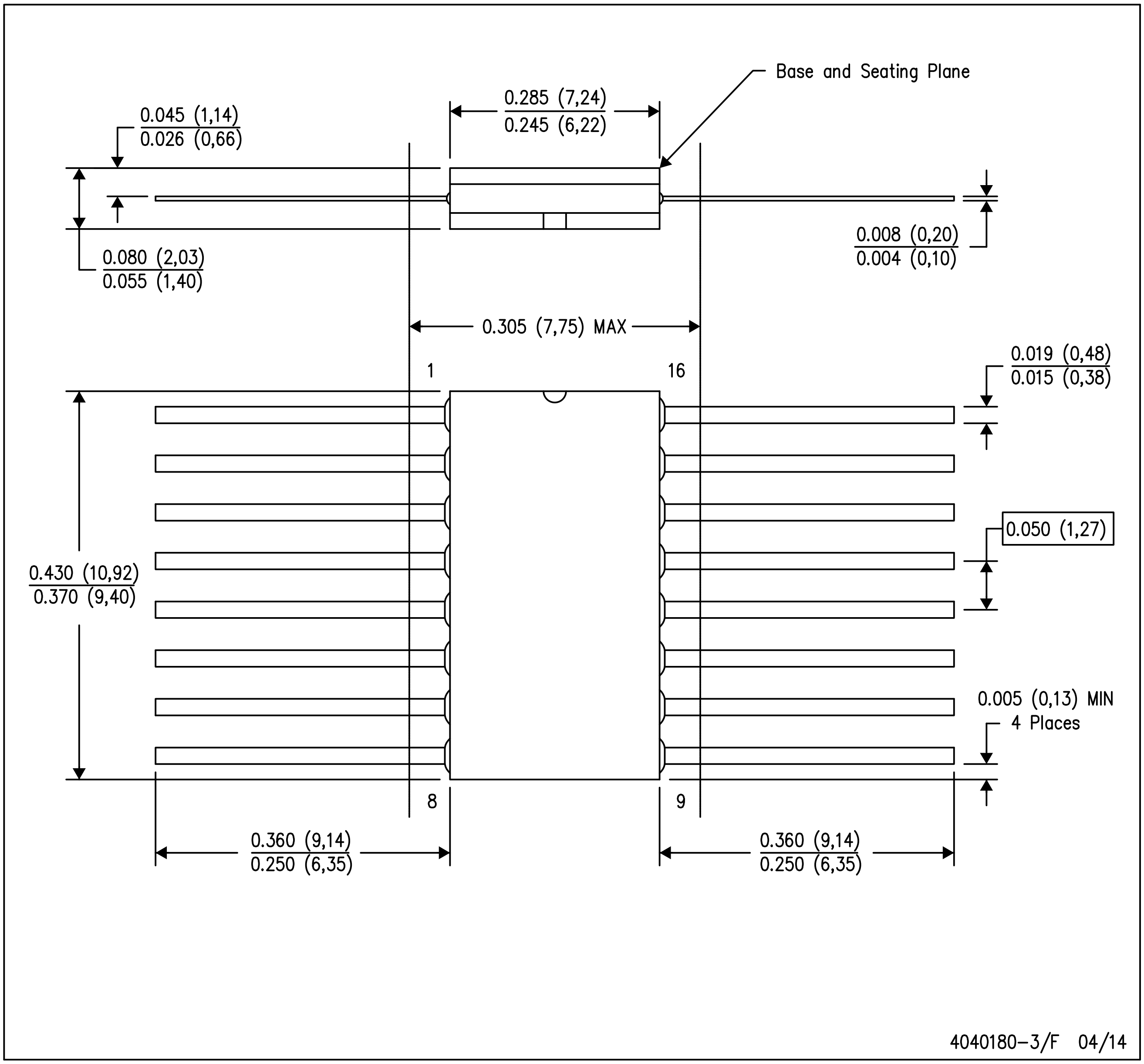
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F16) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

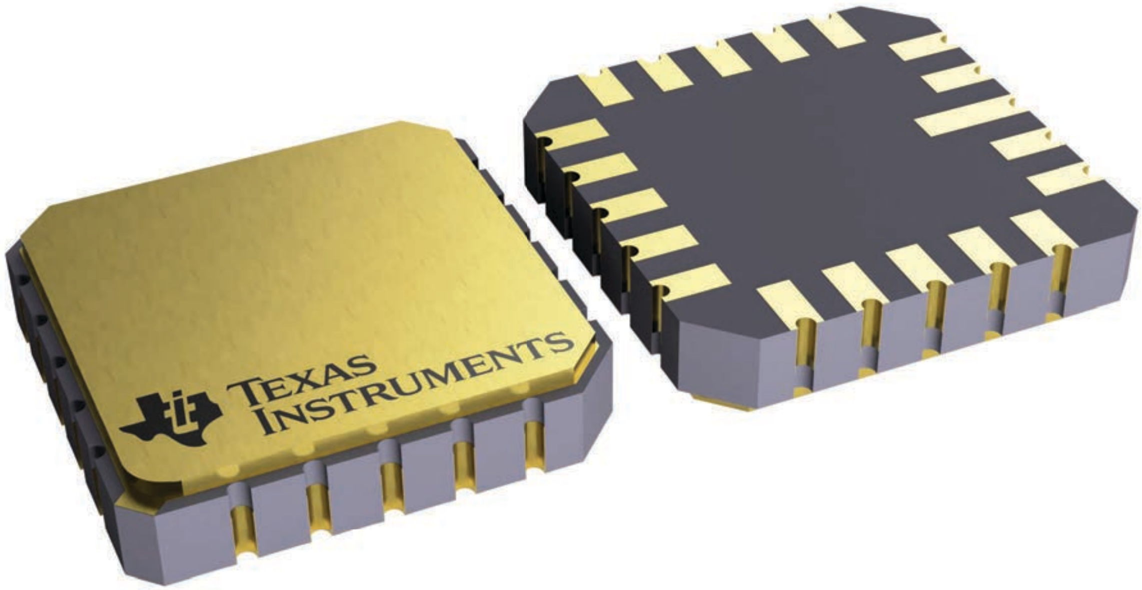
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

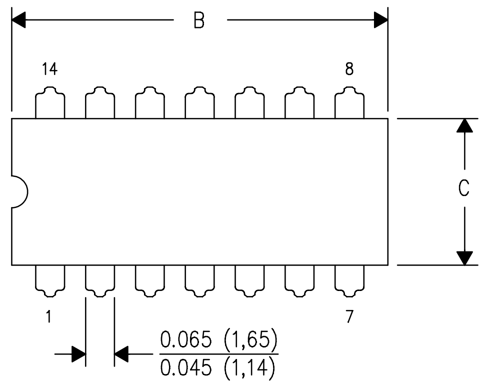
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



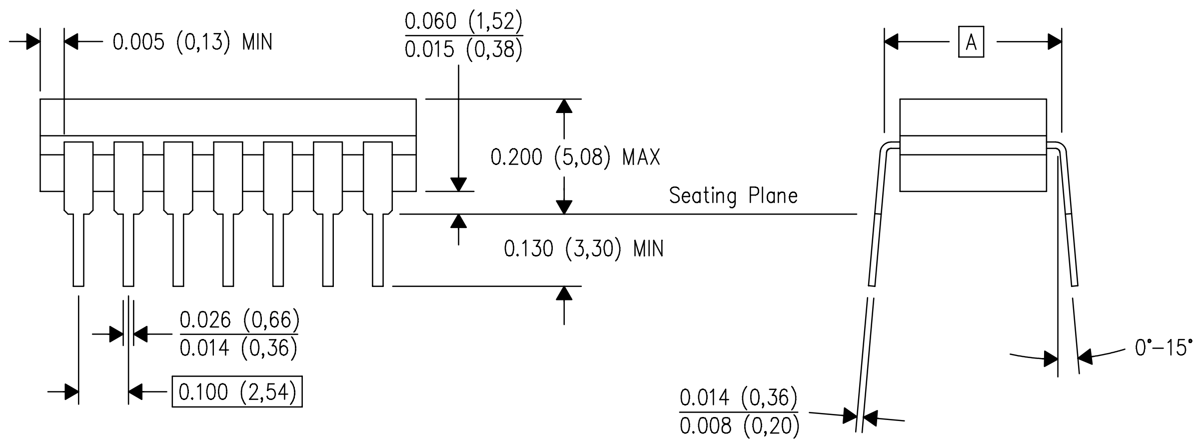
4229370\/A\

J (R-GDIP-T**) CERAMIC DUAL IN-LINE PACKAGE

14 LEADS SHOWN

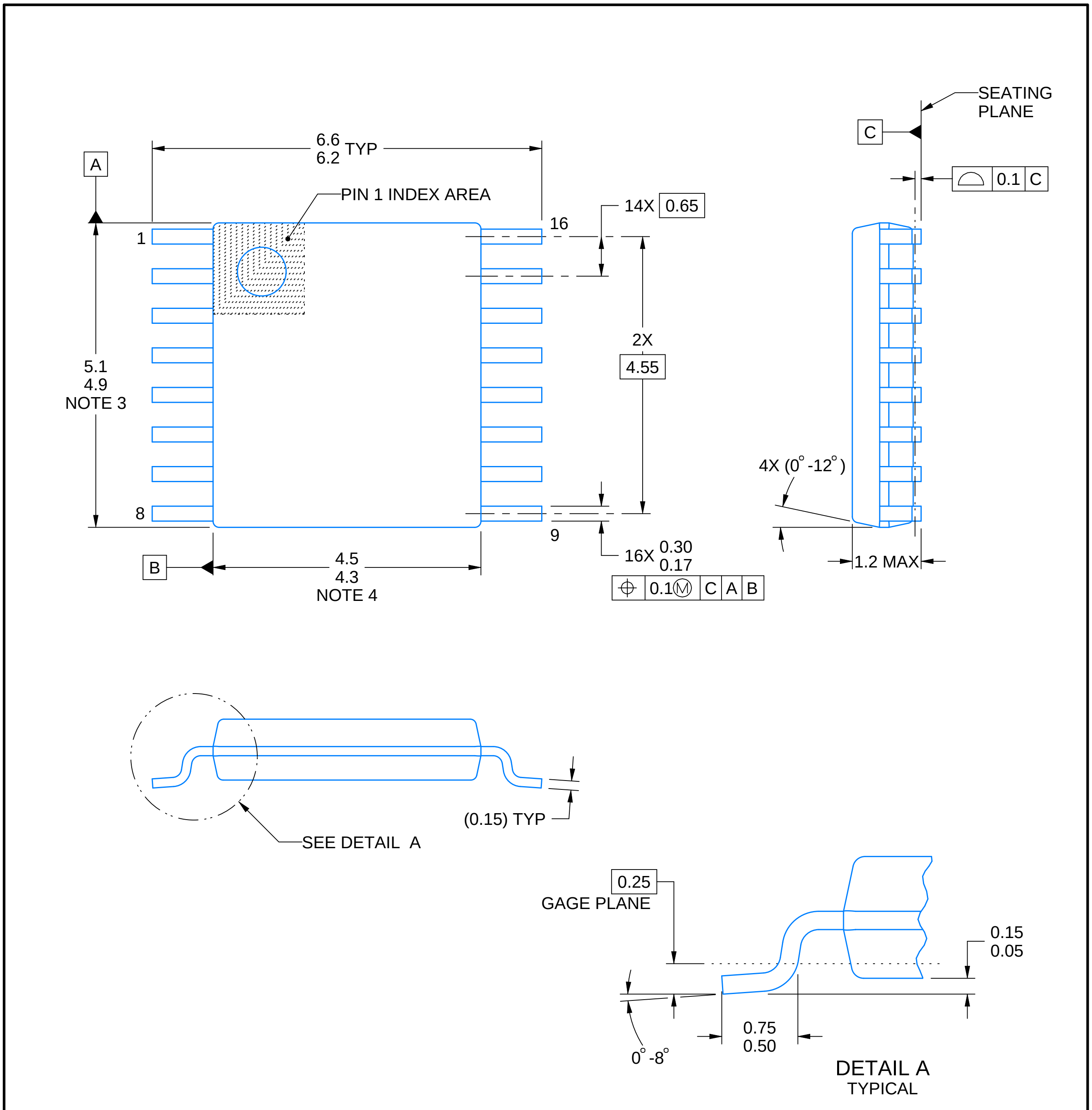


PINS ** / DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

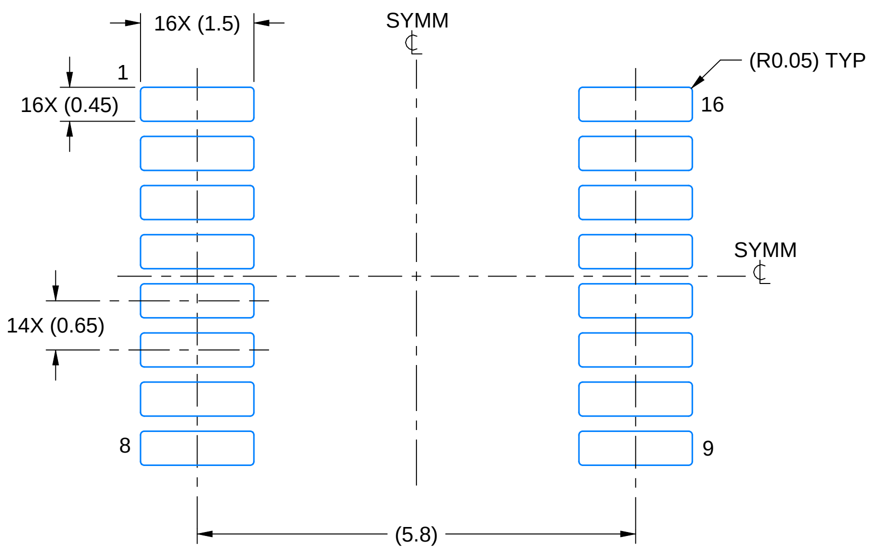
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.



4220204/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

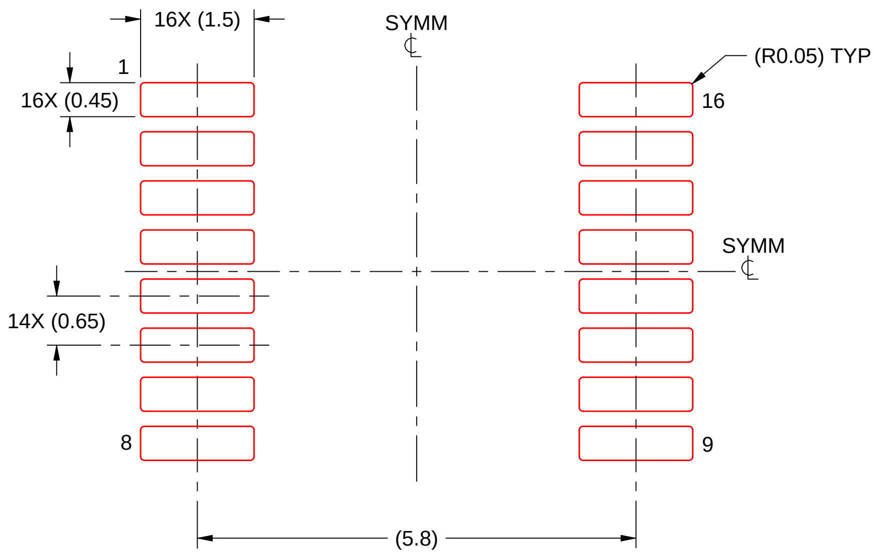
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

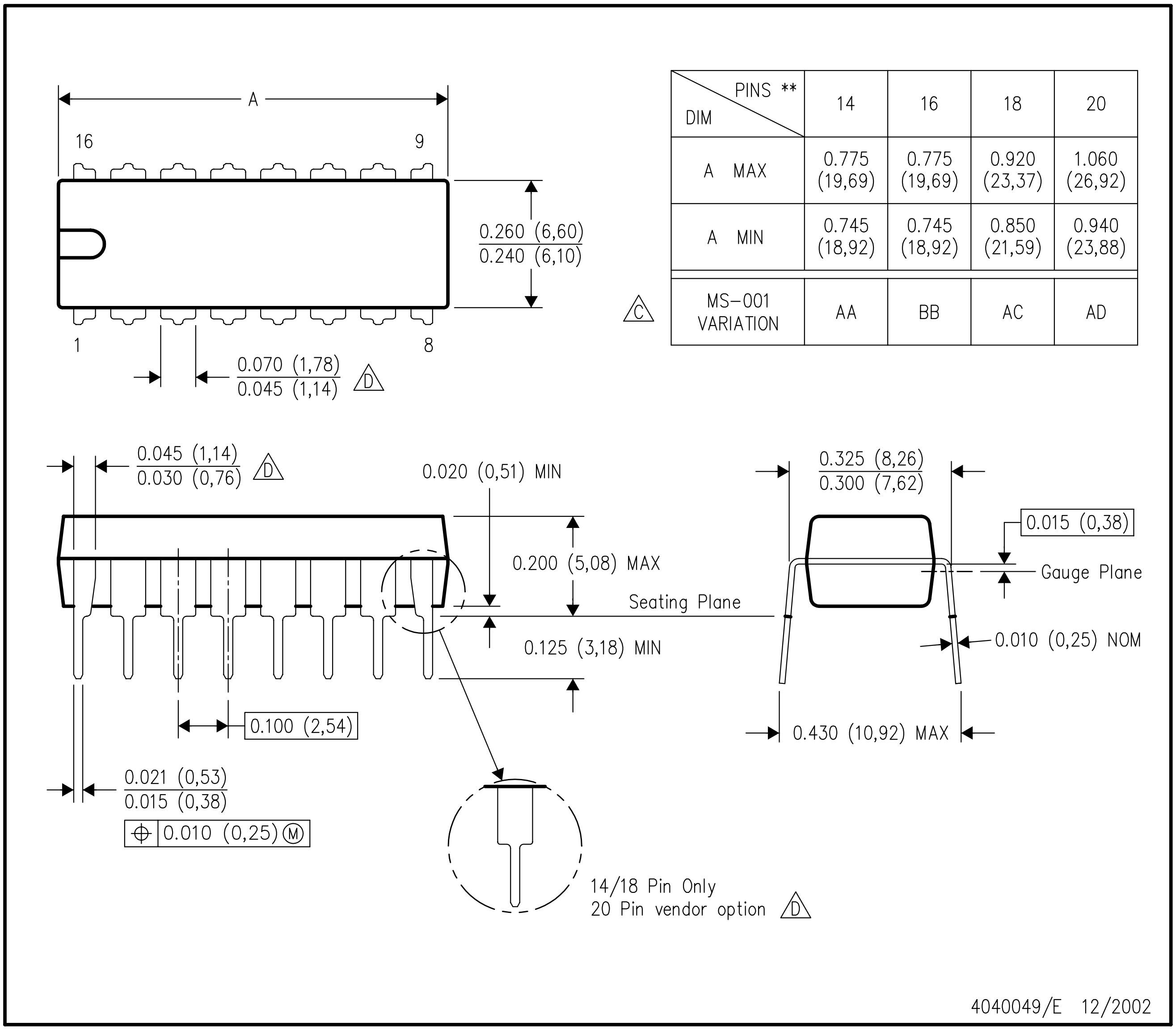
4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- D. The 20 pin end lead shoulder width is a vendor option, either half or full width.